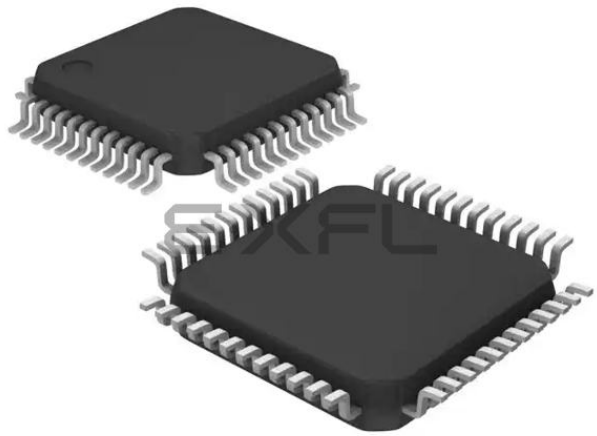
Renesas Electronics America Inc - DF71242D50FPV#Z1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	23
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71242d50fpv-z1

1.2 Block Diagram

The block diagram of this LSI is shown in figure 1.1.

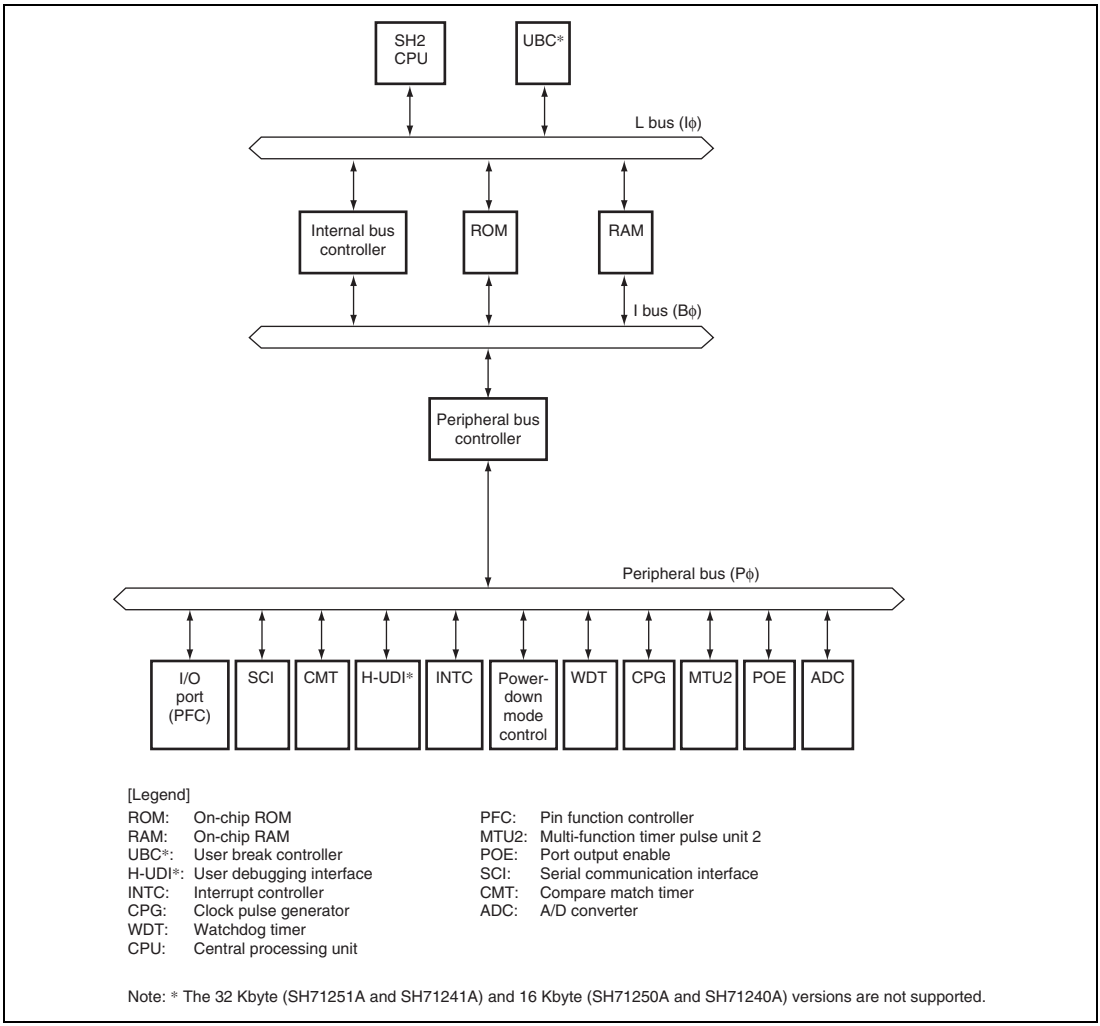


Figure 1.1 Block Diagram

1.4 Pin Functions

Table 1.2 summarizes the pin functions.

Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pin Connect all Vcc pins to the system. There will be no operation if any pins are open.
	Vss	I	Ground	Ground pin Connect all Vss pins to the system power supply (0V). There will be no operation if any pins are open.
	V_{CL}	O	Power supply for internal power-down	External capacitance pins for internal power-down power supply Connect these pins to Vss via a 0.1 to 0.47 μF capacitor (placed close to the pins).
Clock	PLLVss	I	PLL ground	Ground pin for the on-chip PLL oscillator
	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
Operating mode control	MD1	I	Mode set	Sets the operating mode. Do not change values on this pin during operation.
	FWE	I	Flash memory write enable	Pin for flash memory Flash memory can be protected against programming or erasure through this pin.

2.3.3 Immediate Data Formats

Immediate data of eight bits is placed in the instruction code.

For the MOV, ADD, and CMP/EQ instructions, the immediate data is sign-extended to longword and then calculated. For the TST, AND, OR, and XOR instructions, the immediate data is zero-extended to longword and then calculated. Thus, if the immediate data is used for the AND instruction, the upper 24 bits in the destination register are always cleared.

The immediate data of word or longword is not placed in the instruction code. It is placed in a table in memory. The table in memory is accessed by the MOV immediate data instruction in PC relative addressing mode with displacement.

2.4 Features of Instructions

2.4.1 RISC Type

The instructions are RISC-type instructions with the following features:

Fixed 16-Bit Length: All instructions have a fixed length of 16 bits. This improves program code efficiency.

One Instruction per Cycle: Since pipelining is used, basic instructions can be executed in one cycle.

Data Size: The basic data size for operations is longword. Byte, word, or longword can be selected as the memory access size. Byte or word data in memory is sign-extended to longword and then calculated. Immediate data is sign-extended to longword for arithmetic operations or zero-extended to longword size for logical operations.

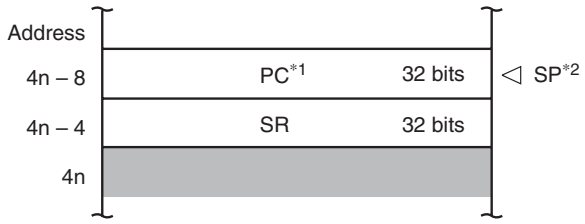
Table 2.2 Word Data Sign Extension

CPU in this LSI		Description	Example of Other CPUs
MOV.W	@(disp,PC),R1	Sign-extended to 32 bits, R1 becomes H'00001234, and is then operated on by the ADD instruction.	ADD.W #H'1234,R0
ADD	R1,R0		
	.....		
.DATA.W	H'1234		

Note: * Immediate data is accessed by @(disp,PC).

6.6.2 Stack after Interrupt Exception Handling

Figure 6.4 shows the stack after interrupt exception handling.



Notes: 1. PC is the start address of the next instruction (instruction at the return address) after the executed instruction.
2. Always make sure that SP is a multiple of 4

Figure 6.4 Stack after Interrupt Exception Handling

6.7 Interrupt Response Time

Table 6.4 lists the interrupt response time, which is the time from the occurrence of an interrupt request until the interrupt exception handling starts and fetching of the first instruction of the interrupt handling routine begins.

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
A/D converter start request delaying function	—	—	—	—	• A/D converter start request at a match between TADCORA_4 and TCNT_4 • A/D converter start request at a match between TADCORB_4 and TCNT_4	—
Interrupt skipping function	—	—	—	• Skips TGRA_3 compare match interrupts	• Skips TCIV_4 interrupts	—

[Legend]

√: Possible

—: Not possible

Notes: 1. This pin is supported only by the SH7125.

2. Input capture is supported only by the SH7125.

Figure 9.1 shows a block diagram of the MTU2.

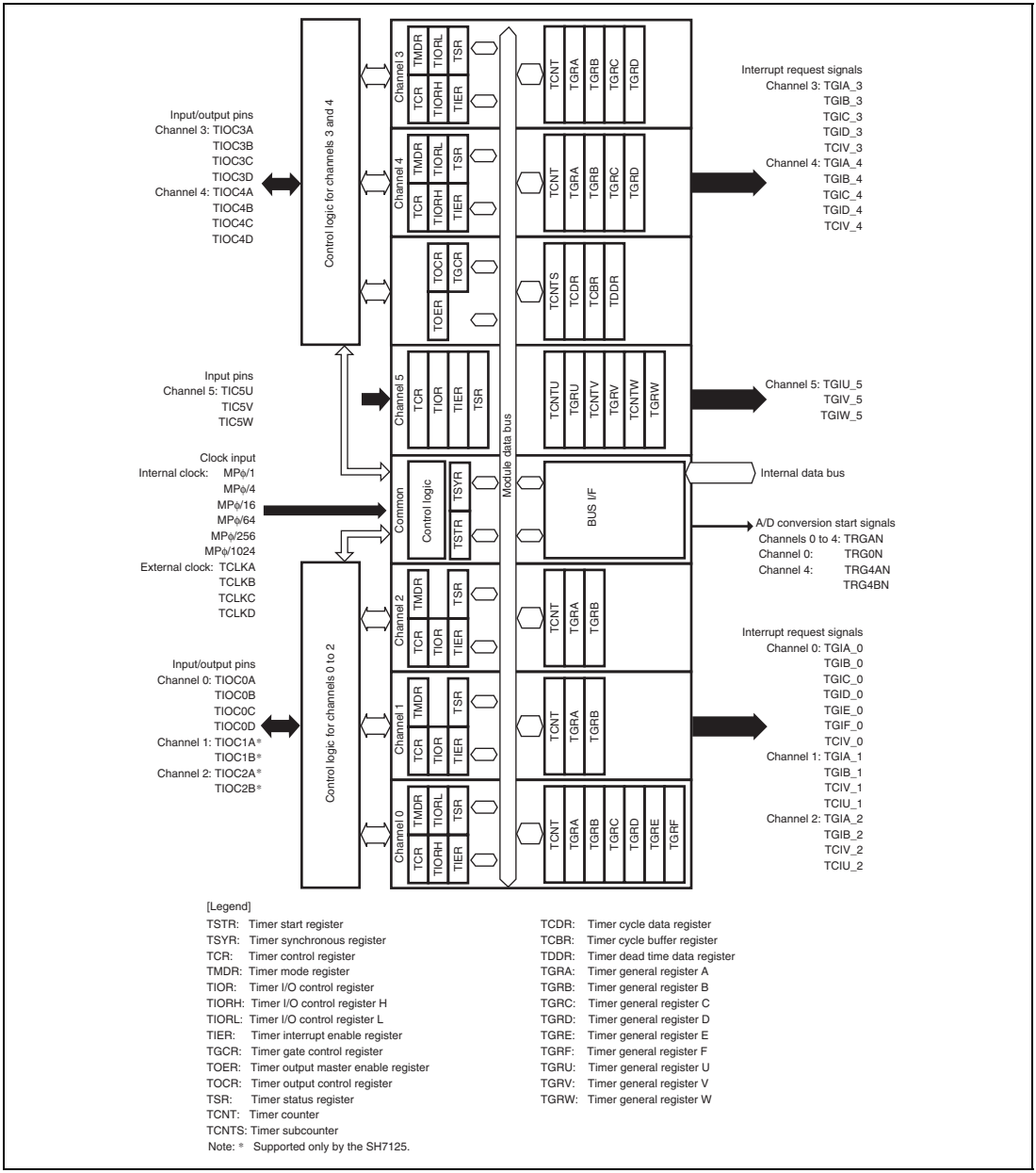


Figure 9.1 Block Diagram of MTU2

Table 9.6 TPSC0 to TPSC2 (Channel 0)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
0	0	0	0	Internal clock: counts on MPϕ/1
			1	Internal clock: counts on MPϕ/4
		1	0	Internal clock: counts on MPϕ/16
			1	Internal clock: counts on MPϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	External clock: counts on TCLKC pin input
			1	External clock: counts on TCLKD pin input

Table 9.7 TPSC0 to TPSC2 (Channel 1)

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Internal clock: counts on MPϕ/1
			1	Internal clock: counts on MPϕ/4
		1	0	Internal clock: counts on MPϕ/16
			1	Internal clock: counts on MPϕ/64
	1	0	0	External clock: counts on TCLKA pin input
			1	External clock: counts on TCLKB pin input
		1	0	Internal clock: counts on MPϕ/256
			1	Counts on TCNT_2 overflow/underflow

Note: This setting is ignored when channel 1 is in phase counting mode.

Table 9.19 TIORL_4 (Channel 4)

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_4 Function**	**TIOC4D Pin Function**
0	0	0	0	Output compare register*2	Output retained*1
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register*2	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Notes: 1. After power-on reset, 0 is output until TIOR is set.

2. When the BFB bit in TMDR_4 is set to 1 and TGRD_4 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

- TIER2_0

Bit:	7	6	5	4	3	2	1	0
	TTGE2	-	-	-	-	-	TGIEF	TGIEE
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TTGE2	0	R/W	A/D Converter Start Request Enable 2 Enables or disables generation of A/D converter start requests by compare match between TCNT_0 and TGRE_0. 0: A/D converter start request generation by compare match between TCNT_0 and TGRE_0 disabled 1: A/D converter start request generation by compare match between TCNT_0 and TGRE_0 enabled
6 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	TGIEF	0	R/W	TGR Interrupt Enable F Enables or disables interrupt requests by compare match between TCNT_0 and TGRF_0. 0: Interrupt requests (TGIF) by TGFE bit disabled 1: Interrupt requests (TGIF) by TGFE bit enabled
0	TGIEE	0	R/W	TGR Interrupt Enable E Enables or disables interrupt requests by compare match between TCNT_0 and TGRE_0. 0: Interrupt requests (TGIE) by TGEE bit disabled 1: Interrupt requests (TGIE) by TGEE bit enabled

Bit	Bit Name	Initial Value	R/W	Description
1	CMFV5	0	R/(W)*[1]	Compare Match/Input Capture Flag V5 Status flag that indicates the occurrence of TGRV_5 input capture or compare match. [Setting conditions] • When TCNTV_5 = TGRV_5 and TGRV_5 is functioning as output compare register • When TCNTV_5 value is transferred to TGRV_5 by input capture signal and TGRV_5 is functioning as input capture register • When TCNTV_5 value is transferred to TGRV_5 and TGRV_5 is functioning as a register for measuring the pulse width of the external input signal. The transfer timing is specified by the IOC bits in timer I/O control register V_5 (TIORV_5)*[2] [Clearing condition] • When 0 is written to CMFV5 after reading CMFV5 = 1

9.3.30 Timer Waveform Control Register (TWCR)

TWCR is an 8-bit readable/writable register that controls the waveform when synchronous counter clearing occurs in TCNT_3 and TCNT_4 in complementary PWM mode and specifies whether to clear the counters at TGRA_3 compare match. The CCE bit and WRE bit in TWCR must be modified only while TCNT stops.

Bit:	7	6	5	4	3	2	1	0
	CCE	-	-	-	-	-	-	WRE
Initial value:	0*	0	0	0	0	0	0	0
R/W:	R/(W)	R	R	R	R	R	R	R/(W)

Note: * Do not set to 1 when complementary PWM mode is not selected.

Bit	Bit Name	Initial Value	R/W	Description
7	CCE	0*	R/(W)	Compare Match Clear Enable Specifies whether to clear counters at TGRA_3 compare match in complementary PWM mode. 0: Does not clear counters at TGRA_3 compare match 1: Clears counters at TGRA_3 compare match [Setting condition] • When 1 is written to CCE after reading CCE = 0
6 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

14. Output Waveform Control at Synchronous Counter Clearing in Complementary PWM Mode

Setting the WRE bit in TWCR to 1 suppresses initial output when synchronous counter clearing occurs in the Tb interval at the trough in complementary PWM mode and controls abrupt change in duty cycle at synchronous counter clearing.

Initial output suppression is applicable only when synchronous clearing occurs in the Tb interval at the trough as indicated by (10) or (11) in figure 9.56. When synchronous clearing occurs outside that interval, the initial value specified by the OLS bits in TOCR is output. Even in the Tb interval at the trough, if synchronous clearing occurs in the initial value output period (indicated by (1) in figure 9.56) immediately after the counters start operation, initial value output is not suppressed.

In the MTU2, synchronous clearing generated in channels 0 to 2 in the MTU2 can cause counter clearing.

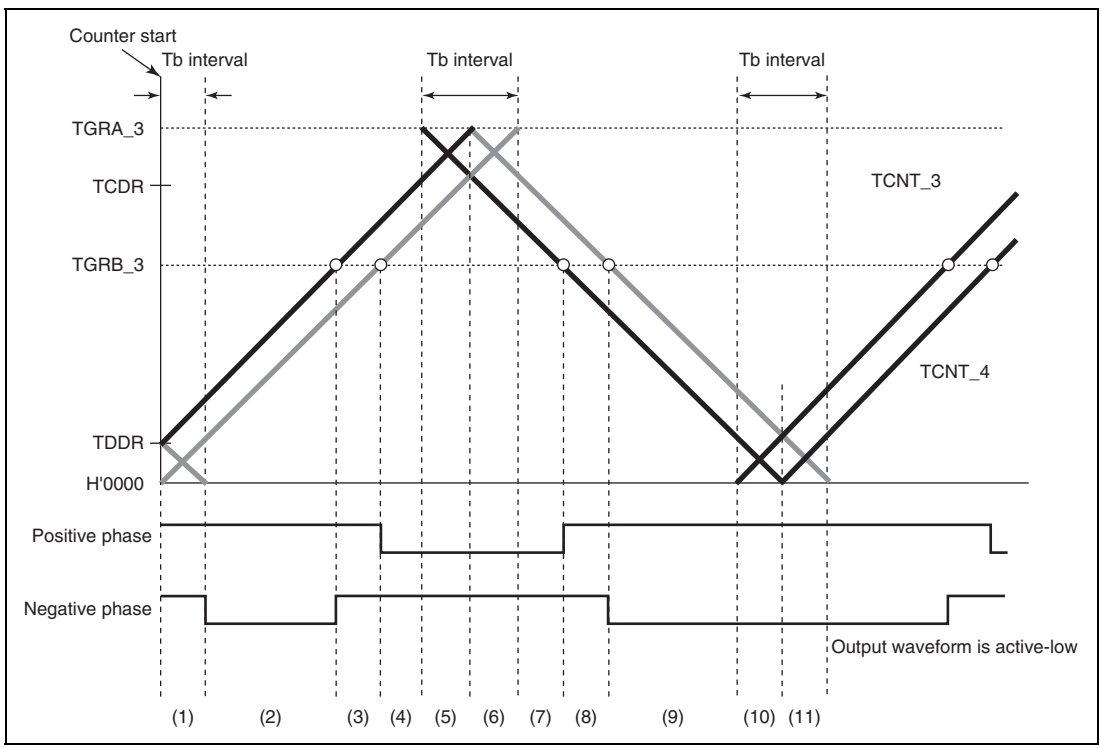
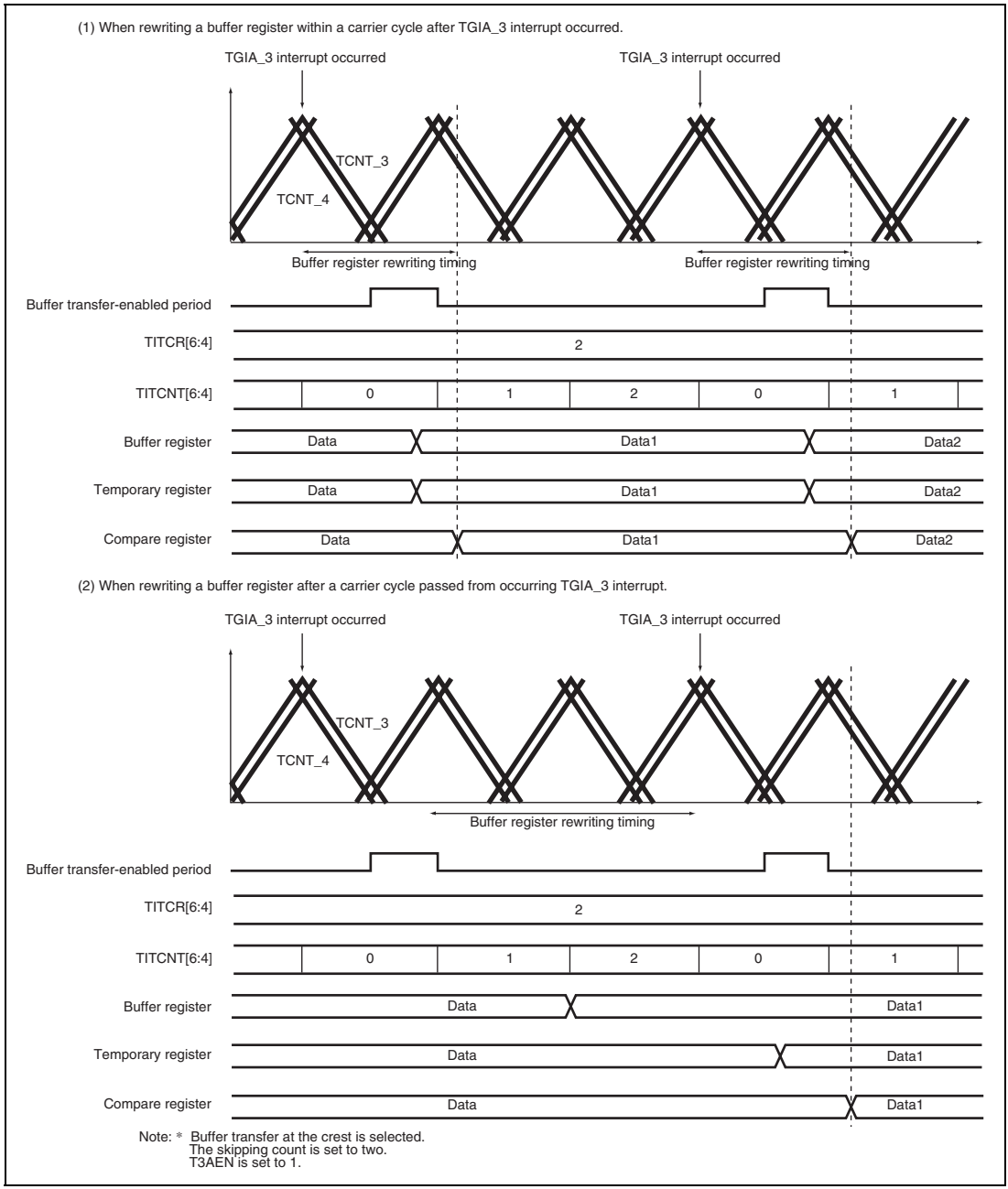


Figure 9.56 Timing for Synchronous Counter Clearing



Note: * Buffer transfer at the crest is selected.
The skipping count is set to two.
T3AEN is set to 1.

Figure 9.71 Example of Operation when Buffer Transfer is Linked with Interrupt Skipping (BTE1 = 1 and BTE0 = 0)

10.4 Operation

Table 10.4 shows the target pins for high-impedance control and conditions to place the pins in high-impedance state.

Table 10.4 Target Pins and Conditions for High-Impedance Control

Pins	Conditions	Detailed Conditions
MTU2 high-current pins (PE9/TIOC3B and PE11/TIOC3D)	Input level detection, output level comparison, or SPOER setting	MTU2P1CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE12/TIOC4A and PE14/TIOC4C)	Input level detection, output level comparison, or SPOER setting	MTU2P2CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE13/TIOC4B and PE15/TIOC4D)	Input level detection, output level comparison, or SPOER setting	MTU2P3CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 channel 0 pin (PE0/TIOC0A)	Input level detection or SPOER setting	MTU2PE0ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE1/TIOC0B)	Input level detection or SPOER setting	MTU2PE1ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE2/TIOC0C)	Input level detection or SPOER setting	MTU2PE2ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE3/TIOC0D)	Input level detection or SPOER setting	MTU2PE3ZE ((POE8F • POE8E) + (MTU2CH0HIZ))

10.4.1 Input Level Detection Operation

If the input conditions set by ICSR1 occur on the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ pins, the high-current pins and the pins for channel 0 of the MTU2 are placed in high-impedance state. Note however, that these high-current and MTU2 pins enter high-impedance state only when general input/output function or MTU2 function is selected for these pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ pins, the high-current pins and the pins for channel 0 of the MTU2 are placed in high-impedance state. Figure 10.2 shows a sample timing after the level changes in input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*, and $\overline{\text{POE8}}$ pins until the respective pins enter high-impedance state.

Note: * This pin is supported only by the SH7125.

Bit	Bit Name	Initial Value	R/W	Description
8	STC	0	R/W	State Control Sets the A/D conversion time in combination with the CKSL1 and CKSL0 bits. 0: 50 states 1: 64 states When changing the A/D conversion time, first clear the ADST bit to 0.
7, 6	CKSL[1:0]	00	R/W	Clock Select 1 and 0 Select the A/D conversion time. 00: Pϕ/4 01: Pϕ/3 10: Pϕ/2 11: Pϕ When changing the A/D conversion time, first clear the ADST bit to 0. CKSL[1:0] = B'11 can be set while Pϕ ≤ 25 MHz.
5, 4	ADM[1:0]	00	R/W	A/D Mode 1 and 0 Select the A/D conversion mode. 00: Single mode 01: 4-channel scan mode 10: Setting prohibited 11: 2-channel scan mode When changing the operating mode, first clear the ADST bit to 0.
3	ADCS	0	R/W	A/D Continuous Scan Selects either single-cycle scan or continuous scan in scan mode. This bit is valid only when scan mode is selected. 0: Single-cycle scan 1: Continuous scan When changing the operating mode, first clear the ADST bit to 0.

13.4.3 Single-Cycle Scan Mode

In single-cycle scan mode, A/D conversion is to be performed once on the specified channels (up to four channels).

1. When the ADST bit in ADCR is set to 1 by a software, MTU2, or external trigger input, A/D conversion starts on the channel with the lowest number in the group (AN0, AN1, ..., AN3).
2. When A/D conversion for each channel is completed, the result is sequentially transferred to the A/D data register corresponding to each channel.
3. When conversion of all the selected channels is completed, the ADF bit in ADCSR is set to 1. If the ADIE bit is set to 1 at this time, an ADI interrupt is requested after A/D conversion ends.
4. After A/D conversion ends, the ADST bit is automatically cleared to 0 and the A/D converter enters the idle state. When the ADST bit is cleared to 0 during A/D conversion, A/D conversion stops and the A/D converter enters the idle state.

13.4.4 Input Sampling and A/D Conversion Time

The A/D converter has a built-in sample-and-hold circuit for each module. The A/D converter samples the analog input when the A/D conversion start delay time (t_D) has passed after the ADST bit in ADCR is set to 1, then starts conversion. Figure 13.2 shows the A/D conversion timing. Table 13.4 shows the A/D conversion time.

As indicated in figure 13.2, the A/D conversion time (t_{CONV}) includes t_D and the input sampling time (t_{SPL}). The length of t_D varies depending on the timing of the write access to ADCR. The total conversion time therefore varies within the ranges indicated in table 13.4.

In scan mode, the values given in table 13.4 apply to the first conversion time. The values given in table 13.5 apply to the second and subsequent conversions.

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
54	PF6/AN6	PF6/AN6
53	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{\text{TRST}}$, TDI, TDO, TCK, and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ when using the E10A (in $\overline{\text{ASEMD0}}$ = low).
2. E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.

Table 15.4 SH7124 Pin Functions in Each Operating Mode

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
4, 17	Vcc	Vcc
6, 19	Vss	Vss
8, 25	VCL	VCL
48	AVcc	AVcc
39	AVss	AVss
35	PLLVss	PLLVss
30	EXTAL	EXTAL
29	XTAL	XTAL
34	MD1	MD1
33	FWE/($\overline{\text{ASEBRKAK}}$/ $\overline{\text{ASEBRK}}$*[1])	FWE
27	$\overline{\text{RES}}$	$\overline{\text{RES}}$
28	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
32	NMI	NMI
31	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$
26	PA0	PA0/$\overline{\text{POE0}}$/RXD0
24	PA1	PA1/$\overline{\text{POE1}}$/TXD0
23	PA3/($\overline{\text{TRST}}$*[1])	PA3/IRQ1/RXD1

16.5 Usage Notes

16.5.1 Handling of Unused Pins

Unused pins should be connected to V_{CC} or GND via a resistor and fixed high or low. Pins PF0 to PF7 should be connected to AV_{CC} or AV_{SS} via a resistor. However, see the descriptions of the associated modules regarding the handling of pins NMI, EXTAL, XTAL, and WDTOVF.

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep	Module
TSR_1	Initialized	Retained	Initialized	Initialized	Retained	MTU2
TCNT_1	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_1	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_1	Initialized	Retained	Initialized	Initialized	Retained	
TICCR	Initialized	Retained	Initialized	Initialized	Retained	
TCR_2	Initialized	Retained	Initialized	Initialized	Retained	
TMDR_2	Initialized	Retained	Initialized	Initialized	Retained	
TIOR_2	Initialized	Retained	Initialized	Initialized	Retained	
TIER_2	Initialized	Retained	Initialized	Initialized	Retained	
TSR_2	Initialized	Retained	Initialized	Initialized	Retained	
TCNT_2	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_2	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_2	Initialized	Retained	Initialized	Initialized	Retained	
TCNTU_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRU_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRU_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORU_5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTV_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRV_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRV_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORV_5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTW_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRW_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRW_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORW_5	Initialized	Retained	Initialized	Initialized	Retained	
TSR_5	Initialized	Retained	Initialized	Initialized	Retained	
TIER_5	Initialized	Retained	Initialized	Initialized	Retained	
TSTR5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTCMPCLR	Initialized	Retained	Initialized	Initialized	Retained	