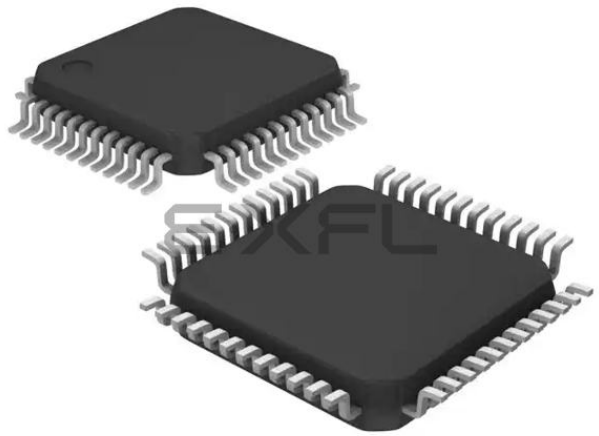
Renesas Electronics America Inc - DF71243N50FPV#Z1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71243n50fpv-z1

Table 1.1 Features

Items	Specification
CPU	• Central processing unit with an internal 32-bit RISC (Reduced Instruction Set Computer) architecture • Instruction length: 16-bit fixed length for improved code efficiency • Load-store architecture (basic operations are executed between registers) • Sixteen 32-bit general registers • Five-stage pipeline • On-chip multiplier: Multiplication operations (32 bits × 32 bits → 64 bits) executed in two to five cycles • C language-oriented 62 basic instructions Note: Some specifications on slot illegal instruction exception handling in this LSI differ from those of the conventional SH-2. For details, see section 5.8.4, Notes on Slot Illegal Instruction Exception Handling.
Operating modes	• Operating modes — Single chip mode • Operating states — Program execution state — Exception handling state • Power-down modes — Sleep mode — Software standby mode — Module standby mode
User break controller (UBC)*	• Addresses, data values, type of access, and data size can all be set as break conditions • Supports a sequential break function • Two break channels
On-chip ROM	• 128 kbytes (SH71253, SH71243) • 64 kbytes (SH71252, SH71242) • 32 kbytes (SH71251A, SH71241A) • 16 kbytes (SH71250A, SH71240A)
On-chip RAM	• 8 kbytes (SH71253, SH71243, SH71252, SH71242, SH71251A, SH71241A) • 4 kbytes (SH71250A, SH71240A)

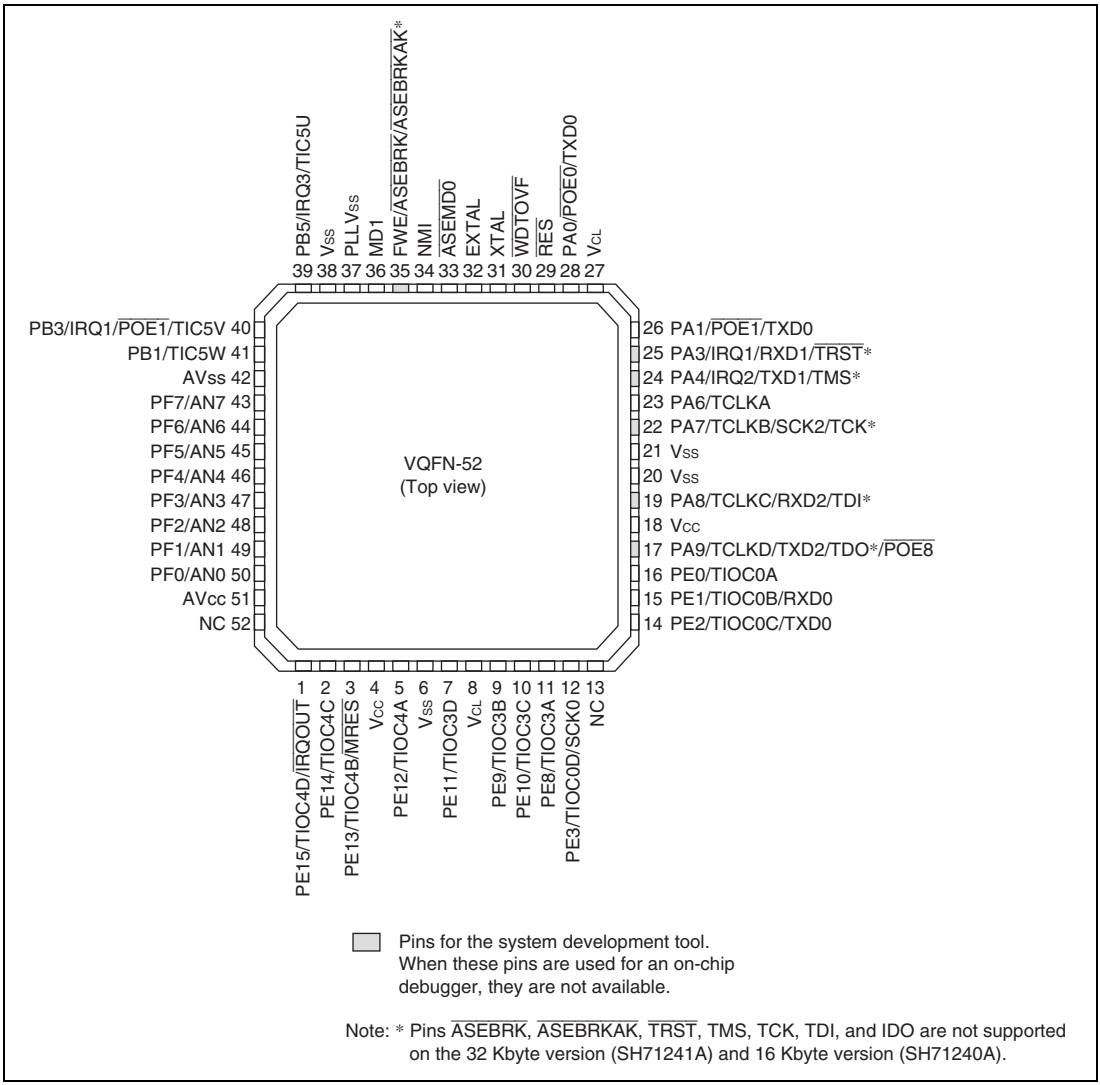

Figure 1.3 (2) Pin Assignments of SH7124

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	IPR[15:12]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
11 to 8	IPR[11:8]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)

Bus cycle: L bus/instruction fetch (after instruction execution)/read (operand size is not included in the condition)

<Channel B>

Address: H'00008010, Address mask: H'00000006

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

A user break occurs after an instruction with addresses H'00008000 to H'00008FFE is executed or before an instruction with addresses H'00008010 to H'00008016 are executed.

Break Condition Specified for L Bus Data Access Cycle:

(Example 2-1)

- Register specifications

  BARA = H'00123456, BAMRA = H'00000000, BBRA = H'0064, BDRA = H'12345678, BDMRA = H'FFFFFFFF, BARB = H'000ABCDE, BAMRB = H'000000FF, BBRB = H'006A, BDRB = H'0000A512, BDMRB = H'00000000, BRCR = H'00000080

  Specified conditions: Channel A/channel B independent mode

  <Channel A>

  Address: H'00123456, Address mask: H'00000000

  Data: H'12345678, Data mask: H'FFFFFFFF

  Bus cycle: L bus/data access/read (operand size is not included in the condition)

  <Channel B>

  Address: H'000ABCDE, Address mask: H'000000FF

  Data: H'0000A512, Data mask: H'00000000

  Bus cycle: L bus/data access/write/word

  On channel A, a user break occurs with longword read from address H'00123454, word read from address H'00123456, or byte read from address H'00123456. On channel B, a user break occurs when word H'A512 is written in addresses H'000ABC00 to H'000ABCFE.

Section 8 Bus State Controller (BSC)

The bus state controller (BSC) controls data transmission and reception between the internal buses (L bus, I bus, and peripheral bus) and also controls the CPU's access to the on-chip FLASH, on-chip RAM, and on-chip peripheral I/O.

8.1 Features

- On-chip FLASH and RAM interface
  - 32-bit data access per one clock cycle (I ϕ synchronous)

8.2 Address Map

The address map is listed in table 8.1.

Table 8.1 Address Map

Address	Type of Memory	Size				Bus Width
		128 Kbytes Version	64 Kbytes Version	32 Kbytes Version	16 Kbytes Version	
H'00000000 to H'00003FFF	On-chip FLASH	128 Kbytes	64 Kbytes	32 Kbytes	16 Kbytes	32
H'00004000 to H'00007FFF					Reserved	
H'00008000 to H'0000FFFF				Reserved		
H'00010000 to H'0001FFFF			Reserved			
H'00020000 to H'FFFF9FFF	Reserved	—	—	—	—	—
H'FFFFA000 to H'FFFFAFFF	On-chip RAM	8 Kbytes	8 Kbytes	8 Kbytes	8 Kbytes	32
H'FFFFB000 to H'FFFFBFFF					Reserved	
H'FFFFC000 to H'FFFFFFFF	On-chip peripheral I/O	128 Kbytes	64 Kbytes	64 Kbytes	64 Kbytes	8/16

8.3 Access to on-chip FLASH and on-chip RAM

Access to the on-chip FLASH for read is synchronized with I ϕ clock and is executed in one clock cycle. For details on programming and erasing, see section 17, Flash Memory.

Access to the on-chip RAM for read/write is synchronized with I ϕ clock and is executed in one clock cycle. For details, see section 18, RAM.

9.3 Register Descriptions

The MTU2 has the following registers. For details on register addresses and register states during each process, see section 20, List of Registers. To distinguish registers in each channel, an underscore and the channel number are added as a suffix to the register name; TCR for channel 0 is expressed as TCR_0.

Table 9.3 Register Configuration

Register Name	Abbreviation	R/W	Initial value	Address	Access Size
Timer control register_3	TCR_3	R/W	H'00	H'FFFFC200	8, 16, 32
Timer control register_4	TCR_4	R/W	H'00	H'FFFFC201	8
Timer mode register_3	TMDR_3	R/W	H'00	H'FFFFC202	8, 16
Timer mode register_4	TMDR_4	R/W	H'00	H'FFFFC203	8
Timer I/O control register H_3	TIORH_3	R/W	H'00	H'FFFFC204	8, 16, 32
Timer I/O control register L_3	TIORL_3	R/W	H'00	H'FFFFC205	8
Timer I/O control register H_4	TIORH_4	R/W	H'00	H'FFFFC206	8, 16
Timer I/O control register L_4	TIORL_4	R/W	H'00	H'FFFFC207	8
Timer interrupt enable register_3	TIER_3	R/W	H'00	H'FFFFC208	8, 16
Timer interrupt enable register_4	TIER_4	R/W	H'00	H'FFFFC209	8
Timer output master enable register	TOER	R/W	H'C0	H'FFFFC20A	8
Timer gate control register	TGCR	R/W	H'80	H'FFFFC20D	8
Timer output control register 1	TOCR1	R/W	H'00	H'FFFFC20E	8, 16
Timer output control register 2	TOCR2	R/W	H'00	H'FFFFC20F	8
Timer counter_3	TCNT_3	R/W	H'0000	H'FFFFC210	16, 32
Timer counter_4	TCNT_4	R/W	H'0000	H'FFFFC212	16
Timer cycle data register	TCDR	R/W	H'FFFF	H'FFFFC214	16, 32
Timer dead time data register	TDDR	R/W	H'FFFF	H'FFFFC216	16
Timer general register A_3	TGRA_3	R/W	H'FFFF	H'FFFFC218	16, 32
Timer general register B_3	TGRB_3	R/W	H'FFFF	H'FFFFC21A	16
Timer general register A_4	TGRA_4	R/W	H'FFFF	H'FFFFC21C	16, 32
Timer general register B_4	TGRB_4	R/W	H'FFFF	H'FFFFC21E	16

9.3.29 Timer Dead Time Enable Register (TDER)

TDER is an 8-bit readable/writable register that controls dead time generation in complementary PWM mode. The MTU2 has one TDER in channel 3. TDER must be modified only while TCNT stops.

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	TDER
Initial value:	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/(W)

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TDER	1	R/(W)	Dead Time Enable Specifies whether to generate dead time. 0: Does not generate dead time 1: Generates dead time* [Clearing condition] • When 0 is written to TDER after reading TDER = 1

Note: * TDDR must be set to 1 or a larger value.

9.3.30 Timer Waveform Control Register (TWCR)

TWCR is an 8-bit readable/writable register that controls the waveform when synchronous counter clearing occurs in TCNT_3 and TCNT_4 in complementary PWM mode and specifies whether to clear the counters at TGRA_3 compare match. The CCE bit and WRE bit in TWCR must be modified only while TCNT stops.

Bit:	7	6	5	4	3	2	1	0
	CCE	-	-	-	-	-	-	WRE
Initial value:	0*	0	0	0	0	0	0	0
R/W:	R/(W)	R	R	R	R	R	R	R/(W)

Note: * Do not set to 1 when complementary PWM mode is not selected.

Bit	Bit Name	Initial Value	R/W	Description
7	CCE	0*	R/(W)	Compare Match Clear Enable Specifies whether to clear counters at TGRA_3 compare match in complementary PWM mode. 0: Does not clear counters at TGRA_3 compare match 1: Clears counters at TGRA_3 compare match [Setting condition] • When 1 is written to CCE after reading CCE = 0
6 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

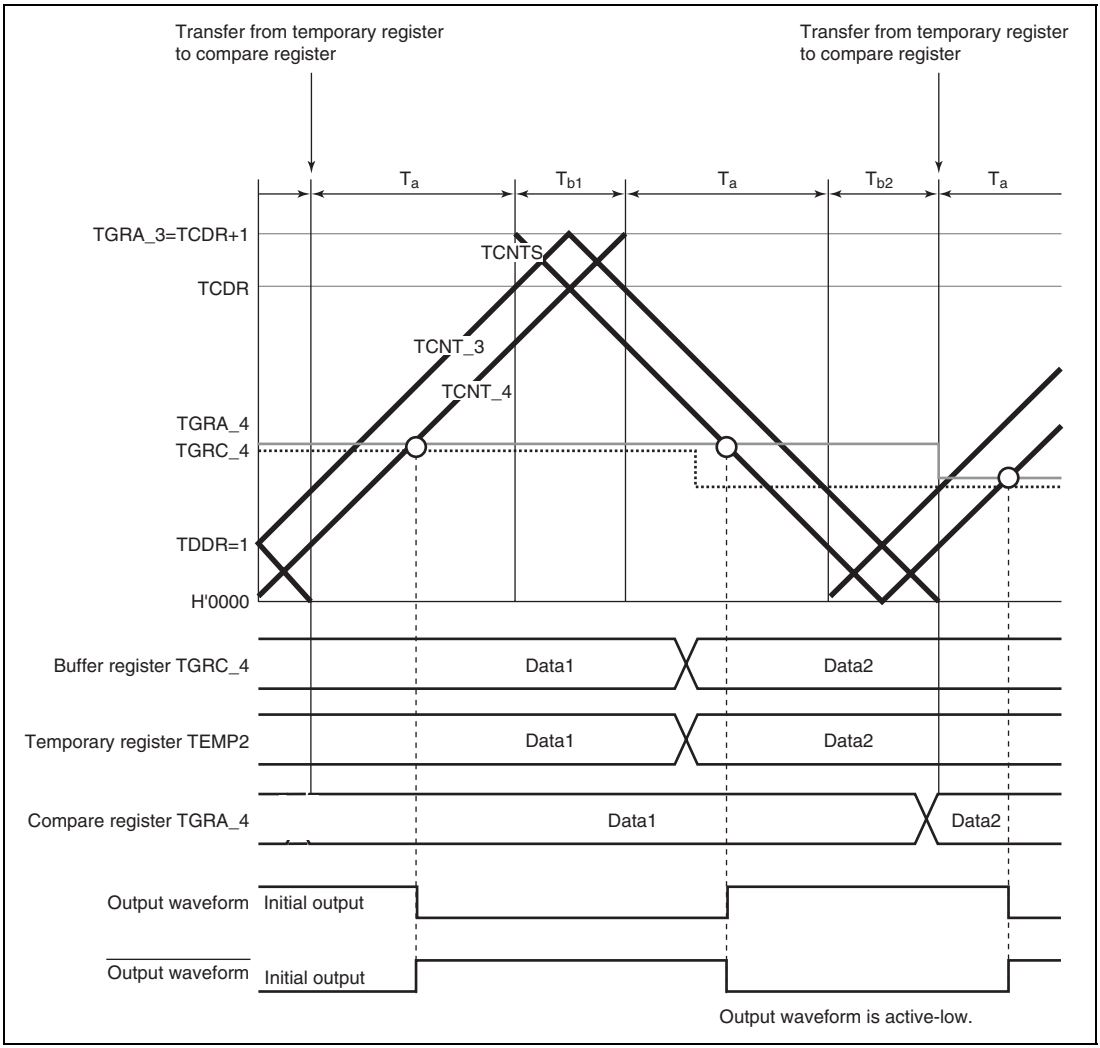

Figure 9.41 Example of Operation without Dead Time

7. PWM Cycle Setting

In complementary PWM mode, the PWM pulse cycle is set in two registers—TGRA_3, in which the TCNT_3 upper limit value is set, and TCDR, in which the TCNT_4 upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:

With dead time: TGRA_3 set value = TCDR set value + TDDR set value
Without dead time: TGRA_3 set value = TCDR set value + 1

The TGRA_3 and TCDR settings are made by setting the values in buffer registers TGRC_3 and TCBR. The values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in the timer mode register (TMDR).

The updated PWM cycle is reflected from the next cycle when the data update is performed at the crest, and from the current cycle when performed in the trough. Figure 9.42 illustrates the operation when the PWM cycle is updated at the crest.

See the following section, Register Data Updating, for the method of updating the data in each buffer register.

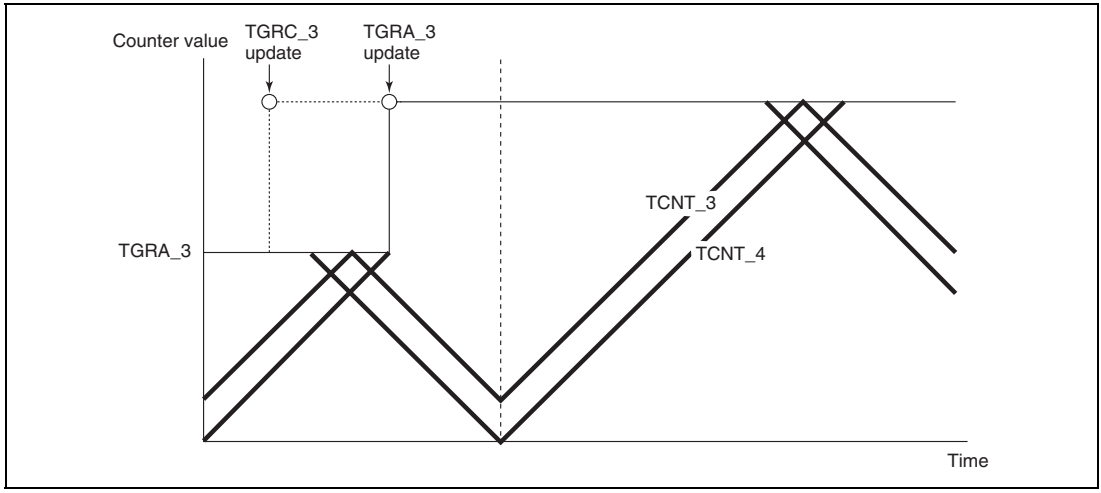

Figure 9.42 Example of PWM Cycle Updating

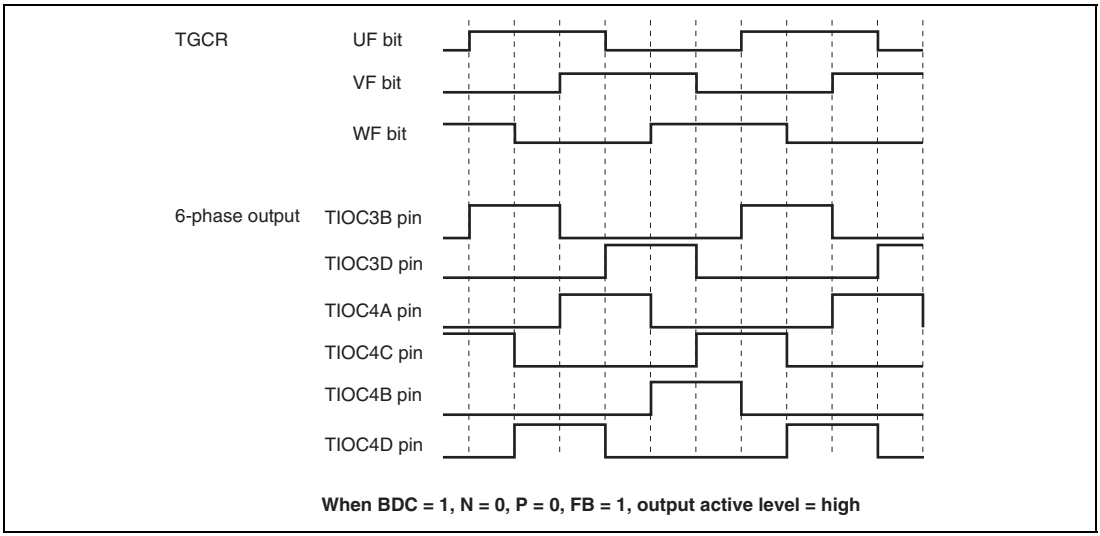

Figure 9.65 Example of Output Phase Switching by Means of UF, VF, WF Bit Settings (1)

Pin initialization procedures are described below for the numbered combinations in table 9.59. The active level is assumed to be low.

Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in Normal Mode: Figure 9.124 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in normal mode after re-setting.

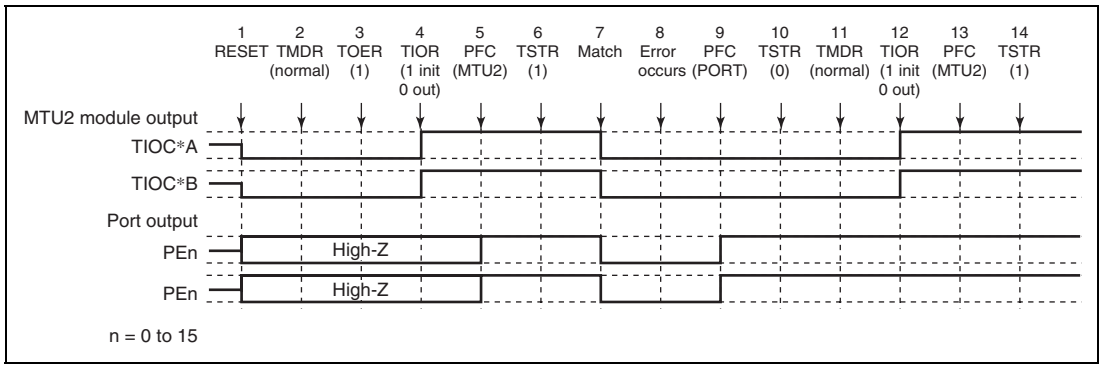

Figure 9.124 Error Occurrence in Normal Mode, Recovery in Normal Mode

1. After a reset, MTU2 output is low and ports are in the high-impedance state.
2. After a reset, the TMDR setting is for normal mode.
3. For channels 3 and 4, enable output with TOER before initializing the pins with TIOR.
4. Initialize the pins with TIOR. (The example shows initial high output, with low output on compare-match occurrence.)
5. Set MTU2 output with the PFC.
6. The count operation is started by TSTR.
7. Output goes low on compare-match occurrence.
8. An error occurs.
9. Set port output with the PFC and output the inverse of the active level.
10. The count operation is stopped by TSTR.
11. Not necessary when restarting in normal mode.
12. Initialize the pins with TIOR.
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Operation when Error Occurs during PWM Mode 1 Operation, and Operation is Restarted in Complementary PWM Mode: Figure 9.134 shows an explanatory diagram of the case where an error occurs in PWM mode 1 and operation is restarted in complementary PWM mode after re-setting.

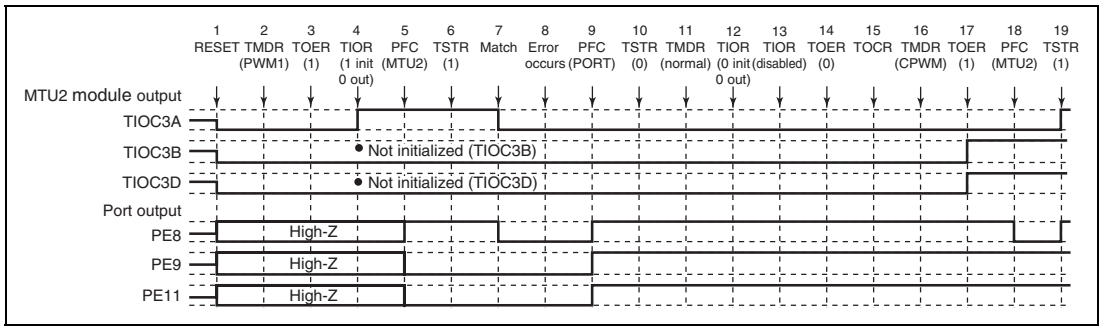

Figure 9.134 Error Occurrence in PWM Mode 1, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.130.

11. Set normal mode for initialization of the normal mode waveform generation section.
12. Initialize the PWM mode 1 waveform generation section with TIOR.
13. Disable operation of the PWM mode 1 waveform generation section with TIOR.
14. Disable channel 3 and 4 output with TOER.
15. Select the complementary PWM output level and cyclic output enabling/disabling with TOCR.
16. Set complementary PWM.
17. Enable channel 3 and 4 output with TOER.
18. Set MTU2 output with the PFC.
19. Operation is restarted by TSTR.

Operation when Error Occurs during Reset-Synchronized PWM Mode Operation, and Operation is Restarted in PWM Mode 1: Figure 9.150 shows an explanatory diagram of the case where an error occurs in reset-synchronized PWM mode and operation is restarted in PWM mode 1 after re-setting.

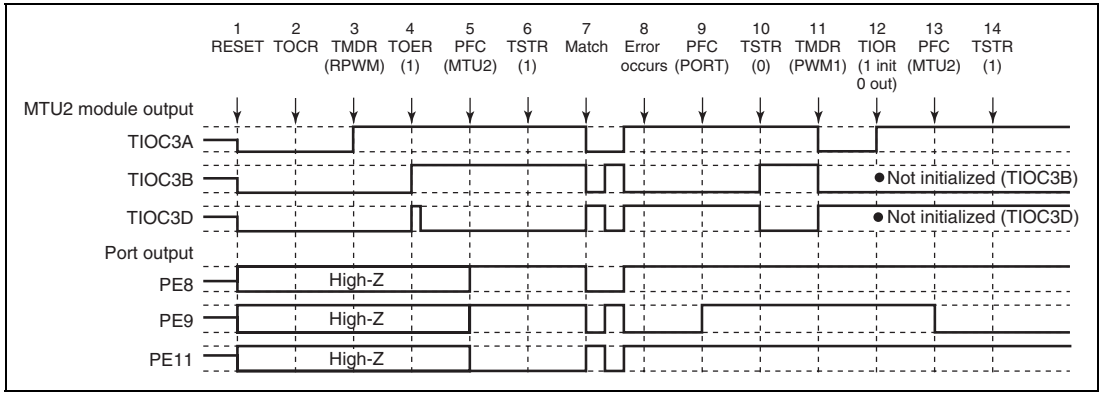

Figure 9.150 Error Occurrence in Reset-Synchronized PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.149.

11. Set PWM mode 1. (MTU2 positive phase output is low, and negative phase output is high.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

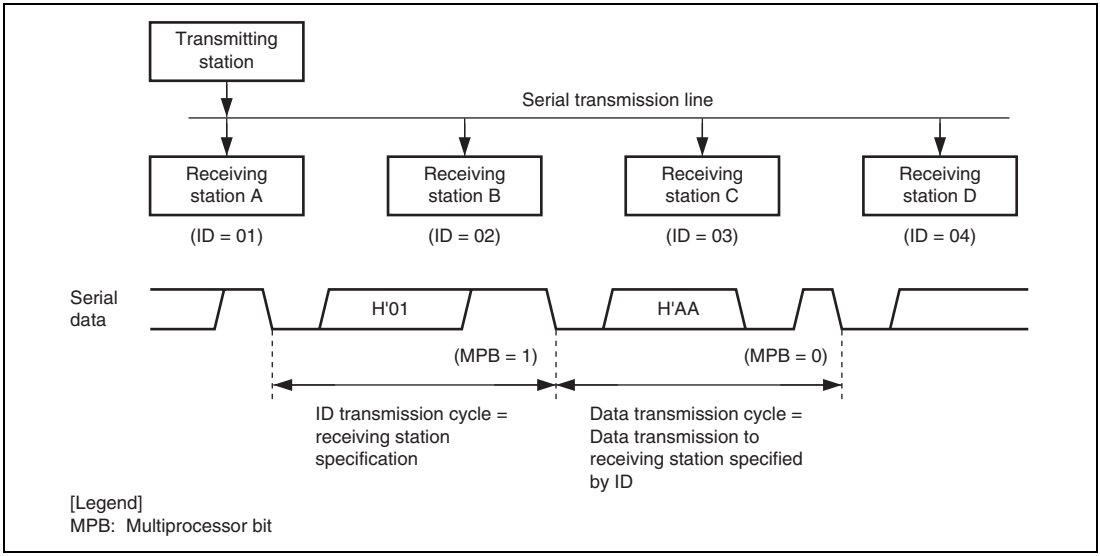

Figure 12.15 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	TRG0S[3:0]	0000	R/W	A/D Trigger 0 Select 3 to 0 Select an external trigger or MTU2 trigger to start A/D conversion for group 0 when A/D module 0 is in single mode, 4-channel scan mode, or 2-channel scan mode. 0000: External trigger pin ($\overline{\text{ADTRG}}$) input 0001: TRGA input capture/compare match for each MTU2 channel or TCNT_4 underflow (trough) in complementary PWM mode (TRGAN) 0010: MTU2 channel 0 compare match (TRG0N) 0011: MTU2 A/D conversion start request delaying (TRG4AN) 0100: MTU2 A/D conversion start request delaying (TRG4BN) 0101: Setting prohibited 0110: Setting prohibited 0111: Setting prohibited 1xxx: Setting prohibited When switching the selector, first clear the ADST bit in the A/D control register (ADCR) to 0. Specify different trigger sources for the group 0 and group 1 conversion requests so that a group 0 conversion request is not generated simultaneously with a group 1 conversion request in 2-channel scan mode.

[Legend]

x: Don't care

Table 15.3 SH7125 Pin Functions in Each Operating Mode

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
4, 22, 35	Vcc	Vcc
6, 24, 33	Vss	Vss
8, 37	VCL	VCL
61	AVcc	AVcc
52	AVss	AVss
47	PLLVss	PLLVss
42	EXTAL	EXTAL
41	XTAL	XTAL
46	MD1	MD1
45	FWE/($\overline{\text{ASEBRKAK}}$/ $\overline{\text{ASEBRK}}$*[1])	FWE
39	$\overline{\text{RES}}$	$\overline{\text{RES}}$
40	$\overline{\text{WDTOVF}}$	$\overline{\text{WDTOVF}}$
44	NMI	NMI
43	$\overline{\text{ASEMD0}}$	$\overline{\text{ASEMD0}}$
38	PA0	PA0/$\overline{\text{POE0}}$/RXD0
36	PA1	PA1/$\overline{\text{POE1}}$/TXD0
34	PA2	PA2/IRQ0/SCK0
32	PA3/($\overline{\text{TRST}}$*[1])	PA3/IRQ1/RXD1
31	PA4/(TMS*[1])	PA4/IRQ2/TXD1
30	PA5	PA5/IRQ3/SCK1
29	PA6	PA6/TCLKA
28	PA7/(TCK*[1])	PA7/TCLKB/SCK2
27	PA8/(TDI*[1])	PA8/TCLKC/RXD2
26	PA9/(TDO*[1])	PA9/TCLKD/TXD2/$\overline{\text{POE8}}$
25	PA10	PA10/RXD0
23	PA11	PA11/TXD0/$\overline{\text{ADTRG}}$
21	PA12	PA12/SCK0
20	PA13	PA13/SCK1

19.4 Sleep Mode

19.4.1 Transition to Sleep Mode

Executing the SLEEP instruction when the STBY bit in STBCR1 is 0 causes a transition from the program execution state to sleep mode. Although the CPU halts immediately after executing the SLEEP instruction, the contents of its internal registers remain unchanged. The on-chip peripheral modules continue to operate.

19.4.2 Canceling Sleep Mode

Sleep mode is canceled by a reset.

(1) Canceling with Reset

Sleep mode is canceled by a power-on reset with the $\overline{\text{RES}}$ pin, a manual reset with the $\overline{\text{MRES}}$ pin, or an internal power-on/manual reset by WDT. Do not cancel sleep mode with an interrupt.

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep	Module
TIORL_3	Initialized	Retained	Initialized	Initialized	Retained	MTU2
TIORH_4	Initialized	Retained	Initialized	Initialized	Retained	
TIORL_4	Initialized	Retained	Initialized	Initialized	Retained	
TIER_3	Initialized	Retained	Initialized	Initialized	Retained	
TIER_4	Initialized	Retained	Initialized	Initialized	Retained	
TOER	Initialized	Retained	Initialized	Initialized	Retained	
TGCR	Initialized	Retained	Initialized	Initialized	Retained	
TOCR1	Initialized	Retained	Initialized	Initialized	Retained	
TOCR2	Initialized	Retained	Initialized	Initialized	Retained	
TCNT_3	Initialized	Retained	Initialized	Initialized	Retained	
TCNT_4	Initialized	Retained	Initialized	Initialized	Retained	
TCDR	Initialized	Retained	Initialized	Initialized	Retained	
TDDR	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_3	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_3	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_4	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_4	Initialized	Retained	Initialized	Initialized	Retained	
TCNTS	Initialized	Retained	Initialized	Initialized	Retained	
TCBR	Initialized	Retained	Initialized	Initialized	Retained	
TGRC_3	Initialized	Retained	Initialized	Initialized	Retained	
TGRD_3	Initialized	Retained	Initialized	Initialized	Retained	
TGRC_4	Initialized	Retained	Initialized	Initialized	Retained	
TGRD_4	Initialized	Retained	Initialized	Initialized	Retained	
TSR_3	Initialized	Retained	Initialized	Initialized	Retained	
TSR_4	Initialized	Retained	Initialized	Initialized	Retained	
TITCR	Initialized	Retained	Initialized	Initialized	Retained	
TITCNT	Initialized	Retained	Initialized	Initialized	Retained	
TBTER	Initialized	Retained	Initialized	Initialized	Retained	
TDER	Initialized	Retained	Initialized	Initialized	Retained	
TOLBR	Initialized	Retained	Initialized	Initialized	Retained	
TBTM_3	Initialized	Retained	Initialized	Initialized	Retained	

Index