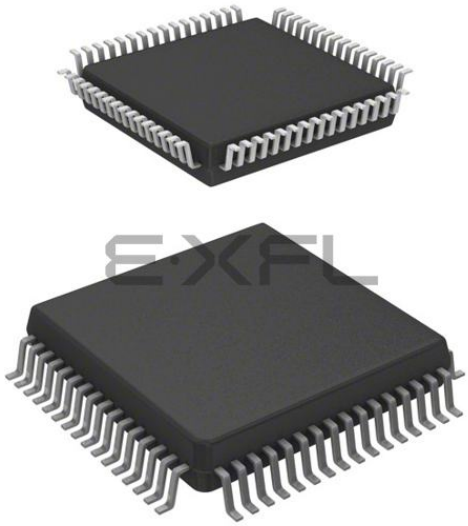

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250ad50fav

2.2.1 General Registers (Rn)

There are sixteen 32-bit general registers (Rn), designated R0 to R15. The general registers are used for data processing and address calculation. R0 is also used as an index register. With a number of instructions, R0 is the only register that can be used. R15 is used as a hardware stack pointer (SP). In exception handling, R15 is used for accessing the stack to save or restore the status register (SR) and program counter (PC) values.

2.2.2 Control Registers

There are three 32-bit control registers, designated status register (SR), global base register (GBR), and vector base register (VBR). SR indicates a processing state. GBR is used as a base address in GBR indirect addressing mode for data transfer of on-chip peripheral module registers. VBR is used as a base address of the exception handling (including interrupts) vector table.

- Status register (SR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	M	Q	I[3:0]				-	-	S	T
Initial value:	0	0	0	0	0	0	-	-	1	1	1	1	0	0	-	-
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit name	Default	Read/ Write	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	M	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instructions.
8	Q	Undefined	R/W	Used by the DIV0U, DIV0S, and DIV1 instructions.
7 to 4	I[3:0]	1111	R/W	Interrupt Mask
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Interrupt sources	7 sources	4 sources	4 sources	5 sources	5 sources	3 sources
	• Compare match or input capture 0A	• Compare match or input capture 1A*2	• Compare match or input capture 2A*2	• Compare match or input capture 3A	• Compare match or input capture 4A	• Compare match or input capture 5U
	• Compare match or input capture 0B	• Compare match or input capture 1B*2	• Compare match or input capture 2B*2	• Compare match or input capture 3B	• Compare match or input capture 4B	• Compare match or input capture 5V
	• Compare match or input capture 0C	• Overflow • Underflow	• Overflow • Underflow	• Compare match or input capture 3C	• Compare match or input capture 4C	• Compare match or input capture 5W
	• Compare match or input capture 0D			• Compare match or input capture 3D	• Compare match or input capture 4D	
	• Compare match 0E			• Overflow	• Overflow or underflow	
	• Compare match 0F					
	• Overflow					

Table 9.10 TPSC1 and TPSC0 (Channel 5)

Channel	Bit 1 TPSC1	Bit 0 TPSC0	Description
5	0	0	Internal clock: counts on MPϕ/1
		1	Internal clock: counts on MPϕ/4
	1	0	Internal clock: counts on MPϕ/16
		1	Internal clock: counts on MPϕ/64

Note: Bits 7 to 2 are reserved in channel 5. These bits are always read as 0. The write value should always be 0.

9.3.2 Timer Mode Register (TMDR)

The TMDR registers are 8-bit readable/writable registers that are used to set the operating mode of each channel. The MTU2 has five TMDR registers, one each for channels 0 to 4. TMDR register settings should be changed only when TCNT operation is stopped.

Bit:	7	6	5	4	3	2	1	0
	-	BFE	BFB	BFA	MD[3:0]			
Initial value:	0	0	0	0	0	0	0	0
R/W:	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved This bit is always read as 0. The write value should always be 0.
6	BFE	0	R/W	Buffer Operation E Specifies whether TGRE_0 and TGRF_0 are to operate in the normal way or to be used together for buffer operation. When TGRF is used as a buffer register, TGRF compare match is generated. In channels 1 to 4, this bit is reserved. It is always read as 0 and the write value should always be 0. 0: TGRE_0 and TGRF_0 operate normally 1: TGRE_0 and TGRF_0 used together for buffer operation

Bit	Bit Name	Initial Value	R/W	Description
0	OE3B	0	R/W	Master Enable TIOC3B This bit enables/disables the TIOC3B pin MTU2 output. 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled

Note: * The inactive level is determined by the settings in timer output control registers 1 and 2 (TOCR1 and TOCR2). For details, refer to section 9.3.18, Timer Output Control Register 1 (TOCR1), and section 9.3.19, Timer Output Control Register 2 (TOCR2). Set these bits to 1 to enable MTU2 output in other than complementary PWM or reset-synchronized PWM mode. When these bits are set to 0, low level is output.

9.3.18 Timer Output Control Register 1 (TOCR1)

TOCR1 is an 8-bit readable/writable register that enables/disables PWM synchronized toggle output in complementary PWM mode/reset synchronized PWM mode, and controls output level inversion of PWM output.

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Bit Name	Initial value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PSYE	0	R/W	PWM Synchronous Output Enable This bit selects the enable/disable of toggle output synchronized with the PWM period. 0: Toggle output is disabled 1: Toggle output is enabled
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial value	R/W	Description
0	OLS1P	0	R/W	Output Level Select 1P* This bit selects the output level on TIOC3B in reset-synchronized PWM mode/complementary PWM mode. See table 9.38.

Note: * Setting the TOCS bit in TOCR1 to 1 makes this bit setting valid.

Table 9.32 Setting of Bits BF1 and BF0

Bit 7	Bit 6	Description	
BF1	**BF0**	**Complementary PWM Mode**	**Reset-Synchronized PWM Mode**
0	0	Does not transfer data from the buffer register (TOLBR) to TOCR2.	Does not transfer data from the buffer register (TOLBR) to TOCR2.
0	1	Transfers data from the buffer register (TOLBR) to TOCR2 at the crest of the TCNT_4 count.	Transfers data from the buffer register (TOLBR) to TOCR2 when TCNT_3/TCNT_4 is cleared
1	0	Transfers data from the buffer register (TOLBR) to TOCR2 at the trough of the TCNT_4 count.	Setting prohibited
1	1	Transfers data from the buffer register (TOLBR) to TOCR2 at the crest and trough of the TCNT_4 count.	Setting prohibited

Table 9.33 TIOC4D Output Level Select Function

Bit 5	Function			
			Compare Match Output	
OLS3N	**Initial Output**	**Active Level**	**Up Count**	**Down Count**
0	High level	Low level	High level	Low level
1	Low level	High level	Low level	High level

Note: The reverse phase waveform initial output value changes to the active level after elapse of the dead time after count start.

Table 9.46 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Registers**	**PWM Mode 1**	**PWM Mode 2**
0	TGRA_0	TIOC0A	TIOC0A
	TGRB_0		TIOC0B
	TGRC_0	TIOC0C	TIOC0C
	TGRD_0		TIOC0D
1	TGRA_1	TIOC1A*	TIOC1A*
	TGRB_1		TIOC1B*
2	TGRA_2	TIOC2A*	TIOC2A*
	TGRB_2		TIOC2B*
3	TGRA_3	TIOC3A	Cannot be set
	TGRB_3		Cannot be set
	TGRC_3	TIOC3C	Cannot be set
	TGRD_3		Cannot be set
4	TGRA_4	TIOC4A	Cannot be set
	TGRB_4		Cannot be set
	TGRC_4	TIOC4C	Cannot be set
	TGRD_4		Cannot be set

Notes: In PWM mode 2, PWM output is not possible for the TGR register in which the period is set.

* Supported only by the SH7125.

Figure 9.28 shows examples of PWM waveform output with 0% duty and 100% duty in PWM mode.

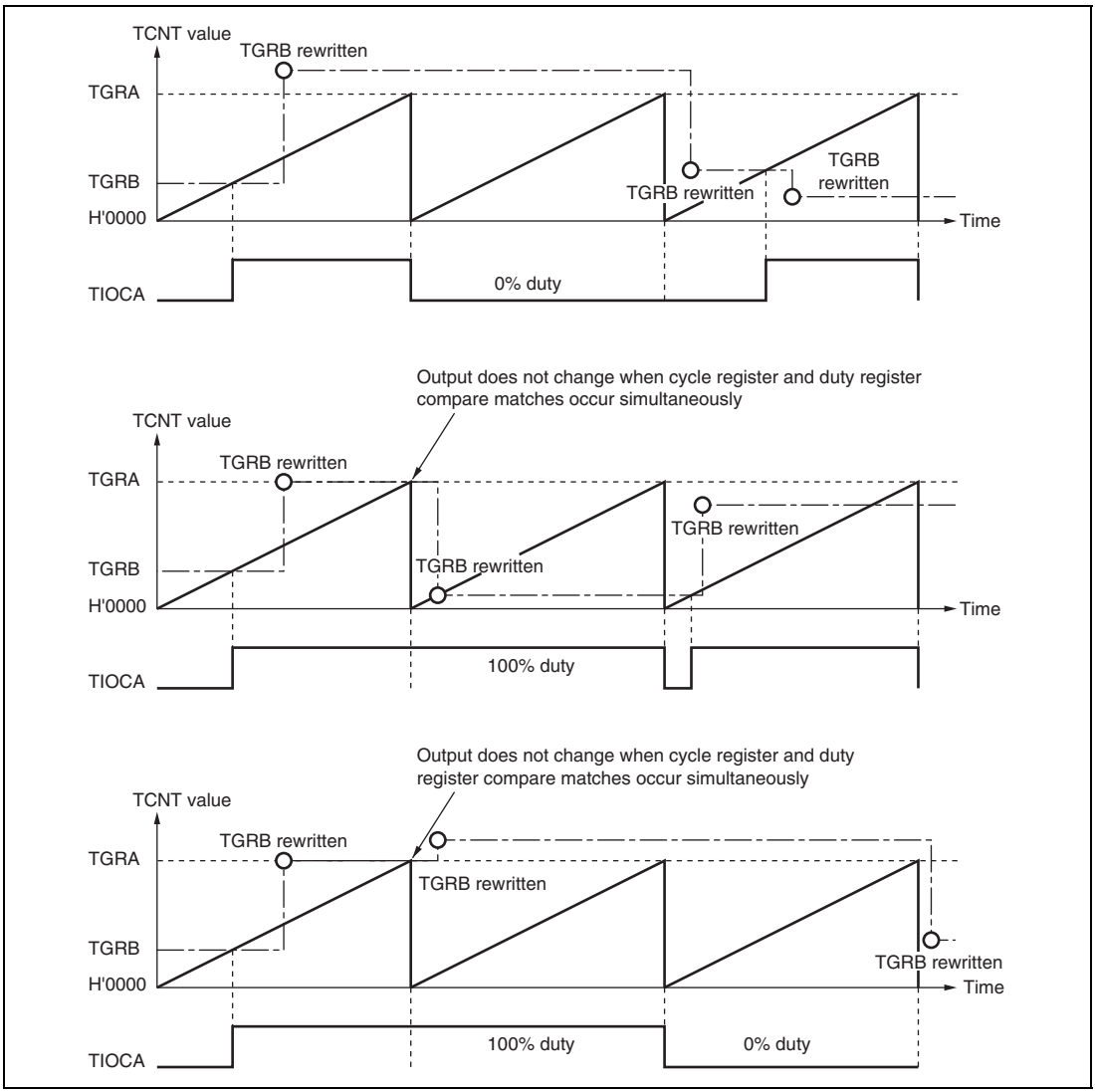


Figure 9.28 Example of PWM Mode Operation (3)

9.7.11 Contention between Buffer Register Write and Input Capture

If an input capture signal is generated in the T2 state of a buffer register write cycle, the buffer operation takes precedence and the write to the buffer register is not performed.

Figure 9.117 shows the timing in this case.

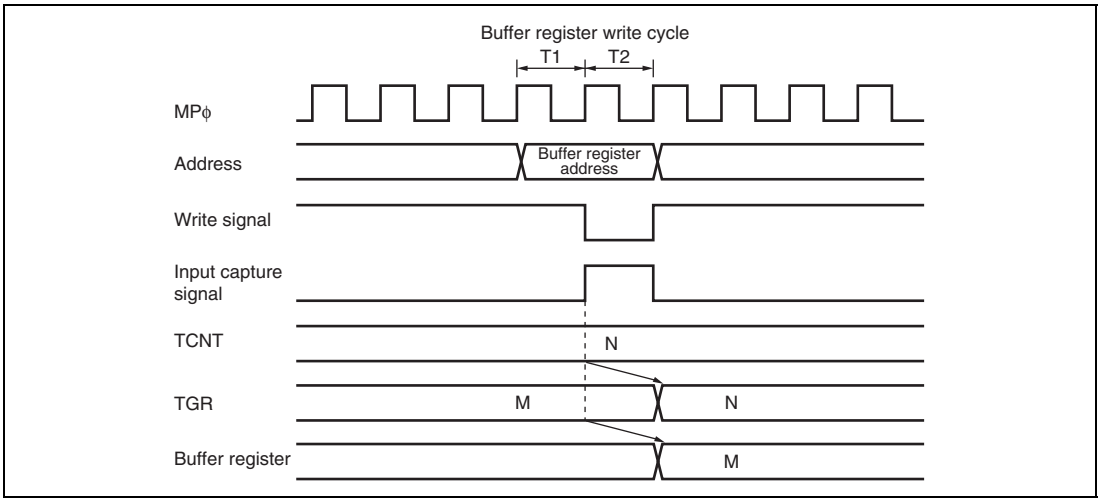


Figure 9.117 Contention between Buffer Register Write and Input Capture

9.7.12 TCNT_2 Write and Overflow/Underflow Contention in Cascade Connection

With timer counters TCNT_1 and TCNT_2 in a cascade connection, when a contention occurs during TCNT_1 count (during a TCNT_2 overflow/underflow) in the T2 state of the TCNT_2 write cycle, the write to TCNT_2 is conducted, and the TCNT_1 count signal is disabled. At this point, if there is match with TGRA_1 and the TCNT_1 value, a compare signal is issued. Furthermore, when the TCNT_1 count clock is selected as the input capture source of channel 0, TGRA_0 to TGRD_0 carry out the input capture operation. In addition, when the compare match/input capture is selected as the input capture source of TGRB_1, TGRB_1 carries out input capture operation. The timing is shown in figure 9.118.

For cascade connections, be sure to synchronize settings for channels 1 and 2 when setting TCNT clearing.

12.4.4 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer to be performed among a number of processors sharing communication lines by means of asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is carried out, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles: an ID transmission cycle that specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle, and if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 12.15 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. The receiving station skips data until data with a 1 multiprocessor bit is sent. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose ID does not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCSCR to implement this function. When the MPIE bit is set to 1, transfer of receive data from SCRSR to SCRDR, error flag detection, and setting the SCSSR status flags, RDRF, FER, and OER to 1 are inhibited until data with a 1 multiprocessor bit is received. On reception of receive character with a 1 multiprocessor bit, the MPB bit in SCSSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCSCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

13.4.5 A/D Converter Activation by MTU2

The A/D converter can be independently activated by an A/D conversion request from the interval timer of the MTU2.

To activate the A/D converter by the MTU2, first set the TRGE bit in the A/D control/status register (ADCSR) to 1, and then set the A/D trigger select register (ADTSR). After this register setting has been made, the ADST bit in ADCR is automatically set to 1 when an A/D conversion request from the interval timer of the MTU2 occurs. The timing from setting of the ADST bit until the start of A/D conversion is the same as when 1 is written to the ADST bit by software.

13.4.6 External Trigger Input Timing

A/D conversion can be externally triggered. When the TRGE bit in the A/D control/status register (ADCSR) is set to 1 while the TRGS3 to TRGS0 bits in the A/D trigger select register_0 (ADTSR_0) is set to external trigger input, external trigger input is enabled at the $\overline{\text{ADTRG}}$ pin. A falling edge of the $\overline{\text{ADTRG}}$ pin sets the ADST bit to 1 in ADCR, starting A/D conversion. Other operations, in both single and scan modes, are the same as when the ADST bit has been set to 1 by software. Figure 13.3 shows the timing.

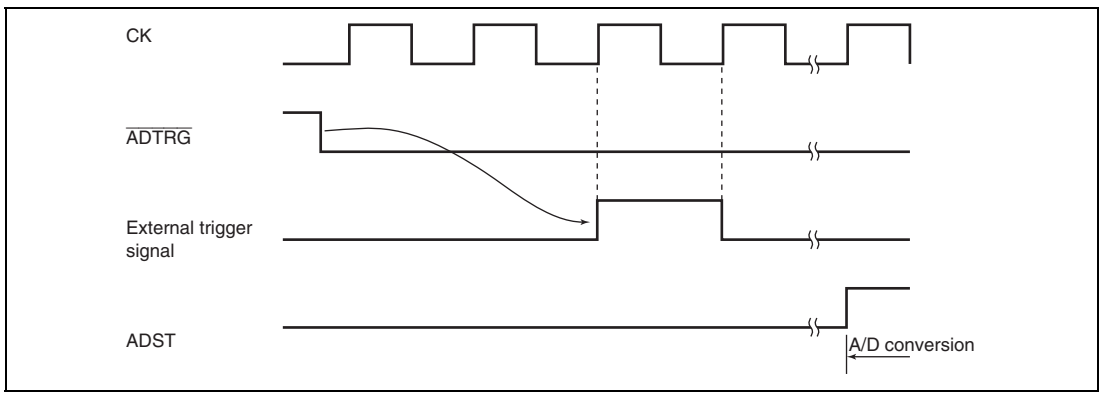


Figure 13.3 External Trigger Input Timing

14.5 Usage Notes

14.5.1 Module Standby Mode Setting

The CMT operation can be disabled or enabled using the standby control register. The initial setting is for CMT operation to be halted. Access to a register is enabled by clearing module standby mode. For details, refer to section 19, Power-Down Modes.

14.5.2 Conflict between Write and Compare-Match Processes of CMCNT

When the compare match signal is generated in the T2 cycle while writing to CMCNT, clearing CMCNT has priority over writing to it. In this case, CMCNT is not written to. Figure 14.5 shows the timing to clear the CMCNT counter.

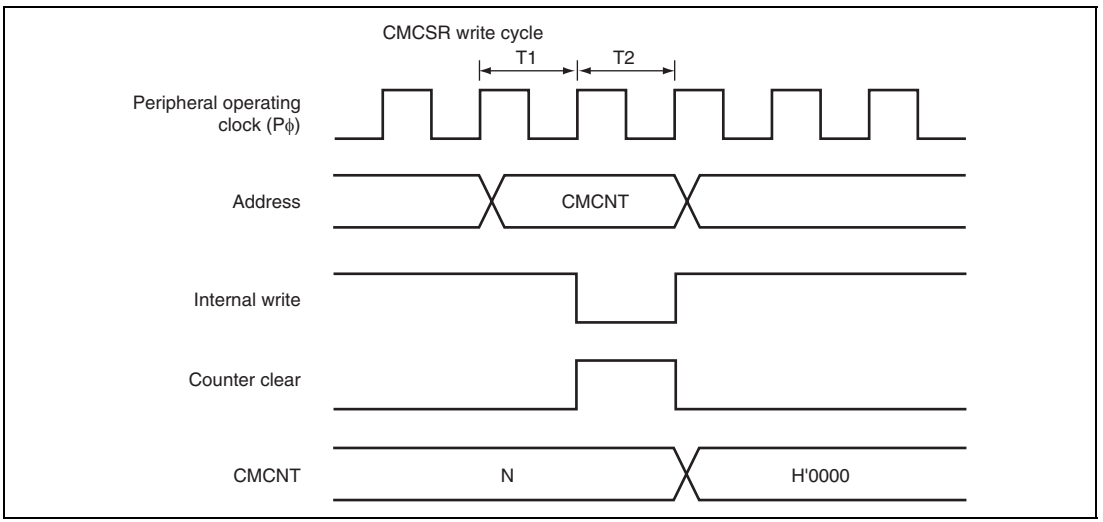


Figure 14.5 Conflict between Write and Compare-Match Processes of CMCNT

Bit	Bit Name	Initial Value	R/W	Description
6	PA9MD2	0	R/W	PA9 Mode
5	PA9MD1	0	R/W	Select the function of the PA9/TCLKD/TXD2/TDO/$\overline{\text{POE8}}$ pin.
4	PA9MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDO output. 000: PA9 I/O (port) 001: TCLKD input (MTU2) 110: TXD2 output (SCI) 111: $\overline{\text{POE8}}$ input (POE) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PA8MD2	0	R/W	PA8 Mode
1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RXD2/TDI pin.
0	PA8MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.

16.3.1 Register Descriptions

Port E is a 16-bit input/output port in the SH7125 and a 12-bit input/output port in the SH7124. Port E has the following registers. For details on register addresses and register states during each processing, refer to section 20, List of Registers.

Table 16.5 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port E data register L	PEDRL	R/W	H'0000	H'FFFFD302	8, 16
Port E port register L	PEPRL	R	—	H'FFFFD31E	8, 16

16.3.2 Port E Data Register L (PEDRL)

PEDRL is a 16-bit readable/writable register that stores port E data. Bits PE15DR to PE0DR correspond to pins PE15 to PE0 (multiplexed functions omitted here) in the SH7125. Bits PE15DR to PE8DR and PE3DR to PE0DR correspond to pins PE15 to PE8 and PE3 to PE0, respectively (multiplexed functions omitted here) in the SH7124.

When a pin function is general output, if a value is written to PEDRL, that value is output directly from the pin, and if PEDRL is read, the register value is returned directly regardless of the pin state.

When a pin function is general input, if PEDRL is read, the pin state, not the register value, is returned directly. If a value is written to PEDRL, although that value is written into PEDRL, it does not affect the pin state. Table 16.6 summarizes port E data register read/write operations.

17.2.3 Mode Comparison

The comparison table of programming and erasing related items about boot mode and user program mode is shown in table 17.2.

Table 17.2 Comparison of Programming Modes

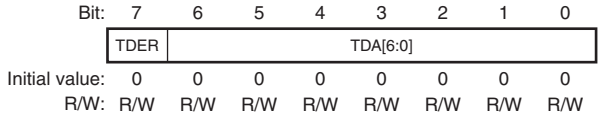
Programming/erasing environment	On-Board Programming		Off-Board Programming
	Boot Mode	User Program Mode*2	
Programming/ erasing enable MAT	User MAT	User MAT	User MAT
Programming/ erasing control	Command method	Programming/erasing interface	—
All erasure	Possible (Automatic)	Possible	Possible (Automatic)
Block division erasure	Possible*1	Possible	Impossible
Program data transfer	From host via SCI	From optional device via RAM	Via programmer
User branch function	Not possible	Possible	Impossible
Reset initiation MAT	Embedded program storage MAT	User MAT	Embedded program storage MAT
Transition to user mode	Mode setting change and reset	FWE setting change	—

Notes: 1. All-erasure is performed. After that, the specified block can be erased.
2. Cannot be used in 32-kbyte on-chip flash memory version.

- The user MAT is all erased in boot mode. Then, the user MAT can be programmed by means of the command method. However, the contents of the MAT cannot be read until this state.

(5) Flash Transfer Destination Address Register (FTDAR)

FTDAR specifies the on-chip RAM address to which the on-chip program is downloaded. Make settings for FTDAR before writing 1 to the SCO bit in FCCS. The initial value is H'00.



Bit	Bit Name	Initial Value	R/W	Description
7	TDER	0	R/W	Transfer Destination Address Setting Error This bit is set to 1 when there is an error in the download start address set by bits 6 to 0 (TDA6 to TDA0). Whether the address setting is erroneous or not is tested by checking whether the setting of TDA6 to TDA0 is between the range of H'02 to H'04 after setting the SCO bit in FCCS to 1 and performing download. Before setting the SCO bit to 1 be sure to set the FTDAR value between H'02 to H'04 as well as clearing this bit to 0. 0: Setting of TDA6 to TDA0 is normal 1: Setting of TDER and TDA6 to TDA0 is H'00 to H'01 and H'05 to H'FF and download has been aborted

17.6.2 Software Protection

Software protection is set up in any of two ways: by disabling the downloading of on-chip programs for programming and erasing and by means of a key code.

Table 17.9 Software Protection

		Function to be Protected	
Item	**Description**	**Download**	**Programming/ Erasure**
Protection by the SCO bit	Clearing the SCO bit in FCCS disables downloading of the programming/erasing program, thus making the LSI enter a programming/erasing-protected state.	√	√
Protection by FKEY	Downloading and programming/erasing are disabled unless the required key code is written in FKEY. Different key codes are used for downloading and for programming/erasing.	√	√

17.6.3 Error Protection

Error protection is a mechanism for aborting programming or erasure when an error occurs, in the form of the microcomputer getting out of control during programming/erasing of the flash memory or operations that are not in accordance with the established procedures for programming/erasing. Aborting programming or erasure in such cases prevents damage to the flash memory due to excessive programming or erasing.

If the microcomputer malfunctions during programming/erasing of the flash memory, the FLER bit in FCCS is set to 1 and the LSI enters the error protection state, thus aborting programming or erasure.

The FLER bit is set to 1 in the following conditions:

- When the relevant bank area of flash memory is read during programming/erasing (including a vector read or an instruction fetch)
- When a SLEEP instruction (including software standby mode) is executed during programming/erasing

Error protection is cancelled (FLER bit is cleared) only by a power-on reset.

Note that the reset signal should only be released after providing a reset input over a period longer than the normal 100 µs. Since high voltages are applied during programming/erasing of the flash memory, some voltage may still remain even after the error protection state has been entered. For this reason, it is necessary to reduce the risk of damage to the flash memory by extending the reset period so that the charge is released.

The state-transition diagram in figure 17.13 shows transitions to and from the error protection state.

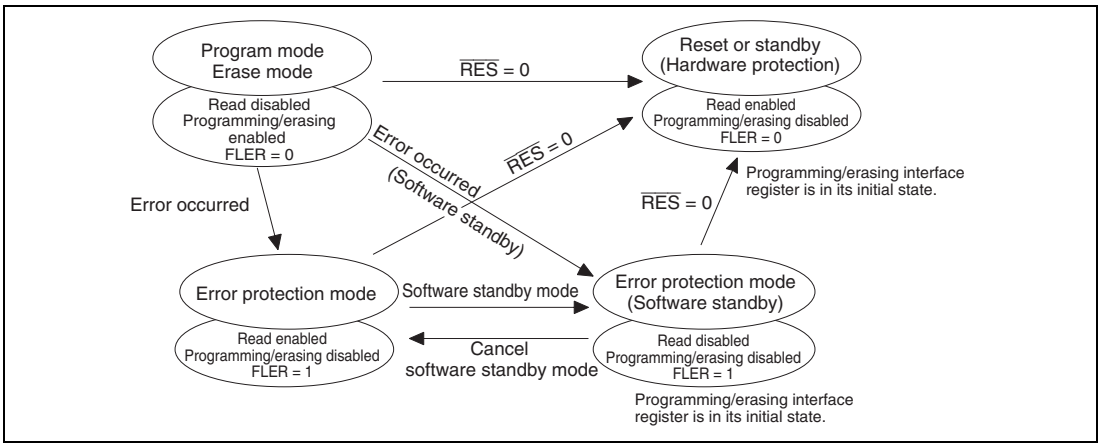


Figure 17.13 Transitions to and from Error Protection State

19.3.3 Standby Control Register 3 (STBCR3)

STBCR3 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	-	-	MSTP13	MSTP12	MSTP11	-	-	-
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.
5	MSTP13	1	R/W	Module Stop Bit 13 When this bit is set to 1, the supply of the clock to the SCI_2 is halted. 0: SCI_2 operates 1: Clock supply to SCI_2 halted
4	MSTP12	1	R/W	Module Stop Bit 12 When this bit is set to 1, the supply of the clock to the SCI_1 is halted. 0: SCI_1 operates 1: Clock supply to SCI_1 halted
3	MSTP11	1	R/W	Module Stop Bit 11 When this bit is set to 1, the supply of the clock to the SCI_0 is halted. 0: SCI_0 operates 1: Clock supply to SCI_0 halted
2 to 0	—	All 1	R/W	Reserved These bits are always read as 1. The write value should always be 1.

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size	Number of Access States
Interrupt priority register D	IPRD	16	H'FFFFE982	INTC	16	Pϕ reference
Interrupt priority register E	IPRE	16	H'FFFFE984		16	B: 2, W: 2
Interrupt priority register F	IPRF	16	H'FFFFE986		16	
Interrupt priority register H	IPRH	16	H'FFFFE98A		16	
Interrupt priority register I	IPRI	16	H'FFFFE98C		16	
Interrupt priority register J	IPRJ	16	H'FFFFE98E		16	
Interrupt priority register K	IPRK	16	H'FFFFE990		16	
Interrupt priority register L	IPRL	16	H'FFFFE992		16	
Interrupt priority register M	IPRM	16	H'FFFFE994		16	
Break address register A*	BARA	32	H'FFFFF300	UBC	32	Bϕ reference
Break address mask register A*	BAMRA	32	H'FFFFF304		32	B: 2, W: 2, L: 2
Break bus cycle register A*	BBRA	16	H'FFFFF308		16	
Break data register A*	BDRA	32	H'FFFFF310		32	
Break data mask register A*	BDMRA	32	H'FFFFF314		32	
Break address register B*	BARB	32	H'FFFFF320		32	
Break address mask register B*	BAMRB	32	H'FFFFF324		32	
Break bus cycle register B*	BBRB	16	H'FFFFF328		16	
Break data register B*	BDRB	32	H'FFFFF330		32	
Break data mask register B*	BDMRB	32	H'FFFFF334		32	
Break control register*	BRCR	32	H'FFFFF3C0		32	
Branch source register*	BRSR	32	H'FFFFF3D0		32	
Branch destination register*	BRDR	32	H'FFFFF3D4		32	
Execution times break register*	BETR	16	H'FFFFF3DC		16	

Note: * The UBC registers are not supported on 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versions (SH71250A, SH71240A).

Item	Page	Revision (See Manual for Details)
15.1.2 Port A Control Registers L1 to L4 (PACRL1 to PACRL4) • Port A Control Register L1 (PACRL1)	529	Table amended

Bit	Bit Name	Initial Value	R/W	Description
14	PA3MD2	0	R/W	PA3 Mode
13	PA3MD1	0	R/W	Select the function of the PA3/IRQ1/RXD1/$\overline{\text{TRST}}$ pin.
12	PA3MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to $\overline{\text{TRST}}$ input. 000: PA3 I/O (port) 001: RXD1 input (SCI) 111: IRQ1 input (INTC) Other than above: Setting prohibited

	530	Note added Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.
• Port A Control Register L3 (PACRL3)	531	Table amended

Bit	Bit Name	Initial Value	R/W	Description
6	PA9MD2	0	R/W	PA9 Mode
5	PA9MD1	0	R/W	Select the function of the
4	PA9MD0	0	R/W	PA9/TCLKD/TXD2/TDO/$\overline{\text{POE8}}$ pin. When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDO output. 000: PA9 I/O (port) 001: TCLKD input (MTU2) 110: TXD2 output (SCI) 111: $\overline{\text{POE8}}$ input (POE) Other than above: Setting prohibited

	532	Table amended

Bit	Bit Name	Initial Value	R/W	Description
2	PA8MD2	0	R/W	PA8 Mode
1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RXD2/TDI pin.
0	PA8MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited

Note added

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.