Renesas Electronics America Inc - DF71250AD50FPV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250ad50fpv

Type	Kinds of Instruction	Op Code	Function	Number of Instructions
Arithmetic operation instructions	21	MULS	Signed multiplication	33
		MULU	Unsigned multiplication	
		NEG	Sign inversion	
		NEGC	Sign inversion with borrow	
		SUB	Binary subtraction	
		SUBC	Binary subtraction with carry	
		SUBV	Binary subtraction with underflow	
Logic operation instructions	6	AND	Logical AND	14
		NOT	Bit inversion	
		OR	Logical OR	
		TAS	Memory test and bit setting	
		TST	T bit setting for logical AND	
		XOR	Exclusive logical OR	
Shift instructions	10	ROTL	1-bit left shift	14
		ROTR	1-bit right shift	
		ROTCL	1-bit left shift with T bit	
		ROTCR	1-bit right shift with T bit	
		SHAL	Arithmetic 1-bit left shift	
		SHAR	Arithmetic 1-bit right shift	
		SHLL	Logical 1-bit left shift	
		SHLLn	Logical n-bit left shift	
		SHLR	Logical 1-bit right shift	
		SHLRn	Logical n-bit right shift	

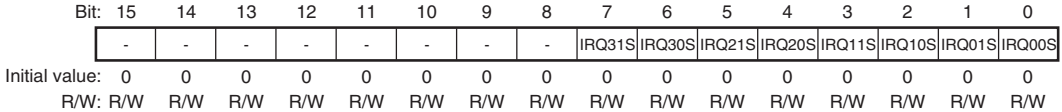
2.5.5 Shift Instructions

Table 2.14 Shift Instructions

Instruction		Operation	Code	Execution Cycles	T Bit
ROTL	Rn	T ← Rn ← MSB	0100nnnn00000100	1	MSB
ROTR	Rn	LSB → Rn → T	0100nnnn00000101	1	LSB
ROTCL	Rn	T ← Rn ← T	0100nnnn00100100	1	MSB
ROTCR	Rn	T → Rn → T	0100nnnn00100101	1	LSB
SHAL	Rn	T ← Rn ← 0	0100nnnn00100000	1	MSB
SHAR	Rn	MSB → Rn → T	0100nnnn00100001	1	LSB
SHLL	Rn	T ← Rn ← 0	0100nnnn00000000	1	MSB
SHLR	Rn	0 → Rn → T	0100nnnn00000001	1	LSB
SHLL2	Rn	Rn << 2 → Rn	0100nnnn00001000	1	—
SHLR2	Rn	Rn >> 2 → Rn	0100nnnn00001001	1	—
SHLL8	Rn	Rn << 8 → Rn	0100nnnn00011000	1	—
SHLR8	Rn	Rn >> 8 → Rn	0100nnnn00011001	1	—
SHLL16	Rn	Rn << 16 → Rn	0100nnnn00101000	1	—
SHLR16	Rn	Rn >> 16 → Rn	0100nnnn00101001	1	—

6.3.2 IRQ Control Register (IRQCR)

IRQCR is a 16-bit register that sets the input signal detection mode of the external interrupt input pins IRQ0 to IRQ3.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	IRQ31S	IRQ30S	IRQ21S	IRQ20S	IRQ11S	IRQ10S	IRQ01S	IRQ00S
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R/W	Reserved These bits are always read as 0. The write value should always be 0.
7	IRQ31S	0	R/W	IRQ3 Sense Select
6	IRQ30S	0	R/W	Set the interrupt request detection mode for pin IRQ3. 00: Interrupt request is detected at the low level of pin IRQ3 01: Interrupt request is detected at the falling edge of pin IRQ3 10: Interrupt request is detected at the rising edge of pin IRQ3 11: Interrupt request is detected at both the falling and rising edges of pin IRQ3
5	IRQ21S	0	R/W	IRQ2 Sense Select
4	IRQ20S	0	R/W	Set the interrupt request detection mode for pin IRQ2. 00: Interrupt request is detected at the low level of pin IRQ2 01: Interrupt request is detected at the falling edge of pin IRQ2 10: Interrupt request is detected at the rising edge of pin IRQ2 11: Interrupt request is detected at both the falling and rising edges of pin IRQ2

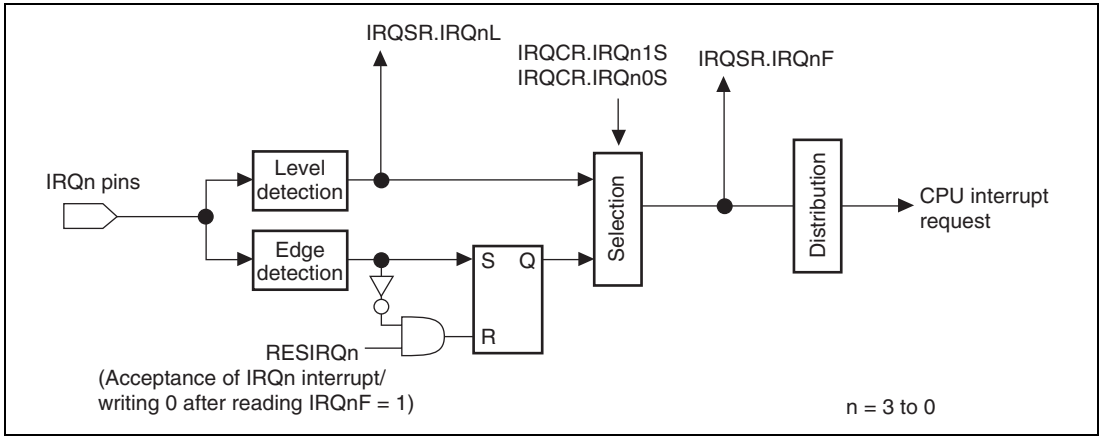


Figure 6.2 Block Diagram of IRQ3 to IRQ0 Interrupts Control

6.4.2 On-Chip Peripheral Module Interrupts

On-chip peripheral module interrupts are interrupts generated by the following on-chip peripheral modules.

Since a different interrupt vector is allocated to each interrupt source, the exception handling routine does not have to decide which interrupt has occurred. Priority levels between 0 and 15 can be allocated to individual on-chip peripheral modules in interrupt priority registers C to F and H to M (IPRC to IPRF and IPRH to IPRM). On-chip peripheral module interrupt exception handling sets the interrupt mask level bits (I3 to I0) in the status register (SR) to the priority level value of the on-chip peripheral module interrupt that was accepted.

6.4.3 User Break Interrupt*

A user break interrupt has a priority level of 15, and occurs when the break condition set in the user break controller (UBC) is satisfied. User break interrupt requests are detected by edge and are held until accepted. User break interrupt exception handling sets the interrupt mask level bits (I3 to I0) in the status register (SR) to level 15. For more details on the user break interrupt, see section 7, User Break Controller (UBC).

Note: * The user break interrupt is not generated on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.

Table 6.3 Interrupt Exception Handling Vectors and Priorities

Interrupt Source	Name	Vector No.	Vector Table Starting Address	IPR	Default Priority
User break		12	H'00000030	—	High
External pin	NMI	11	H'0000002C	—	
	IRQ0 (only SH7125)	64	H'00000100	IPRA15 to IPRA12	
	IRQ1	65	H'00000104	IPRA11 to IPRA8	
	IRQ2	66	H'00000108	IPRA7 to IPRA4	
	IRQ3	67	H'0000010C	IPRA3 to IPRA0	
MTU2_0	TGIA_0	88	H'00000160	IPRD15 to IPRD12	
	TGIB_0	89	H'00000164		
	TGIC_0	90	H'00000168		
	TGID_0	91	H'0000016C		
	TCIV_0	92	H'00000170	IPRD11 to IPRD8	
	TGIE_0	93	H'00000174		
	TGIF_0	94	H'00000178		
MTU2_1	TGIA_1	96	H'00000180	IPRD7 to IPRD4	
	TGIB_1	97	H'00000184		
	TCIV_1	100	H'00000190	IPRD3 to IPRD0	
	TCIU_1	101	H'00000194		
MTU2_2	TGIA_2	104	H'000001A0	IPRE15 to IPRE12	
	TGIB_2	105	H'000001A4		
	TCIV_2	108	H'000001B0	IPRE11 to IPRE8	
	TCIU_2	109	H'000001B4		
MTU2_3	TGIA_3	112	H'000001C0	IPRE7 to IPRE4	
	TGIB_3	113	H'000001C4		
	TGIC_3	114	H'000001C8		
	TGID_3	115	H'000001CC		
	TCIV_3	116	H'000001D0	IPRE3 to IPRE0	Low

7.3 Operation

7.3.1 Flow of the User Break Operation

The flow from setting of break conditions to user break exception processing is described below:

1. The break addresses are set in the break address registers (BARA or BARB). The masked addresses are set in the break address mask registers (BAMRA or BAMRB). The break data is set in the break data register (BDRA or BDRB). The masked data is set in the break data mask register (BDMRA or BDMRB). The bus break conditions are set in the break bus cycle registers (BBRA or BBRB). Three groups of BBRA or BBRB (L bus cycle/I bus cycle select, instruction fetch/data access select, and read/write select) are each set. No user break will be generated if even one of these groups is set with B'00. The respective conditions are set in the bits of the break control register (BRCR). Make sure to set all registers related to breaks before setting BBRA or BBRB.
2. When the break conditions are satisfied, the UBC sends a user break interrupt request to the CPU and sets the L bus condition match flag (SCMFCA or SCMFCB) and the I bus condition match flag (SCMFDA or SCMFDB) for the appropriate channel.
3. The appropriate condition match flags (SCMFCA, SCMFDA, SCMFCB, and SCMFDB) can be used to check if the set conditions match or not. The matching of the conditions sets flags, but they are not reset. Before using them again, 0 must first be written to them and then reset flags.
4. There may be an occasion when a break condition match occurs both in channels A and B around the same time. In this case, the flags for both conditions matches will be set even though only one user-break interrupt request is issued to the CPU.
5. When selecting the I bus as the break condition, note the following:
   — The CPU is connected to the I bus. The UBC monitors bus cycles generated by all bus masters that are selected by the CPA2 to CPA0 bits in BBRA or the CPB2 to CPB0 bits in BBRB, and compares the condition match.
   — I bus cycles (including read fill cycles) resulting from instruction fetches on the L bus by the CPU are defined as instruction fetch cycles on the I bus, while other bus cycles are defined as data access cycles.
   — If a break condition is specified for the I bus, even when the condition matches in an I bus cycle resulting from an instruction executed by the CPU, at which instruction the user-break is to be accepted cannot be clearly defined.

9.2 Input/Output Pins

Table 9.2 Pin Configuration

Channel	Pin Name	I/O	Function
Common	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOC1A*	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOC1B*	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOC2A*	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOC2B*	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM output pin
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM output pin
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM output pin
5	TIC5U	Input	TGRU_5 input capture input/external pulse input pin
	TIC5V	Input	TGRV_5 input capture input/external pulse input pin
	TIC5W	Input	TGRW_5 input capture input/external pulse input pin

Note: * Supported only by the SH7125.

Table 9.45 shows the TICCR setting and input capture input pins.

Table 9.45 TICCR Setting and Input Capture Input Pins

Target Input Capture	TICCR Setting	Input Capture Input Pins
Input capture from TCNT_1 to TGRA_1	I2AE bit = 0 (initial value)	TIOC1A
	I2AE bit = 1	TIOC1A, TIOC2A
Input capture from TCNT_1 to TGRB_1	I2BE bit = 0 (initial value)	TIOC1B
	I2BE bit = 1	TIOC1B, TIOC2B
Input capture from TCNT_2 to TGRA_2	I1AE bit = 0 (initial value)	TIOC2A
	I1AE bit = 1	TIOC2A, TIOC1A
Input capture from TCNT_2 to TGRB_2	I1BE bit = 0 (initial value)	TIOC2B
	I1BE bit = 1	TIOC2B, TIOC1B

Example of Cascaded Operation Setting Procedure: Figure 9.20 shows an example of the setting procedure for cascaded operation.

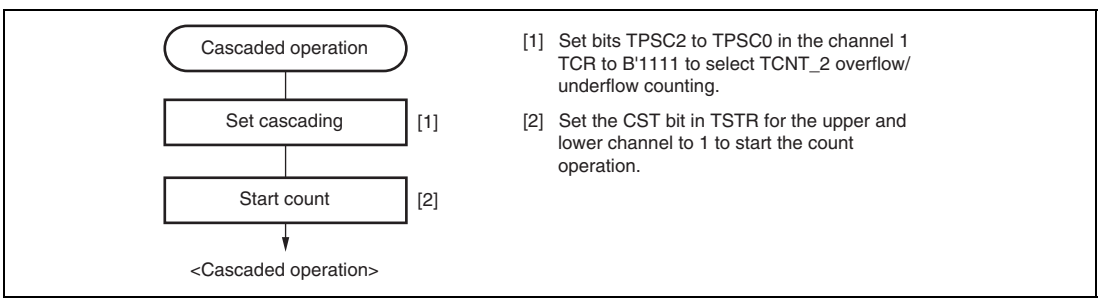
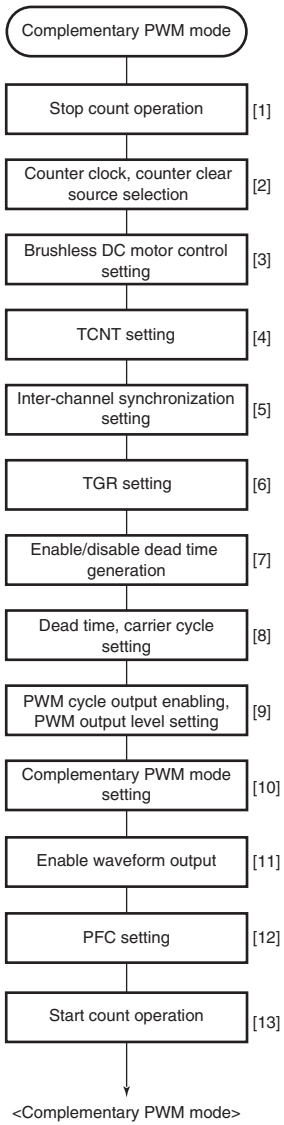


Figure 9.20 Cascaded Operation Setting Procedure

Cascaded Operation Example (a): Figure 9.21 illustrates the operation when TCNT_2 overflow/underflow counting has been set for TCNT_1 and phase counting mode has been designated for channel 2.

TCNT_1 is incremented by TCNT_2 overflow and decremented by TCNT_2 underflow.

Example of Complementary PWM Mode Setting Procedure: An example of the complementary PWM mode setting procedure is shown in figure 9.38.



[1] Clear bits CST3 and CST4 in the timer start register (TSTR) to 0, and halt timer counter (TCNT) operation. Perform complementary PWM mode setting when TCNT_3 and TCNT_4 are stopped.

[2] Set the same counter clock and clock edge for channels 3 and 4 with bits TPSC2 to TPSC0 and bits CKEG1 and CKEG0 in the timer control register (TCR). Use bits CCLR2 to CCLR0 to set synchronous clearing only when restarting by a synchronous clear from another channel during complementary PWM mode operation.

[3] When performing brushless DC motor control, set bit BDC in the timer gate control register (TGCR) and set the feedback signal input source and output chopping or gate signal direct output.

[4] Set the dead time in TCNT_3. Set TCNT_4 to H'0000.

[5] Set only when restarting by a synchronous clear from another channel during complementary PWM mode operation. In this case, synchronize the channel generating the synchronous clear with channels 3 and 4 using the timer synchro register (TSYR).

[6] Set the output PWM duty in the duty registers (TGRB_3, TGRA_4, TGRB_4) and buffer registers (TGRD_3, TGRC_4, TGRD_4). Set the same initial value in each corresponding TGR.

[7] This setting is necessary only when no dead time should be generated. Make appropriate settings in the timer dead time enable register (TDER) so that no dead time is generated.

[8] Set the dead time in the dead time register (TDDR), 1/2 the carrier cycle in the carrier cycle data register (TCDR) and carrier cycle buffer register (TCBR), and 1/2 the carrier cycle plus the dead time in TGRA_3 and TGRC_3. When no dead time generation is selected, set 1 in TDDR and 1/2 the carrier cycle + 1 in TGRA_3 and TGRC_3.

[9] Select enabling/disabling of toggle output synchronized with the PWM cycle using bit PSYE in the timer output control register 1 (TOCR1), and set the PWM output level with bits OLSP and OLSN. When specifying the PWM output level by using TOLBR as a buffer for TOCR_2, see figure 9.3.

[10] Select complementary PWM mode in timer mode register 3 (TMDR_3). Do not set in TMDR_4.

[11] Set enabling/disabling of PWM waveform output pin output in the timer output master enable register (TOER).

[12] Set the port control register and the port I/O register.

[13] Set bits CST3 and CST4 in TSTR to 1 simultaneously to start the count operation.

Figure 9.38 Example of Complementary PWM Mode Setting Procedure

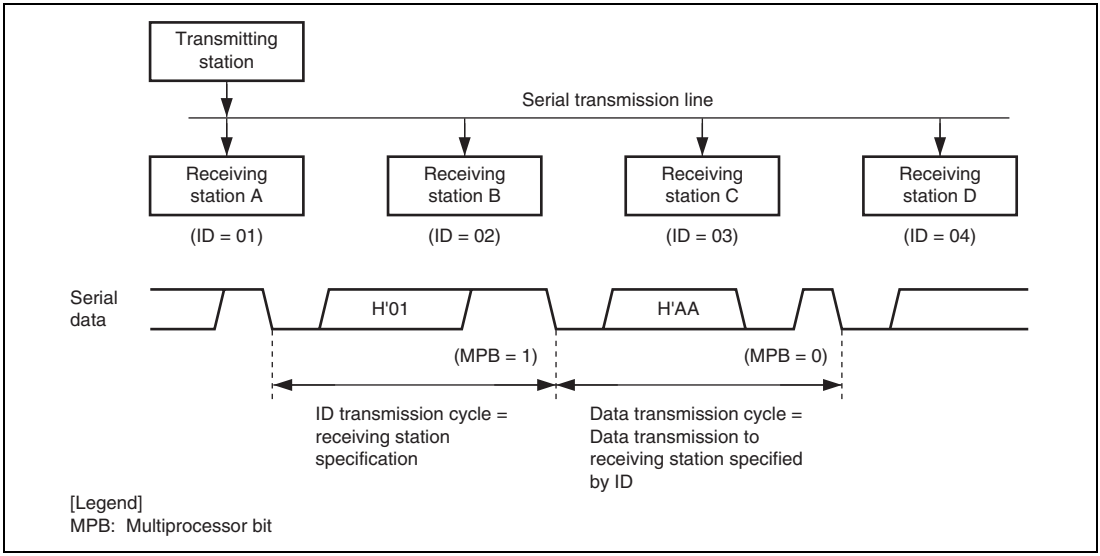


Figure 12.15 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

Bit	Bit Name	Initial Value	R/W	Description
14	ADIE	0	R/W	A/D Interrupt Enable The A/D conversion end interrupt (ADI) request is enabled when 1 is set When changing the operating mode, first clear the ADST bit to 0.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TRGE	0	R/W	Trigger Enable Enables or disables triggering of A/D conversion by $\overline{\text{ADTRG}}$ and an MTU2 trigger. 0: A/D conversion triggering is disabled 1: A/D conversion triggering is enabled When changing the operating mode, first clear the ADST bit to 0.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	CONADF	0	R/W	ADF Control Controls setting of the ADF bit in 2-channel scan mode. The setting of this bit is valid only when triggering of A/D conversion is enabled (TRGE = 1) in 2-channel scan mode. The setting of this bit is ignored in single mode or 4-channel scan mode. 0: The ADF bit is set when A/D conversion started by the group 0 trigger or group 1 trigger has finished. 1: The ADF bit is set when A/D conversion started by the group 0 trigger and A/D conversion started by the group 1 trigger have both finished. Note that the triggering order has no affect. When changing the operating mode, first clear the ADST bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	TRG0S[3:0]	0000	R/W	A/D Trigger 0 Select 3 to 0 Select an external trigger or MTU2 trigger to start A/D conversion for group 0 when A/D module 0 is in single mode, 4-channel scan mode, or 2-channel scan mode. 0000: External trigger pin ($\overline{\text{ADTRG}}$) input 0001: TRGA input capture/compare match for each MTU2 channel or TCNT_4 underflow (trough) in complementary PWM mode (TRGAN) 0010: MTU2 channel 0 compare match (TRG0N) 0011: MTU2 A/D conversion start request delaying (TRG4AN) 0100: MTU2 A/D conversion start request delaying (TRG4BN) 0101: Setting prohibited 0110: Setting prohibited 0111: Setting prohibited 1xxx: Setting prohibited When switching the selector, first clear the ADST bit in the A/D control register (ADCR) to 0. Specify different trigger sources for the group 0 and group 1 conversion requests so that a group 0 conversion request is not generated simultaneously with a group 1 conversion request in 2-channel scan mode.

[Legend]

x: Don't care

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PE9MD2	0	R/W	PE9 Mode
5	PE9MD1	0	R/W	Select the function of the PE9/TIOC3B pin.
4	PE9MD0	0	R/W	000: PE9 I/O (port) 001: TIOC3B I/O (MTU2) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PE8MD2	0	R/W	PE8 Mode
1	PE8MD1	0	R/W	Select the function of the PE8/TIOC3A pin.
0	PE8MD0	0	R/W	000: PE8 I/O (port) 001: TIOC3A I/O (MTU2) Other than above: Setting prohibited

- Port E Control Register L2 (PECRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

16.2 Port B

Port B in the SH7125 is an input/output port with the five pins shown in figure 16.3.

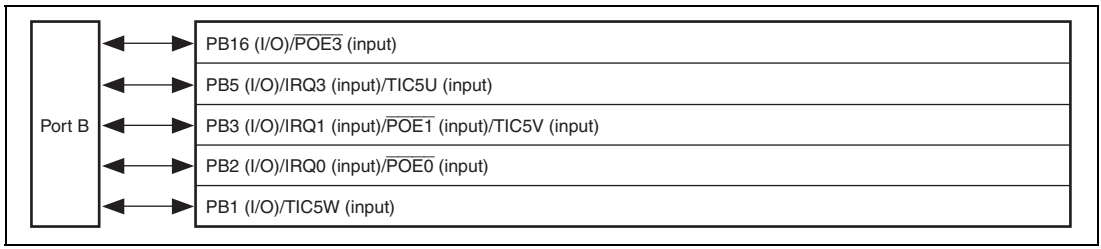


Figure 16.3 Port B (SH7125)

Port B in the SH7124 is an input/output port with the three pins shown in figure 16.4.

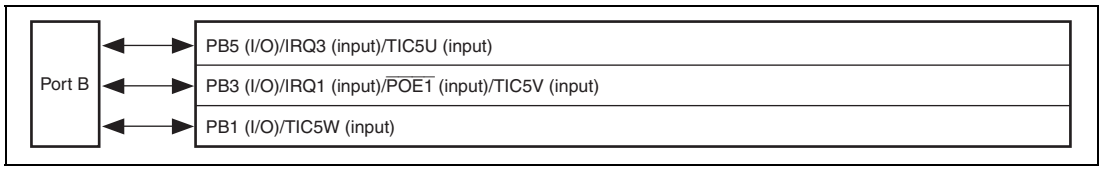


Figure 16.4 Port B (SH7124)

16.2.1 Register Descriptions

Port B is a 5-bit input/output port in the SH7125 and a 3-bit input/output port in the SH7124. Port B has the following register. For details on register addresses and register states during each processing, refer to section 20, List of Registers.

Table 16.3 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Port B data register H	PBDRH	R/W	H'0000	H'FFFFD180	8, 16, 32
Port B data register L	PBDRL	R/W	H'0000	H'FFFFD182	8, 16
Port B port register H	PBPRH	R	—	H'FFFFD19C	8, 16, 32
Port B port register L	PBPRL	R	—	H'FFFFD19E	8, 16

(2.3) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter indicates the return value of the initialization result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	BR	FQ	SF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	Undefined	R/W	Unused Return 0.
2	BR	Undefined	R/W	User Branch Error Detect Returns the check result whether the specified user branch destination address is in the area other than the storage area of the programming/erasing program which has been downloaded. 0: User branch address setting is normal 1: User branch address setting is abnormal
1	FQ	Undefined	R/W	Frequency Error Detect Returns the check result whether the specified operating frequency of the CPU is in the range of the supported operating frequency. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	Undefined	R/W	Success/Fail Indicates whether initialization is completed normally. 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error occurs)

(1) SCI Interface Setting by Host

When boot mode is initiated, this LSI measures the low period of asynchronous SCI-communication data (H'00), which is transmitted consecutively by the host. The SCI transmit/receive format is set to 8-bit data, 1 stop bit, and no parity. This LSI calculates the bit rate of transmission by the host by means of the measured low period and transmits the bit adjustment end sign (1 byte of H'00) to the host. The host must confirm that this bit adjustment end sign (H'00) has been received normally and transmits 1 byte of H'55 to this LSI. When reception is not executed normally, boot mode is initiated again (reset) and the operation described above must be executed. The bit rate between the host and this LSI is not matched because of the bit rate of transmission by the host and system clock frequency of this LSI. To operate the SCI normally, the transfer bit rate of the host must be set to 9,600 bps or 19,200 bps.

The system clock frequency, which can automatically adjust the transfer bit rate of the host and the bit rate of this LSI is shown in table 17.7. Boot mode must be initiated in the range of this system clock. Note that the internal clock division ratio of ×1/3 is not supported in boot mode.

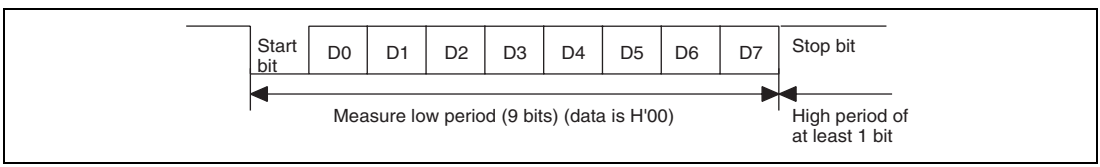


Figure 17.7 Automatic Adjustment Operation of SCI Bit Rate

Table 17.7 Peripheral Clock (Pϕ) Frequency that Can Automatically Adjust Bit Rate of This LSI

Host Bit Rate	Peripheral Clock (Pϕ) Frequency Which Can Automatically Adjust LSI's Bit Rate
9,600 bps	20 to 25 MHz
19,200 bps	20 to 25 MHz

Note: The internal clock division ratio of ×1/3 is not supported in boot mode.

H'26: Frequency multiplier error (the specified multiplier does not match an available one).

H'27: Operating frequency error (the specified operating frequency is not within the range from the minimum to the maximum value).

The received data are checked in the following ways.

1. Input frequency

   The value of the received input frequency is checked to see if it is within the range of the minimum and maximum values of input frequency for the selected clock mode of the selected device. A value outside the range generates an input frequency error.

2. Multiplier

   The value of the received multiplier is checked to see if it matches a multiplier or divisor that is available for the selected clock mode of the selected device. A value that does not match an available ratio generates a frequency multiplier error.

3. Operating frequency

   The operating frequency is calculated from the received input frequency and the frequency multiplier or divisor. The input frequency is the frequency of the clock signal supplied to the LSI, while the operating frequency is the frequency at which the LSI is actually driven. The following formulae are used for this calculation.

   Operating frequency = input frequency × multiplier, or

   Operating frequency = input frequency / divisor

   The calculated operating frequency is checked to see if it is within the range of the minimum and maximum values of the operating frequency for the selected clock mode of the selected device. A value outside the range generates an operating frequency error.

4. Bit rate

   From the peripheral operating frequency (Pϕ) and the bit rate (B), the value (= n) of the clock select bits (CKS) in the serial mode register (SCSMR) and the value (= N) of the bit rate register (SCBRR) are calculated, after which the error in the bit rate is calculated. This error is checked to see if it is smaller than 4%. A result greater than or equal to 4% generates a bit rate selection error. The following formula is use to calculate the error.

$$\text{Error (\%)} = \left\{ \left[\frac{P\phi \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} \right] - 1 \right\} \times 100$$

20.1 Register Address Table (In the Order from Lower Addresses)

Access sizes are indicated with the number of bits. Access states are indicated with the number of specified reference clock states. These values are those at 8-bit access (B), 16-bit access (W), or 32-bit access (L).

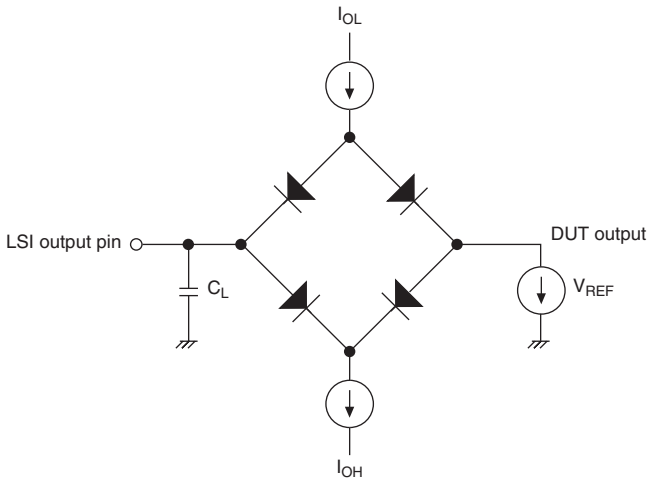
Note: Access to undefined or reserved addresses is prohibited. Correct operation cannot be guaranteed if these addresses are accessed.

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size	Number of Access States
Serial mode register_0	SCSMR_0	8	H'FFFFC000	SCI	8	Pϕ reference
Bit rate register_0	SCBRR_0	8	H'FFFFC002	(Channel 0)	8	B: 2
Serial control register_0	SCSCR_0	8	H'FFFFC004		8	
Transmit data register_0	SCTDR_0	8	H'FFFFC006		8	
Serial status register_0	SCSSR_0	8	H'FFFFC008		8	
Receive data register_0	SCRDR_0	8	H'FFFFC00A		8	
Serial direction control register_0	SCSDCR_0	8	H'FFFFC00C		8	
Serial port register_0	SCSPTR_0	8	H'FFFFC00E		8	
Serial mode register_1	SCSMR_1	8	H'FFFFC080	SCI	8	Pϕ reference
Bit rate register_1	SCBRR_1	8	H'FFFFC082	(Channel 1)	8	B: 2
Serial control register_1	SCSCR_1	8	H'FFFFC084		8	
Transmit data register_1	SCTDR_1	8	H'FFFFC086		8	
Serial status register_1	SCSSR_1	8	H'FFFFC088		8	
Receive data register_1	SCRDR_1	8	H'FFFFC08A		8	
Serial direction control register_1	SCSDCR_1	8	H'FFFFC08C		8	
Serial port register_1	SCSPTR_1	8	H'FFFFC08E		8	
Serial mode register_2	SCSMR_2	8	H'FFFFC100	SCI	8	Pϕ reference
Bit rate register_2	SCBRR_2	8	H'FFFFC102	(Channel 2)	8	B: 2
Serial control register_2	SCSCR_2	8	H'FFFFC104		8	
Transmit data register_2	SCTDR_2	8	H'FFFFC106		8	
Serial status register_2	SCSSR_2	8	H'FFFFC108		8	
Receive data register_2	SCRDR_2	8	H'FFFFC10A		8	
Serial direction control register_2	SCSDCR_2	8	H'FFFFC10C		8	
Serial port register_2	SCSPTR_2	8	H'FFFFC10E		8	

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
PBPRH (SH7125)	—	—	—	—	—	—	—	—	I/O
	—	—	—	—	—	—	—	PB16PR	
PBPRH (SH7124)	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
PBPRL (SH7125)	—	—	—	—	—	—	—	—	
	—	—	PB5PR	—	PB3PR	PB2PR	PB1PR	—	
PBPRL (SH7124)	—	—	—	—	—	—	—	—	
	—	—	PB5PR	—	PB3PR	—	PB1PR	—	
PEDRL (SH7125)	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	
	PE7DR	PE6DR	PE5DR	PE4DR	PE3DR	PE2DR	PE1DR	PE0DR	
PEDRL (SH7124)	PE15DR	PE14DR	PE13DR	PE12DR	PE11DR	PE10DR	PE9DR	PE8DR	
	—	—	—	—	PE3DR	PE2DR	PE1DR	PE0DR	
PEIORL (SH7125)	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	PFC
	PE7IOR	PE6IOR	PE5IOR	PE4IOR	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
PEIORL (SH7124)	PE15IOR	PE14IOR	PE13IOR	PE12IOR	PE11IOR	PE10IOR	PE9IOR	PE8IOR	
	—	—	—	—	PE3IOR	PE2IOR	PE1IOR	PE0IOR	
PECRL4	—	PE15MD2	PE15MD1	PE15MD0	—	PE14MD2	PE14MD1	PE14MD0	
	—	—	PE13MD1	PE13MD0	—	PE12MD2	PE12MD1	PE12MD0	
PECRL3	—	PE11MD2	PE11MD1	PE11MD0	—	PE10MD2	PE10MD1	PE10MD0	
	—	PE9MD2	PE9MD1	PE9MD0	—	PE8MD2	PE8MD1	PE8MD0	
PECRL2 (SH7125)	—	PE7MD2	PE7MD1	PE7MD0	—	PE6MD2	PE6MD1	PE6MD0	
	—	PE5MD2	PE5MD1	PE5MD0	—	PE4MD2	PE4MD1	PE4MD0	
PECRL2 (SH7124)	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
PECRL1	—	PE3MD2	PE3MD1	PE3MD0	—	PE2MD2	PE2MD1	PE2MD0	
	—	PE1MD2	PE1MD1	PE1MD0	—	—	PE0MD1	PE0MD0	
PEPRL (SH7125)	PE15PR	PE14PR	PE13PR	PE12PR	PE11PR	PE10PR	PE9PR	PE8PR	I/O
	PE7PR	PE6PR	PE5PR	PE4PR	PE3PR	PE2PR	PE1PR	PE0PR	
PEPRL (SH7124)	PE15PR	PE14PR	PE13PR	PE12PR	PE11PR	PE10PR	PE9PR	PE8PR	
	—	—	—	—	PE3PR	PE2PR	PE1PR	PE0PR	

21.3.9 Conditions for Testing AC Characteristics

- Input signal level: V_{IL} (Max.)/V_{IH} (Min.)
- Output signal reference level: 2.0 V (high level), 0.8 V (low level)



Notes: 1. C_L is the total value that includes the capacitance of the measurement instrument and is set as follows for the respective pins.
30pF: All other output pins
2. I_{OL} = 1.6 mA and I_{OH} = -200 mA in the test conditions.

Figure 21.16 Output Load Circuit