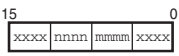
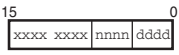
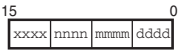
Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250ad50npv

Instruction Format	Source Operand	Destination Operand	Sample Instruction
nm type 	mmmm: register direct	nnnn: register direct	ADD Rm,Rn
	mmmm: register direct	nnnn: register indirect	MOV.L Rm,@Rn
	mmmm: post-increment register indirect (multiply-and-accumulate operation) nnnn: * post-increment register indirect (multiply-and-accumulate operation)	MACH, MACL	MAC.W @Rm+,@Rn+
	mmmm: post-increment register indirect	nnnn: register direct	MOV.L @Rm+,Rn
	mmmm: register direct	nnnn: pre-decrement register indirect	MOV.L Rm,@-Rn
	mmmm: register direct	nnnn: index register indirect	MOV.L Rm,@(R0,Rn)
md type 	mmmmdddd: register indirect with displacement	R0 (register direct)	MOV.B @(disp,Rm),R0
nd4 type 	R0 (register direct)	nnnndddd: register indirect with displacement	MOV.B R0,@(disp,Rn)
nmd type 	mmmm: register direct	nnnndddd: register indirect with displacement	MOV.L Rm,@(disp,Rn)
	mmmmdddd: register indirect with displacement	nnnn: register direct	MOV.L @(disp,Rm),Rn

Instruction		Operation	Code	Execution Cycles	T Bit
MOV.B	Rm,@(R0,Rn)	Rm → (R0 + Rn)	0000nnnnmmmm0100	1	—
MOV.W	Rm,@(R0,Rn)	Rm → (R0 + Rn)	0000nnnnmmmm0101	1	—
MOV.L	Rm,@(R0,Rn)	Rm → (R0 + Rn)	0000nnnnmmmm0110	1	—
MOV.B	@(R0,Rm),Rn	(R0 + Rm) → Sign extension → Rn	0000nnnnmmmm1100	1	—
MOV.W	@(R0,Rm),Rn	(R0 + Rm) → Sign extension → Rn	0000nnnnmmmm1101	1	—
MOV.L	@(R0,Rm),Rn	(R0 + Rm) → Rn	0000nnnnmmmm1110	1	—
MOV.B	R0,@(disp,GBR)	R0 → (disp + GBR)	11000000dddddddd	1	—
MOV.W	R0,@(disp,GBR)	R0 → (disp × 2 + GBR)	11000001dddddddd	1	—
MOV.L	R0,@(disp,GBR)	R0 → (disp × 4 + GBR)	11000010dddddddd	1	—
MOV.B	@(disp,GBR),R0	(disp + GBR) → Sign extension → R0	11000100dddddddd	1	—
MOV.W	@(disp,GBR),R0	(disp × 2 + GBR) → Sign extension → R0	11000101dddddddd	1	—
MOV.L	@(disp,GBR),R0	(disp × 4 + GBR) → R0	11000110dddddddd	1	—
MOVA	@(disp,PC),R0	disp × 4 + PC → R0	11000111dddddddd	1	—
MOVT	Rn	T → Rn	0000nnnn00101001	1	—
SWAP.B	Rm,Rn	Rm → Swap lowest two bytes → Rn	0110nnnnmmmm1000	1	—
SWAP.W	Rm,Rn	Rm → Swap two consecutive words → Rn	0110nnnnmmmm1001	1	—
XTRCT	Rm,Rn	Rm: Middle 32 bits of Rn → Rn	0010nnnnmmmm1101	1	—

3.2 Input/Output Pins

Table 3.2 describes the configuration of operating mode related pin.

Table 3.2 Pin Configuration

Pin Name	Input/Output	Function
MD1	Input	Designates operating mode through the level applied to this pin
FWE	Input	Enables, by hardware, programming/erasing of the on-chip flash memory

3.3 Operating Modes

3.3.1 Mode 3 (Single Chip Mode)

All ports can be used in this mode, however the external address cannot be used.

Section 4 Clock Pulse Generator (CPG)

This LSI has a clock pulse generator (CPG) that generates an internal clock (Iϕ), a bus clock (Bϕ), a peripheral clock (Pϕ), and a clock (MPϕ) for the MTU2 module. The CPG also controls power-down modes.

4.1 Features

- Five clocks generated independently

  An internal clock (Iϕ) for the CPU; a peripheral clock (Pϕ) for the on-chip peripheral modules; a bus clock (Bϕ = CK) for the external bus interface; and a MTU2 clock (MPϕ) for the on-chip MTU2 module.
- Frequency change function

  Frequencies of the internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), and MTU2 clock (MPϕ) can be changed independently using the divider circuit within the CPG. Frequencies are changed by software using the frequency control register (FRQCR) setting.
- Power-down mode control

  The clock can be stopped in sleep mode and standby mode and specific modules can be stopped using the module standby function.
- Oscillation stop detection

  If the clock supplied through the clock input pin stops for any reason, the timer pins can be automatically placed in the high-impedance state.

7.2.1 Break Address Register A (BARA)

BARA is a 32-bit readable/writable register. BARA specifies the address used as a break condition in channel A.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BAA31	BAA30	BAA29	BAA28	BAA27	BAA26	BAA25	BAA24	BAA23	BAA22	BAA21	BAA20	BAA19	BAA18	BAA17	BAA16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BAA15	BAA14	BAA13	BAA12	BAA11	BAA10	BAA9	BAA8	BAA7	BAA6	BAA5	BAA4	BAA3	BAA2	BAA1	BAA0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BAA31 to BAA 0	All 0	R/W	Break Address A Store the address on the LAB or IAB specifying break conditions of channel A.

7.2.2 Break Address Mask Register A (BAMRA)

BAMRA is a 32-bit readable/writable register. BAMRA specifies bits masked in the break address specified by BARA.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BAMA31	BAMA30	BAMA29	BAMA28	BAMA27	BAMA26	BAMA25	BAMA24	BAMA23	BAMA22	BAMA21	BAMA20	BAMA19	BAMA18	BAMA17	BAMA16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BAMA15	BAMA14	BAMA13	BAMA12	BAMA11	BAMA10	BAMA9	BAMA8	BAMA7	BAMA6	BAMA5	BAMA4	BAMA3	BAMA2	BAMA1	BAMA0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

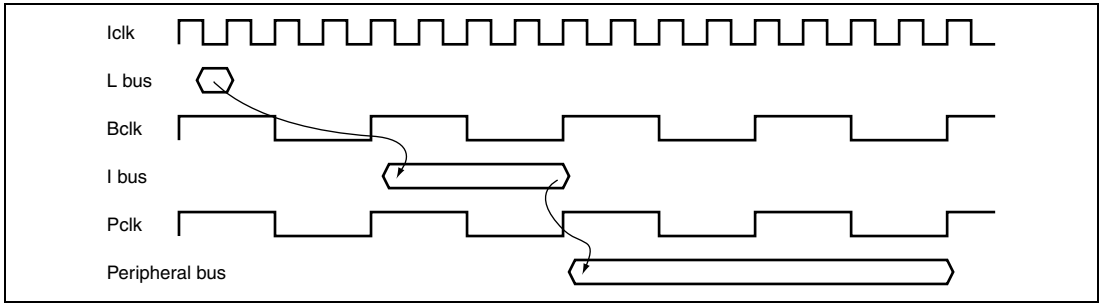


Figure 8.1 Timing of Write Access to the Peripheral Bus (Iclk:Bclk:Pclk = 4:1:1)

Figure 8.2 shows an example of timing of write access to the peripheral bus when Iclk:Bclk:Pclk = 4:4:1. From the L bus, to which the CPU is connected, data is output in synchronization with Iclk. When Iclk:Bclk = 1:1, a period of 3 Iclk + Bclk is required to transfer data from the L bus to the I bus. In data transfer from the I bus to the peripheral bus, there are four BIclk cycles in a single Pclk cycle when Bclk:Pclk = 4:1, and data can therefore be output onto the peripheral bus in four possible timings within one Pclk cycle. Accordingly, a maximum of four Bclk cycles of period (four Bclk cycles in the example shown in the figure) is required before the rising edge of Pclk, on which data is transferred from the I bus to the peripheral bus. Because of this, data is transferred from the I bus to the peripheral bus in a period of (1 + m) × Bclk (m = 0 to 3) when Bclk:Pclk = 4:1. The relation of the timing of data output to the I bus and the rising edge of Pclk depends on the state of program execution. In the case shown in figure 8.2, where Iclk = Bclk = 1:1, the period required for access by the CPU is 3 × Iclk + (1 + m) × Bclk + 2 × Pclk.

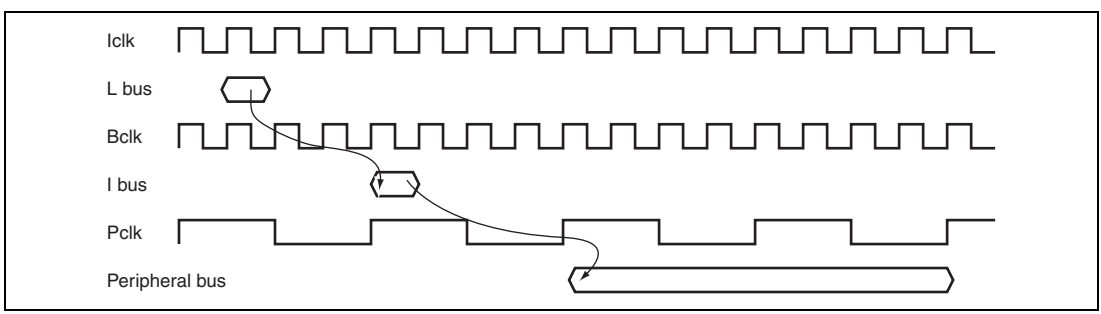


Figure 8.2 Timing of Write Access to the Peripheral Bus (Iclk:Bclk:Pclk = 4:4:1)

Figure 8.3 shows an example of timing of read access to the peripheral bus when Iclk:Bclk:Pclk = 4:2:1. Transfer from the L bus to the peripheral bus is performed in the same way as for write access. In the case of reading, however, values output onto the peripheral bus must be transferred to the CPU. Transfers from the external bus to the I bus and from the I bus to the L bus are again performed in synchronization with rising edges of the respective bus clocks. 2 × Iclk cycles of

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
A/D converter start request delaying function	—	—	—	—	• A/D converter start request at a match between TADCORA_4 and TCNT_4 • A/D converter start request at a match between TADCORB_4 and TCNT_4	—
Interrupt skipping function	—	—	—	• Skips TGRA_3 compare match interrupts	• Skips TCIV_4 interrupts	—

[Legend]

√: Possible

—: Not possible

Notes: 1. This pin is supported only by the SH7125.

2. Input capture is supported only by the SH7125.

Figure 9.1 shows a block diagram of the MTU2.

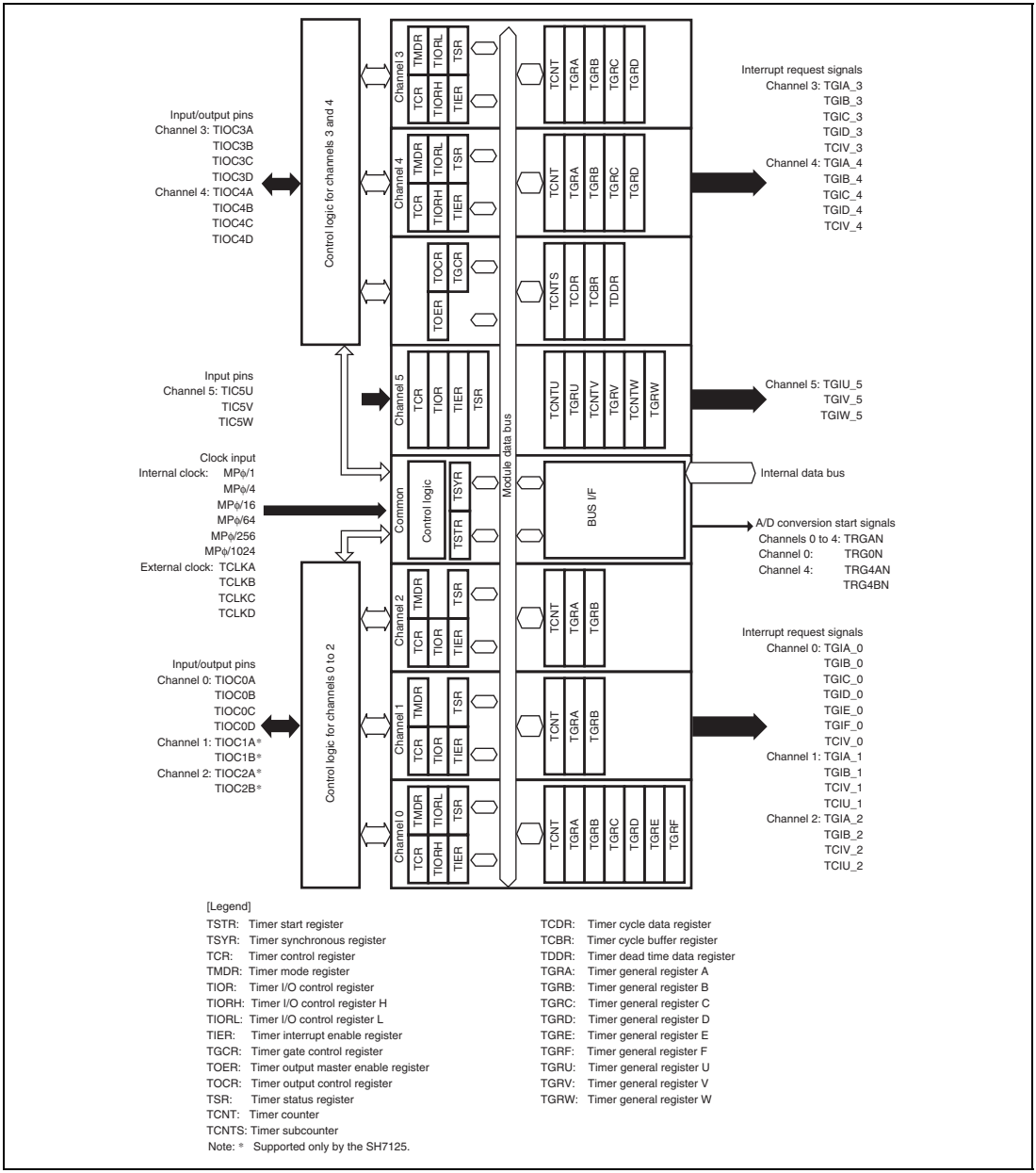


Figure 9.1 Block Diagram of MTU2

Figure 11.1 shows a block diagram of the WDT.

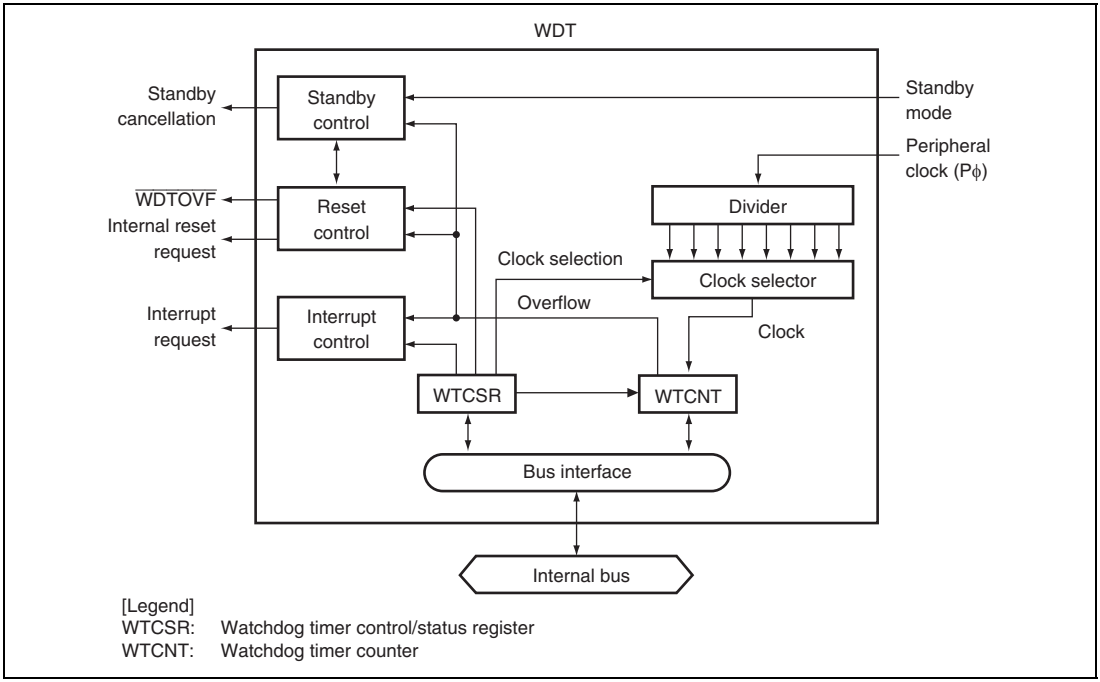


Figure 11.1 Block Diagram of WDT

16.3.3 Port E Port Register L (PEPRL)

PEPRL is a 16-bit read-only register that always returns the states of the pins regardless of the PFC setting. Bits PE15PR to PE0PR correspond to pins PE15 to PE0 (multiplexed functions omitted here) in the SH7125. Bits PE15PR to PE8PR and PE3PR to PE0PR correspond to pins PE15 to PE8 and PE3 to PE0, respectively (multiplexed functions omitted here) in the SH7124.

- PEPRL (SH7125)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PE15PR	PE14PR	PE13PR	PE12PR	PE11PR	PE10PR	PE9PR	PE8PR	PE7PR	PE6PR	PE5PR	PE4PR	PE3PR	PE2PR	PE1PR	PE0PR
Initial value:	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PE15PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
14	PE14PR	Pin state	R	
13	PE13PR	Pin state	R	
12	PE12PR	Pin state	R	
11	PE11PR	Pin state	R	
10	PE10PR	Pin state	R	
9	PE9PR	Pin state	R	
8	PE8PR	Pin state	R	
7	PE7PR	Pin state	R	
6	PE6PR	Pin state	R	
5	PE5PR	Pin state	R	
4	PE4PR	Pin state	R	
3	PE3PR	Pin state	R	
2	PE2PR	Pin state	R	
1	PE1PR	Pin state	R	
0	PE0PR	Pin state	R	

(2) Download of On-Chip Program

The on-chip program is automatically downloaded by clearing VBR of the CPU to H'84000000 and then setting the SCO bit in the flash code control and status register (FCCS) and the flash key code register (FKEY), which are programming/erasing interface registers.

The user MAT is replaced to the embedded program storage area when downloading. Since the flash memory cannot be read when programming/erasing, the procedure program, which is working from download to completion of programming/erasing, must be executed in a space other than the flash memory to be programmed/erased (for example, on-chip RAM).

Since the result of download is returned to the programming/erasing interface parameters, whether the normal download is executed or not can be confirmed.

Note that VBR can be changed after download is completed.

(3) Initialization of Programming/Erasing

The operating frequency and user branch are set before execution of programming/erasing. The user branch destination must be in an area other than the user MAT area, which is in the middle of programming and the area where the on-chip program is downloaded. These settings are performed by using the programming/erasing interface parameters.

(4) Programming/Erasing Execution

To program or erase, the FWE pin must be brought high and user program mode must be entered.

The program data/programming destination address is specified in 128-byte units when programming.

The block to be erased is specified in erase-block units when erasing.

These specifications are set by using the programming/erasing interface parameters and the on-chip program is initiated. The on-chip program is executed by using the JSR or BSR instruction to perform the subroutine call of the specified address in the on-chip RAM. The execution result is returned to the programming/erasing interface parameters.

The area to be programmed must be erased in advance when programming flash memory.

There are limitations and notes on the interrupt processing during programming/erasing. For details, see section 17.7.1, Interrupts during Programming/Erasing.

(5) When Programming/Erasing is Executed Consecutively

When the processing is not ended by the 128-byte programming or one-block erasure, the program address/data and erase-block number must be updated and consecutive programming/erasing is required.

Since the downloaded on-chip program is left in the on-chip RAM after the processing, download and initialization are not required when the same processing is executed consecutively.

The programming/erasing interface parameters are used in the following four items.

1. Download control
2. Initialization before programming or erasing
3. Programming
4. Erasing

These items use different parameters. The correspondence table is shown in table 17.6.

The processing results of initialization, programming, and erasing are returned, but the bit contents have different meanings according to the processing program. See the description of FPFR for each processing.

Table 17.6 Usable Parameters and Target Modes

Name of Parameter	Abbreviation	Download	Initialization	Programming	Erasure	R/W	Initial Value	Allocation
Download pass/fail result	DPFR	√	—	—	—	R/W	Undefined	On-chip RAM*
Flash pass/fail result	FPFR	—	√	√	√	R/W	Undefined	R0 of CPU
Flash programming/ erasing frequency control	FPEFEQ	—	√	—	—	R/W	Undefined	R4 of CPU
Flash user branch address set	FUBRA	—	√	—	—	R/W	Undefined	R5 of CPU
Flash multipurpose address area	FMPAR	—	—	√	—	R/W	Undefined	R5 of CPU
Flash multipurpose data destination area	FMPDR	—	—	√	—	R/W	Undefined	R4 of CPU
Flash erase block select	FEBS	—	—	—	√	R/W	Undefined	R4 of CPU

Note: * One byte of start address of download destination specified by FTDAR

(1) SCI Interface Setting by Host

When boot mode is initiated, this LSI measures the low period of asynchronous SCI-communication data (H'00), which is transmitted consecutively by the host. The SCI transmit/receive format is set to 8-bit data, 1 stop bit, and no parity. This LSI calculates the bit rate of transmission by the host by means of the measured low period and transmits the bit adjustment end sign (1 byte of H'00) to the host. The host must confirm that this bit adjustment end sign (H'00) has been received normally and transmits 1 byte of H'55 to this LSI. When reception is not executed normally, boot mode is initiated again (reset) and the operation described above must be executed. The bit rate between the host and this LSI is not matched because of the bit rate of transmission by the host and system clock frequency of this LSI. To operate the SCI normally, the transfer bit rate of the host must be set to 9,600 bps or 19,200 bps.

The system clock frequency, which can automatically adjust the transfer bit rate of the host and the bit rate of this LSI is shown in table 17.7. Boot mode must be initiated in the range of this system clock. Note that the internal clock division ratio of ×1/3 is not supported in boot mode.

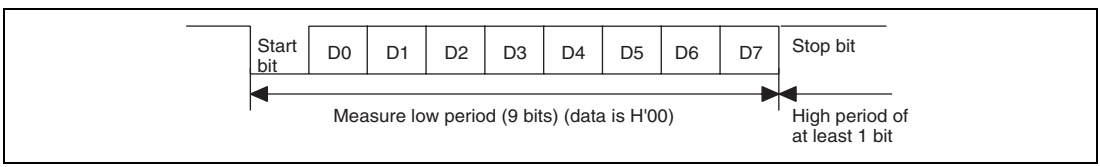


Figure 17.7 Automatic Adjustment Operation of SCI Bit Rate

Table 17.7 Peripheral Clock (Pϕ) Frequency that Can Automatically Adjust Bit Rate of This LSI

Host Bit Rate	Peripheral Clock (Pϕ) Frequency Which Can Automatically Adjust LSI's Bit Rate
9,600 bps	20 to 25 MHz
19,200 bps	20 to 25 MHz

Note: The internal clock division ratio of ×1/3 is not supported in boot mode.

(2) State Transition Diagram

Figure 17.8 gives an overview of the state transitions after the chip has been started up in boot mode. For details on boot mode, see section 17.8.1, Specifications of the Standard Serial Communications Interface in Boot Mode.

1. Bit-rate matching

   After the chip has been started up in boot mode, bit-rate matching between the SCI and the host proceeds.

2. Waiting for inquiry and selection commands

   The chip sends the requested information to the host in response to inquiries regarding the size and configuration of the user MAT, start addresses of the MATs, information on supported devices, etc.

3. Automatic erasure of the entire user MAT

   After all necessary inquiries and selections have been made and the command for transition to the programming/erasure state is sent by the host, the entire user MAT is automatically erased.

4. Waiting for programming/erasure command

— On receiving the programming selection command, the chip waits for data to be programmed. To program data, the host transmits the programming command code followed by the address where programming should start and the data to be programmed. This is repeated as required while the chip is in the programming-selected state. To terminate programming, H'FFFFFFFF should be transmitted as the first address of the area for programming. This makes the chip return to the programming/erasure command waiting state from the programming data waiting state.

— On receiving the erasure select command, the chip waits for the block number of a block to be erased. To erase a block, the host transmits the erasure command code followed by the number of the block to be erased. This is repeated as required while the chip is in the erasure-selected state. To terminate erasure, H'FF should be transmitted as the block number. This makes the chip return to the programming/erasure command waiting state from the erasure block number waiting state. Erasure should only be executed when a specific block is to be reprogrammed without executing a reset-start of the chip after the flash memory has been programmed in boot mode. If all desired programming is done in a single operation, such erasure processing is not necessary because all blocks are erased before the chip enters the programming/erasure/other command waiting state.

— In addition to the programming and erasure commands, commands for sum checking and blank checking (checking for erasure) of the user MAT, reading data from the user MAT, and acquiring current state information are provided.

Note that the command for reading from the user MAT can only read data that has been programmed after automatic erasure of the entire user MAT.

19.3.4 Standby Control Register 4 (STBCR4)

STBCR4 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	-	MSTP22	MSTP21	-	-	-	MSTP17	MSTP16
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
6	MSTP22	1	R/W	Module Stop Bit 22 When this bit is set to 1, the supply of the clock to the MTU2 is halted. 0: MTU2 operates 1: Clock supply to MTU2 halted
5	MSTP21	1	R/W	Module Stop Bit 21 When this bit is set to 1, the supply of the clock to the CMT is halted. 0: CMT operates 1: Clock supply to CMT halted
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
1	MSTP17	1	R/W	Module Stop Bit 17 When this bit is set to 1, the supply of the clock to the A/D_1 is halted. 0: A/D_1 operates 1: Clock supply to A/D_1 halted

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
TCR_3	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]			MTU2
TCR_4	CCLR[2:0]			CKEG[1:0]		TPSC[2:0]			
TMDR_3	—	—	BFB	BFA	MD[3:0]				
TMDR_4	—	—	BFB	BFA	MD[3:0]				
TIORH_3	IOB[3:0]				IOA[3:0]				
TIORL_3	IOD[3:0]				IOC[3:0]				
TIORH_4	IOB[3:0]				IOA[3:0]				
TIORL_4	IOD[3:0]				IOC[3:0]				
TIER_3	TTGE	—	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TIER_4	TTGE	TTGE2	—	TCIEV	TGIED	TGIEC	TGIEB	TGIEA	
TOER	—	—	OE4D	OE4C	OE3D	OE4B	OE4A	OE3B	
TGCR	—	BDC	N	P	FB	WF	VF	UF	
TOCR1	—	PSYE	—	—	TOCL	TOCS	OLSN	OLSP	
TOCR2	BF[1:0]		OLS3N	OLS3P	OLS2N	OLS2P	OLS1N	OLS1P	
TCNT_3									
TCNT_4									
TCDR									
TDDR									
TGRA_3									
TGRB_3									
TGRA_4									
TGRB_4									

21.3.5 Watchdog Timer (WDT) Timing

Table 21.9 Watchdog Timer (WDT) Timing

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = -20$ to +85°C (consumer specifications),
$T_a = -40$ to +85°C (industrial specifications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{\text{WDTOVF}}$ delay time (reference values)	t_{WOVD}	—	50	ns	Figure 21.11

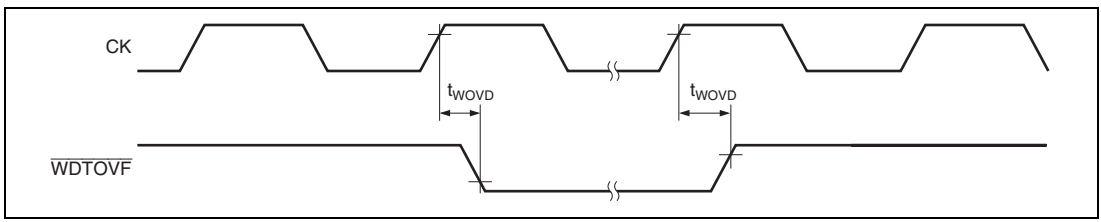


Figure 21.11 WDT Timing

Item	Page	Revision (See Manual for Details)
20.2 Register Bit List	699	Table amended

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
BARA	BAA31	BAA30	BAA29	BAA28	BAA27	BAA26	BAA25	BAA24	UBC*

	700	Table amended

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
BDRA	BDA31	BDA30	BDA29	BDA28	BDA27	BDA26	BDA25	BDA24	UBC*

	701	Table amended

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
BRSR	SVF				BSA27	BSA26	BSA25	BSA24	UBC*

Note added

Note: * The UBC registers are not supported on 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versions (SH71250A, SH71240A).

20.3 Register States in Each Operating Mode	708	Table amended

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep	Module
BARA	Initialized	Retained	Retained	Initialized	Retained	UBC*4

	709	Table amended

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep	Module
BDRB	Initialized	Retained	Retained	Initialized	Retained	UBC*4

Note added

Notes: 4. The UBC registers are not supported on 32 Kbyte versions (SH71251A, SH71241A) and 16 Kbyte versions (SH71250A, SH71240A).

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510