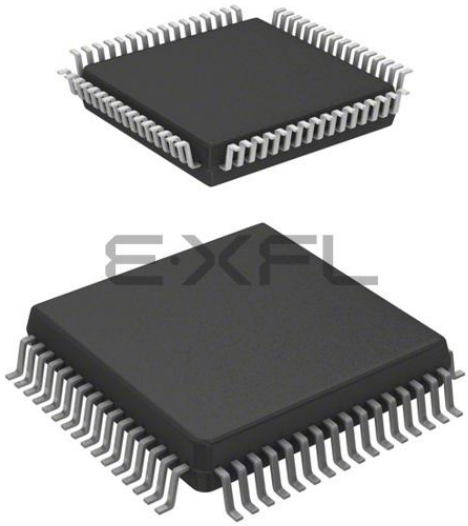

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-BQFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250an50fav

2.3 Data Formats

2.3.1 Register Data Format

The size of register operands is always longwords (32 bits). When loading byte (8 bits) or word (16 bits) data in memory into a register, the data is sign-extended to longword and stored in the register.

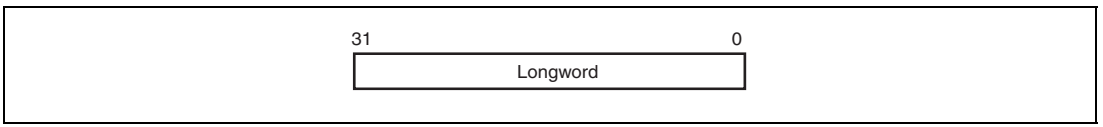


Figure 2.2 Register Data Format

2.3.2 Memory Data Formats

Memory data formats are classified into bytes, words, and longwords. Byte data can be accessed from any address. Locate, however, word data at an address 2n, longword data at 4n. Otherwise, an address error will occur if an attempt is made to access word data starting from an address other than 2n or longword data starting from an address other than 4n. In such cases, the data accessed cannot be guaranteed. The hardware stack area, pointed by the hardware stack pointer (SP, R15), uses only longword data starting from address 4n because this area holds the program counter and status register.

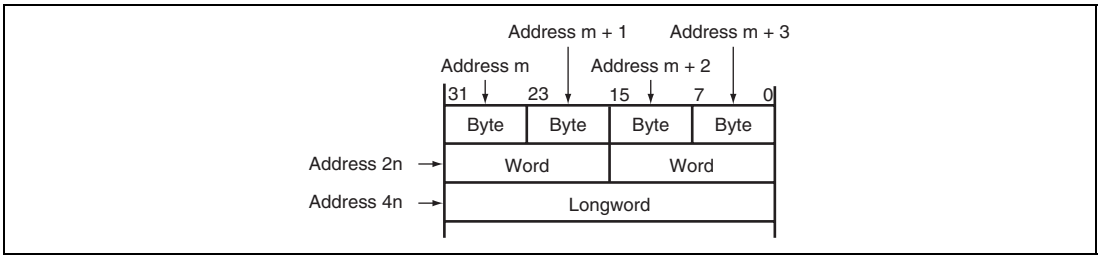


Figure 2.3 Memory Data Format

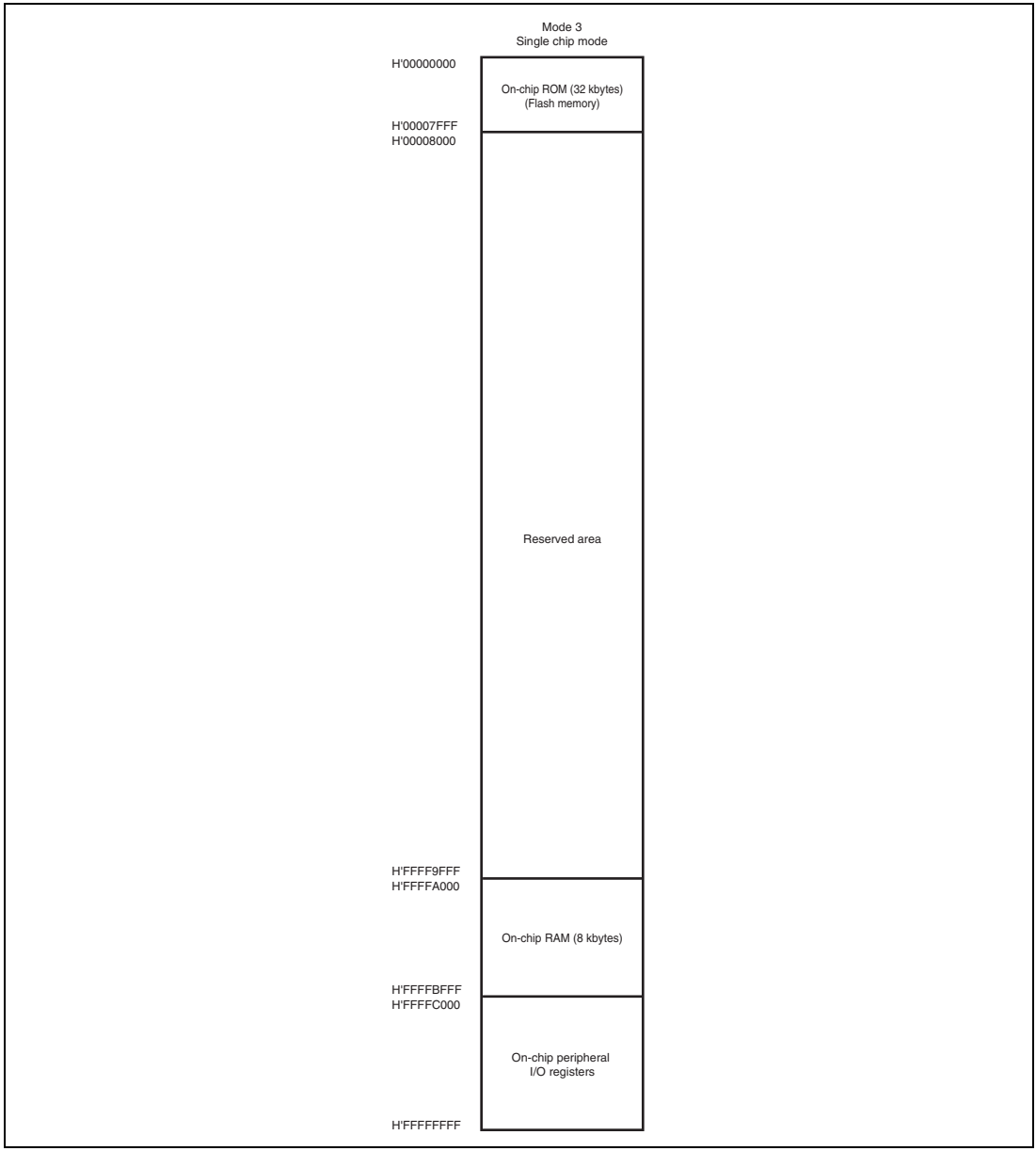


Figure 3.3 Address Map in SH71251A and SH71241A (32 Kbytes Flash Memory Version)

Bit	Bit Name	Initial Value	R/W	Description
3	IRQ11S	0	R/W	IRQ1 Sense Select
2	IRQ10S	0	R/W	Set the interrupt request detection mode for pin IRQ1. 00: Interrupt request is detected at the low level of pin IRQ1 01: Interrupt request is detected at the falling edge of pin IRQ1 10: Interrupt request is detected at the rising edge of pin IRQ1 11: Interrupt request is detected at both the falling and rising edges of pin IRQ1
1	IRQ01S	0	R/W	IRQ0 Sense Select (SH7125)
0	IRQ00S	0	R/W	Set the interrupt request detection mode for pin IRQ0. 00: Interrupt request is detected at the low level of pin IRQ0 01: Interrupt request is detected at the falling edge of pin IRQ0 10: Interrupt request is detected at the rising edge of pin IRQ0 11: Interrupt request is detected at both the falling and rising edges of pin IRQ0 Reserved (SH7124) These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IPR[7:4]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)
3 to 0	IPR[3:0]	0000	R/W	Set priority levels for the corresponding interrupt source. 0000: Priority level 0 (lowest) 0001: Priority level 1 0010: Priority level 2 0011: Priority level 3 0100: Priority level 4 0101: Priority level 5 0110: Priority level 6 0111: Priority level 7 1000: Priority level 8 1001: Priority level 9 1010: Priority level 10 1011: Priority level 11 1100: Priority level 12 1101: Priority level 13 1110: Priority level 14 1111: Priority level 15 (highest)

Note: Name in the tables above is represented by a general name. Name in the list of register is, on the other hand, represented by a module name.

Register Name	Abbreviation	R/W	Initial value	Address	Access Size
Timer waveform control register	TWCR	R/W	H'00	H'FFFFC260	8
Timer start register	TSTR	R/W	H'00	H'FFFFC280	8, 16
Timer synchronous register	TSYR	R/W	H'00	H'FFFFC281	8
Timer read/write enable register	TRWER	R/W	H'01	H'FFFFC284	8
Timer control register_0	TCR_0	R/W	H'00	H'FFFFC300	8, 16, 32
Timer mode register_0	TMDR_0	R/W	H'00	H'FFFFC301	8
Timer I/O control register H_0	TIORH_0	R/W	H'00	H'FFFFC302	8, 16
Timer I/O control register L_0	TIORL_0	R/W	H'00	H'FFFFC303	8
Timer interrupt enable register_0	TIER_0	R/W	H'00	H'FFFFC304	8, 16, 32
Timer status register_0	TSR_0	R/W	H'C0	H'FFFFC305	8
Timer counter_0	TCNT_0	R/W	H'0000	H'FFFFC306	16
Timer general register A_0	TGRA_0	R/W	H'FFFF	H'FFFFC308	16, 32
Timer general register B_0	TGRB_0	R/W	H'FFFF	H'FFFFC30A	16
Timer general register C_0	TGRC_0	R/W	H'FFFF	H'FFFFC30C	16, 32
Timer general register D_0	TGRD_0	R/W	H'FFFF	H'FFFFC30E	16
Timer general register E_0	TGRE_0	R/W	H'FFFF	H'FFFFC320	16, 32
Timer general register F_0	TGRF_0	R/W	H'FFFF	H'FFFFC322	16
Timer interrupt enable register 2_0	TIER2_0	R/W	H'00	H'FFFFC324	8, 16
Timer status register 2_0	TSR2_0	R/W	H'C0	H'FFFFC325	8
Timer buffer operation transfer mode register_0	TBTM_0	R/W	H'00	H'FFFFC326	8
Timer control register_1	TCR_1	R/W	H'00	H'FFFFC380	8, 16
Timer mode register_1	TMDR_1	R/W	H'00	H'FFFFC381	8
Timer I/O control register_1	TIOR_1	R/W	H'00	H'FFFFC382	8
Timer interrupt enable register_1	TIER_1	R/W	H'00	H'FFFFC384	8, 16, 32
Timer status register_1	TSR_1	R/W	H'C0	H'FFFFC385	8

9.7.16 Overflow Flags in Reset Synchronous PWM Mode

When set to reset synchronous PWM mode, TCNT_3 and TCNT_4 start counting when the CST3 bit in TSTR is set to 1. At this point, TCNT_4's count clock source and count edge obey the TCR_3 setting.

In reset synchronous PWM mode, with cycle register TGRA_3's set value at H'FFFF, when specifying TGR3A compare-match for the counter clear source, TCNT_3 and TCNT_4 count up to H'FFFF, then a compare-match occurs with TGRA_3, and TCNT_3 and TCNT_4 are both cleared. At this point, TSR's overflow flag TCFV bit is not set.

Figure 9.121 shows a TCFV bit operation example in reset synchronous PWM mode with a set value for cycle register TGRA_3 of H'FFFF, when a TGRA_3 compare-match has been specified without synchronous setting for the counter clear source.

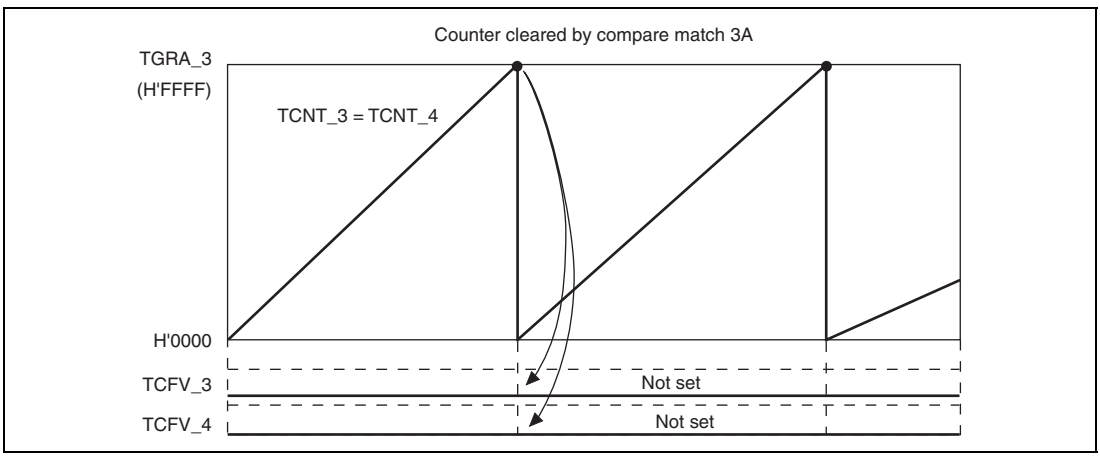


Figure 9.121 Reset Synchronous PWM Mode Overflow Flag

Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in PWM Mode 1: Figure 9.145 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in PWM mode 1 after re-setting.

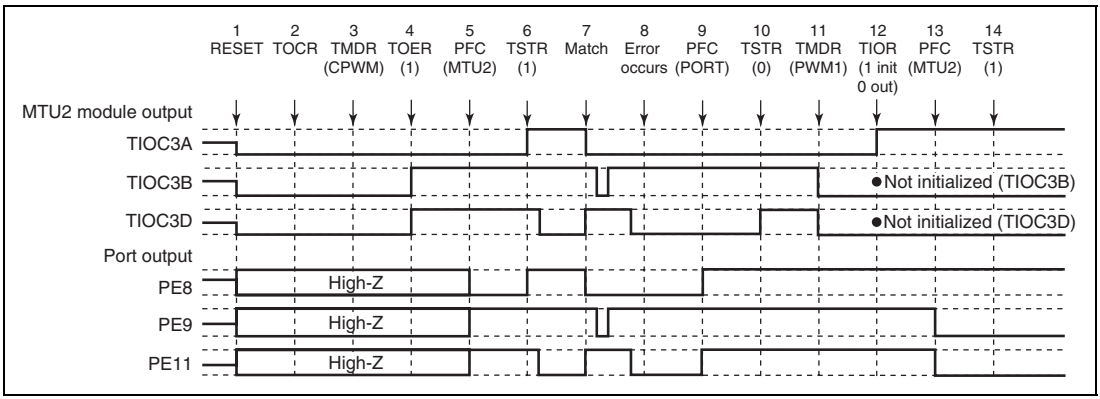


Figure 9.145 Error Occurrence in Complementary PWM Mode, Recovery in PWM Mode 1

1 to 10 are the same as in figure 9.144.

11. Set PWM mode 1. (MTU2 output goes low.)
12. Initialize the pins with TIOR. (In PWM mode 1, the TIOC *B side is not initialized.)
13. Set MTU2 output with the PFC.
14. Operation is restarted by TSTR.

Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode: Figure 9.146 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the cycle and duty settings at the time the counter was stopped).

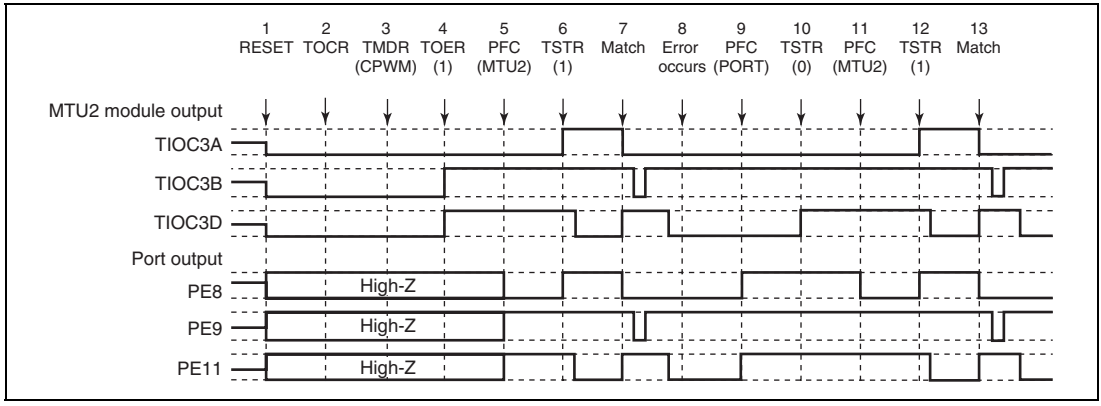


Figure 9.146 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 9.144.

11. Set MTU2 output with the PFC.
12. Operation is restarted by TSTR.
13. The complementary PWM waveform is output on compare-match occurrence.

10.3.1 Input Level Control/Status Register 1 (ICSR1)

ICSR1 is a 16-bit readable/writable register that selects the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, and $\overline{\text{POE3}}$ pin input modes, controls the enable/disable of interrupts, and indicates status.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	POE3F	-	POE1F	POE0F	-	-	-	PIE1	POE3M[1:0]		-	-	POE1M[1:0]		POE0M[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*1	R/(W)*1	R/(W)*1	R/(W)*1	R	R	R	R/W	R/W*2	R/W*2	R/W*2	R/W*2	R/W*2	R/W*2	R/W*2	R/W*2

Notes: 1. Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way.

2. Can be modified only once after a power-on reset.

Bit	Bit Name	Initial value	R/W	Description
15	POE3F	0	R/(W)*1	POE3 Flag (Supported only by the SH7125.) This flag indicates that a high impedance request has been input to the $\overline{\text{POE3}}$ pin. [Clearing conditions] • By writing 0 to POE3F after reading POE3F = 1 (when the falling edge is selected by bits 7 and 6 in ICSR1) • By writing 0 to POE3F after reading POE3F = 1 after a high level input to POE3 is sampled at Pϕ/8, Pϕ/16, or Pϕ/128 clock (when low-level sampling is selected by bits 7 and 6 in ICSR1) [Setting condition] • When the input set by ICSR1 bits 7 and 6 occurs at the $\overline{\text{POE3}}$ pin
14	—	0	R/(W)*1	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial value	R/W	Description
8	PIE1	0	R/W	Port Interrupt Enable 1 This bit enables/disables interrupt requests when any one of the POE0F to POE3F bits of the ICSR1 is set to 1. 0: Interrupt requests disabled 1: Interrupt requests enabled
7, 6	POE3M[1:0]	00	R/W*[2]	POE3 mode 1, 0 (Supported only by the SH7125. Write 00 to these bits in the SH7124.) These bits select the input mode of the $\overline{\text{POE3}}$ pin. 00: Accept request on falling edge of POE3 input 01: Accept request when POE3 input has been sampled for 16 Pϕ/8 clock pulses and all are low level. 10: Accept request when POE3 input has been sampled for 16 Pϕ/16 clock pulses and all are low level. 11: Accept request when POE3 input has been sampled for 16 Pϕ/128 clock pulses and all are low level.
5, 4	—	All 0	R/W*[2]	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	POE1M[1:0]	00	R/W*[2]	POE1 mode 1, 0 These bits select the input mode of the $\overline{\text{POE1}}$ pin. 00: Accept request on falling edge of POE1 input 01: Accept request when POE1 input has been sampled for 16 Pϕ/8 clock pulses and all are low level. 10: Accept request when POE1 input has been sampled for 16 Pϕ/16 clock pulses and all are low level. 11: Accept request when POE1 input has been sampled for 16 Pϕ/128 clock pulses and all are low level.

Section 13 A/D Converter (ADC)

This LSI includes a successive approximation type 10-bit A/D converter.

13.1 Features

- 10-bit resolution
- Input channels
  - 8 channels (two independent A/D conversion modules)
- Conversion time: 2.0 μs per channel (preliminary value, operation when Pϕ = 25 MHz)
- Three operating modes
  - Single mode: Single-channel A/D conversion
  - Continuous scan mode: Repetitive A/D conversion on up to four channels
  - Single-cycle scan mode: Continuous A/D conversion on up to four channels
- Data registers
  - Conversion results are held in a 16-bit data register for each channel
- Sample-and-hold function
- Three methods for conversion start
  - Software
  - Conversion start trigger from multifunction timer pulse unit 2 (MTU2)
  - External trigger signal
- Interrupt request
  - An A/D conversion end interrupt request (ADI) can be generated
- Module standby mode can be set

13.2 Input/Output Pins

Table 13.1 summarizes the input pins used by the A/D converter. This LSI has two A/D conversion modules, each of which can be operated independently. The input channels of A/D modules 0 and 1 are divided into two channel groups.

Table 13.1 Pin Configuration

Module Type	Symbol	I/O	Function	
Common	AV_{CC}	Input	Analog block power supply and reference voltage	
	AV_{SS}	Input	Analog block ground and reference voltage	
	$\overline{ADTRG}$	Input	A/D external trigger input pin*	
A/D module 0 (A/D_0)	AN0	Input	Analog input pin 0	Group 0
	AN1	Input	Analog input pin 1	
	AN2	Input	Analog input pin 2	Group 1
	AN3	Input	Analog input pin 3	
A/D module 1 (A/D_1)	AN4	Input	Analog input pin 4	Group 0
	AN5	Input	Analog input pin 5	
	AN6	Input	Analog input pin 6	Group 1
	AN7	Input	Analog input pin 7	

Notes: The connected A/D module differs for each pin. The control registers of each module must be set.

* This pin is supported only by the SH7125.

(1) On-Chip RAM Address Map when Programming/Erasing is Executed

Parts of the procedure program that are made by the user, like download request, programming/erasing procedure, and decision of the result, must be executed in the on-chip RAM. All of the on-chip program that is to be downloaded is in on-chip RAM. Note that on-chip RAM must be controlled so that these parts do not overlap.

Figure 17.10 shows the program area to be downloaded.

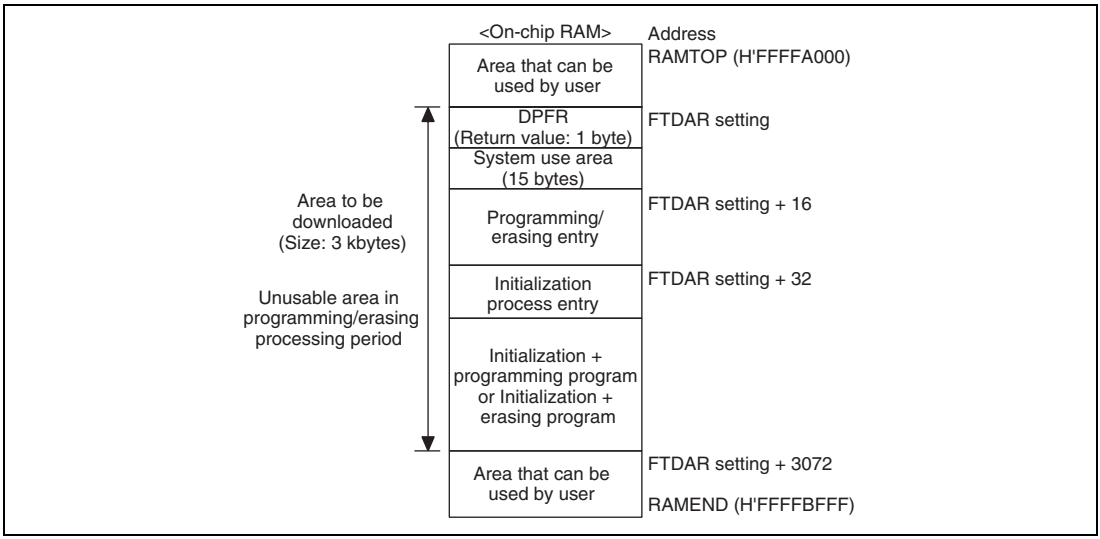


Figure 17.10 RAM Map after Download

(2) Programming Procedure in User Program Mode

The procedures for download, initialization, and programming are shown in figure 17.11.

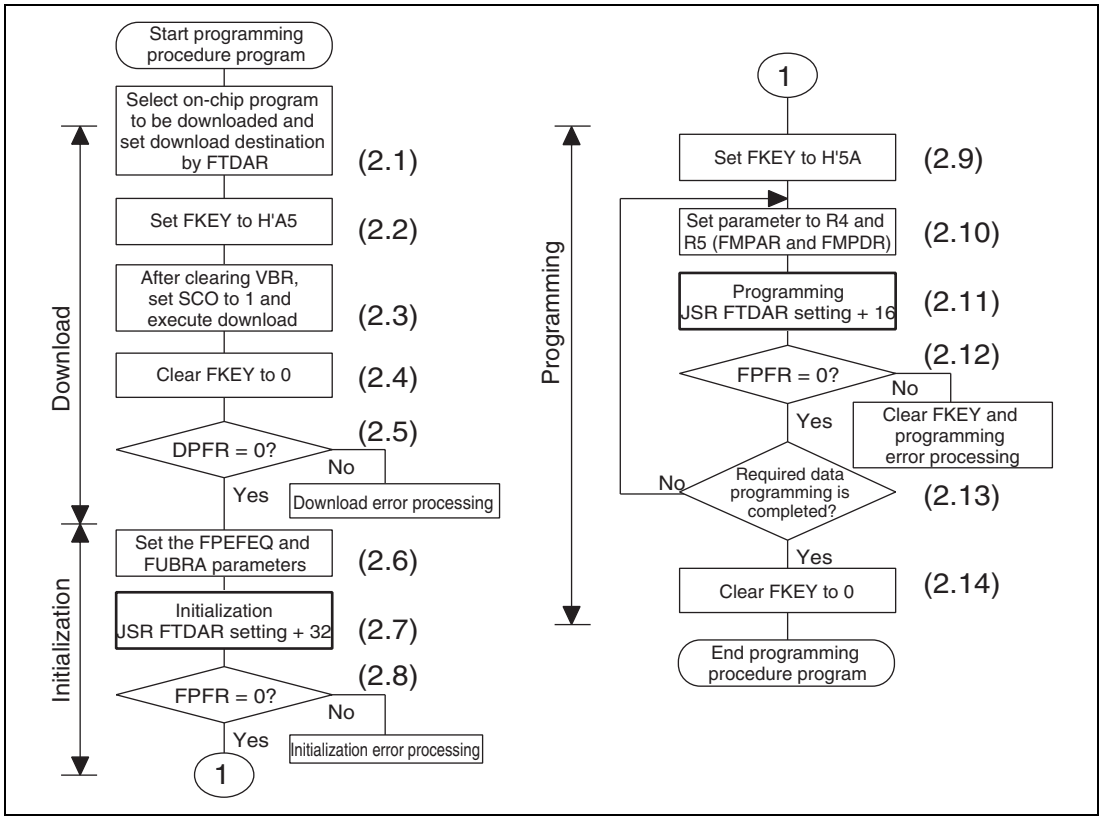


Figure 17.11 Programming Procedure

The details of the programming procedure are described below. The procedure program must be executed in an area other than the flash memory to be programmed. Especially the part where the SCO bit in FCCS is set to 1 for downloading must be executed in the on-chip RAM.

Specify 1/4 (initial value) as the frequency division ratios of an internal clock (Iϕ), a bus clock (Bϕ), and a peripheral clock (Pϕ) through the frequency control register (FRQCR).

After the programming/erasing program has been downloaded and the SCO bit is cleared to 0, the setting of the frequency control register (FRQCR) can be changed to the desired value. The following description assumes the area to be programmed on the user MAT is erased and program data is prepared in the consecutive area. When erasing has not been executed, carry out erasing before writing.

parameter FPFR. Since the unit is 128 bytes, the lower eight bits (MOA7 to MOA0) must be in the 128-byte boundary of H'00 or H'80.

- FMPDR setting

  If the storage destination of the program data is flash memory, even when the program execution routine is executed, programming is not executed and an error is returned to the FPFR parameter. In this case, the program data must be transferred to on-chip RAM and then programming must be executed.

(2.11) Programming

There is an entry point of the programming program in the area from (download start address set by FTDAR) + 16 bytes of on-chip RAM. The subroutine is called and programming is executed by using the following steps.

```
MOV.L  #DLTOP+16,R1          ; Set entry address to R1
JSR    @R1                   ; Call programming routine
NOP
```

— The general registers other than R0 are saved in the programming program.

— R0 is a return value of the FPFR parameter.

— Since the stack area is used in the programming program, a stack area of maximum 128 bytes must be reserved in RAM.

(2.12) The return value in the programming program, FPFR (general register R0) is checked.

(2.13) Determine whether programming of the necessary data has finished.

If more than 128 bytes of data are to be programmed, specify FMPAR and FMPDR in 128-byte units, and repeat steps (2.10) to (2.13). Increment the programming destination address by 128 bytes and update the programming data pointer correctly. If an address which has already been programmed is written to again, not only will a programming error occur, but also flash memory will be damaged.

(2.14) After programming finishes, clear FKEY and specify software protection.

If this LSI is restarted by a power-on reset immediately after user MAT programming has finished, secure a reset period (period of $\overline{RES}$ = 0) that is at least as long as the normal 100 µs.

17.9 Off-Board Programming Mode

A PROM programmer can be used to perform programming/erasing via a socket adapter. Use a PROM programmer that supports the proprietary Renesas specification.

Note that before using a PROM programmer to program the MCU, the MAT should initially be erased completely.

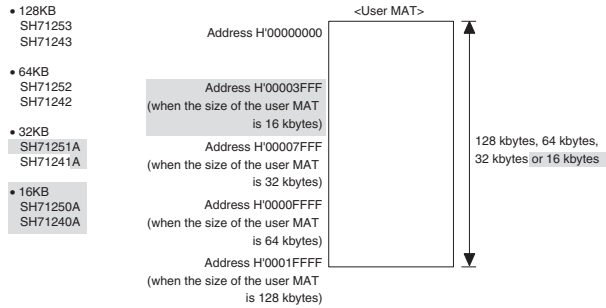
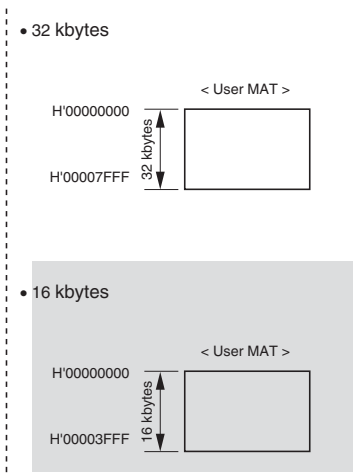
19.3.4 Standby Control Register 4 (STBCR4)

STBCR4 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	-	MSTP22	MSTP21	-	-	-	MSTP17	MSTP16
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
6	MSTP22	1	R/W	Module Stop Bit 22 When this bit is set to 1, the supply of the clock to the MTU2 is halted. 0: MTU2 operates 1: Clock supply to MTU2 halted
5	MSTP21	1	R/W	Module Stop Bit 21 When this bit is set to 1, the supply of the clock to the CMT is halted. 0: CMT operates 1: Clock supply to CMT halted
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
1	MSTP17	1	R/W	Module Stop Bit 17 When this bit is set to 1, the supply of the clock to the A/D_1 is halted. 0: A/D_1 operates 1: Clock supply to A/D_1 halted

Register Abbreviation	Power-on reset	Manual reset	Software Standby	Module Standby	Sleep	Module
TSR_1	Initialized	Retained	Initialized	Initialized	Retained	MTU2
TCNT_1	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_1	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_1	Initialized	Retained	Initialized	Initialized	Retained	
TICCR	Initialized	Retained	Initialized	Initialized	Retained	
TCR_2	Initialized	Retained	Initialized	Initialized	Retained	
TMDR_2	Initialized	Retained	Initialized	Initialized	Retained	
TIOR_2	Initialized	Retained	Initialized	Initialized	Retained	
TIER_2	Initialized	Retained	Initialized	Initialized	Retained	
TSR_2	Initialized	Retained	Initialized	Initialized	Retained	
TCNT_2	Initialized	Retained	Initialized	Initialized	Retained	
TGRA_2	Initialized	Retained	Initialized	Initialized	Retained	
TGRB_2	Initialized	Retained	Initialized	Initialized	Retained	
TCNTU_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRU_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRU_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORU_5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTV_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRV_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRV_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORV_5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTW_5	Initialized	Retained	Initialized	Initialized	Retained	
TGRW_5	Initialized	Retained	Initialized	Initialized	Retained	
TCRW_5	Initialized	Retained	Initialized	Initialized	Retained	
TIORW_5	Initialized	Retained	Initialized	Initialized	Retained	
TSR_5	Initialized	Retained	Initialized	Initialized	Retained	
TIER_5	Initialized	Retained	Initialized	Initialized	Retained	
TSTR5	Initialized	Retained	Initialized	Initialized	Retained	
TCNTCMPCLR	Initialized	Retained	Initialized	Initialized	Retained	

Item	Page	Revision (See Manual for Details)
17.2.4 Flash Memory Configuration Figure 17.3 Flash Memory Configuration	584	Figure amended 
17.2.5 Block Division	584	Description amended It is not divided on the 32 Kbyte versions of the SH71251A and SH71241A or the 16 Kbyte versions of the SH71250A and SH71240A.
Figure 17.4 Block Division of User MAT	584	Figure amended 
17.9 Off-Board Programming Mode	662	Description amended A PROM programmer can be used to perform programming/erasing via a socket adapter. Use a PROM programmer that supports the proprietary Renesas specification. Note that before using a PROM programmer to program the MCU, the MAT should initially be erased completely.