Renesas Electronics America Inc - DF71250AN50FPV Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250an50fpv

Section 4 Clock Pulse Generator (CPG)

This LSI has a clock pulse generator (CPG) that generates an internal clock (Iϕ), a bus clock (Bϕ), a peripheral clock (Pϕ), and a clock (MPϕ) for the MTU2 module. The CPG also controls power-down modes.

4.1 Features

- Five clocks generated independently

  An internal clock (Iϕ) for the CPU; a peripheral clock (Pϕ) for the on-chip peripheral modules; a bus clock (Bϕ = CK) for the external bus interface; and a MTU2 clock (MPϕ) for the on-chip MTU2 module.
- Frequency change function

  Frequencies of the internal clock (Iϕ), bus clock (Bϕ), peripheral clock (Pϕ), and MTU2 clock (MPϕ) can be changed independently using the divider circuit within the CPG. Frequencies are changed by software using the frequency control register (FRQCR) setting.
- Power-down mode control

  The clock can be stopped in sleep mode and standby mode and specific modules can be stopped using the module standby function.
- Oscillation stop detection

  If the clock supplied through the clock input pin stops for any reason, the timer pins can be automatically placed in the high-impedance state.

6.6 Interrupt Operation

6.6.1 Interrupt Sequence

The sequence of interrupt operations is explained below. Figure 6.3 is a flowchart of the operations.

1. The interrupt request sources send interrupt request signals to the interrupt controller.
2. The interrupt controller selects the highest priority interrupt from interrupt requests sent, according to the priority levels set in interrupt priority registers A to F and H to M (IPRA to IPRF and IPRH to IPRM). Interrupts that have lower-priority than that of the selected interrupt are ignored*. If interrupts that have the same priority level or interrupts within a same module occur simultaneously, the interrupt with the highest priority is selected according to the default priority shown in table 6.3.
3. The interrupt controller compares the priority level of the selected interrupt request with the interrupt mask bits (I3 to I0) in the status register (SR) of the CPU. If the priority level of the selected request is equal to or less than the level set in bits I3 to I0, the request is ignored. If the priority level of the selected request is higher than the level in bits I3 to I0, the interrupt controller accepts the request and sends an interrupt request signal to the CPU.
4. When the interrupt controller accepts an interrupt, a low level is output from the $\overline{\text{IRQOUT}}$ pin.
5. The CPU detects the interrupt request sent from the interrupt controller in the decode stage of an instruction to be executed. Instead of executing the decoded instruction, the CPU starts interrupt exception handling.
6. SR and PC are saved onto the stack.
7. The priority level of the accepted interrupt is copied to bits (I3 to I0) in SR.
8. When the accepted interrupt is sensed by level or is from an on-chip peripheral module, a high level is output from the $\overline{\text{IRQOUT}}$ pin. When the accepted interrupt is sensed by edge, a high level is output from the $\overline{\text{IRQOUT}}$ pin at the moment when the CPU starts interrupt exception processing instead of instruction execution as noted in 5. above. However, if the interrupt controller accepts an interrupt with a higher priority than the interrupt just to be accepted, the $\overline{\text{IRQOUT}}$ pin holds low level.
9. The CPU reads the start address of the exception handling routine from the exception vector table for the accepted interrupt, branches to that address, and starts executing the program. This branch is not a delayed branch.

7.4 Usage Notes

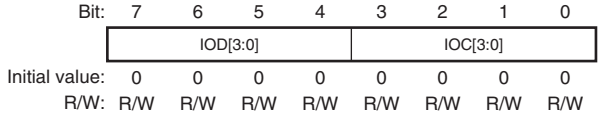
1. The CPU can read from or write to the UBC registers via the I bus. Accordingly, during the period from executing an instruction to rewrite the UBC register till the new value is actually rewritten, the desired break may not occur. In order to know the timing when the UBC register is changed, read from the last written register. Instructions after then are valid for the newly written register value.
2. UBC cannot monitor access to the L bus and I bus in the same channel.
3. Note on specification of sequential break:

   A condition match occurs when a B-channel match occurs in a bus cycle after an A-channel match occurs in another bus cycle in sequential break setting. Therefore, no break occurs even if a bus cycle, in which an A-channel match and a channel B match occur simultaneously, is set.
4. When a user break and another exception occur at the same instruction, which has higher priority is determined according to the priority levels defined in table 5.1 in section 5, Exception Handling. If an exception with higher priority occurs, the user break is not generated.
   - Pre-execution break has the highest priority.
   - When a post-execution break or data access break occurs simultaneously with a re-execution-type exception (including pre-execution break) that has higher priority, the re-execution-type exception is accepted, and the condition match flag is not set (see the exception in the following note). The break will occur and the condition match flag will be set only after the exception source of the re-execution-type exception has been cleared by the exception handling routine and re-execution of the same instruction has ended.
   - When a post-execution break or data access break occurs simultaneously with a completion-type exception (TRAPA) that has higher priority, though a break does not occur, the condition match flag is set.
5. Note the following exception for the above note.

   If a post-execution break or data access break is satisfied by an instruction that generates a CPU address error by data access, the CPU address error is given priority to the break. Note that the UBC condition match flag is set in this case.
6. Note the following when a break occurs in a delay slot.

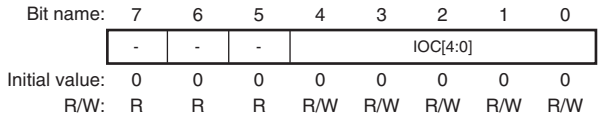
   If a pre-execution break is set at the delay slot instruction of the RTE instruction, the break does not occur until the branch destination of the RTE instruction.
7. User breaks are disabled during UBC module standby mode. Do not read from or write to the UBC registers during UBC module standby mode; the values are not guaranteed.

- TIORL_0, TIORL_3, TIORL_4



Bit	Bit Name	Initial Value	R/W	Description
7 to 4	IOD[3:0]	0000	R/W	I/O Control D0 to D3 Specify the function of TGRD. See the following tables. TIORL_0: Table 9.13 TIORL_3: Table 9.17 TIORL_4: Table 9.19
3 to 0	IOC[3:0]	0000	R/W	I/O Control C0 to C3 Specify the function of TGRC. See the following tables. TIORL_0: Table 9.21 TIORL_3: Table 9.25 TIORL_4: Table 9.27

- TIORU_5, TIORV_5, TIORW_5



Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	IOC[4:0]	00000	R/W	I/O Control C0 to C4 Specify the function of TGRU_5, TGRV_5, and TGRW_5. For details, see table 9.28.

7. PWM Cycle Setting

In complementary PWM mode, the PWM pulse cycle is set in two registers—TGRA_3, in which the TCNT_3 upper limit value is set, and TCDR, in which the TCNT_4 upper limit value is set. The settings should be made so as to achieve the following relationship between these two registers:

With dead time: TGRA_3 set value = TCDR set value + TDDR set value
Without dead time: TGRA_3 set value = TCDR set value + 1

The TGRA_3 and TCDR settings are made by setting the values in buffer registers TGRC_3 and TCBR. The values set in TGRC_3 and TCBR are transferred simultaneously to TGRA_3 and TCDR in accordance with the transfer timing selected with bits MD3 to MD0 in the timer mode register (TMDR).

The updated PWM cycle is reflected from the next cycle when the data update is performed at the crest, and from the current cycle when performed in the trough. Figure 9.42 illustrates the operation when the PWM cycle is updated at the crest.

See the following section, Register Data Updating, for the method of updating the data in each buffer register.

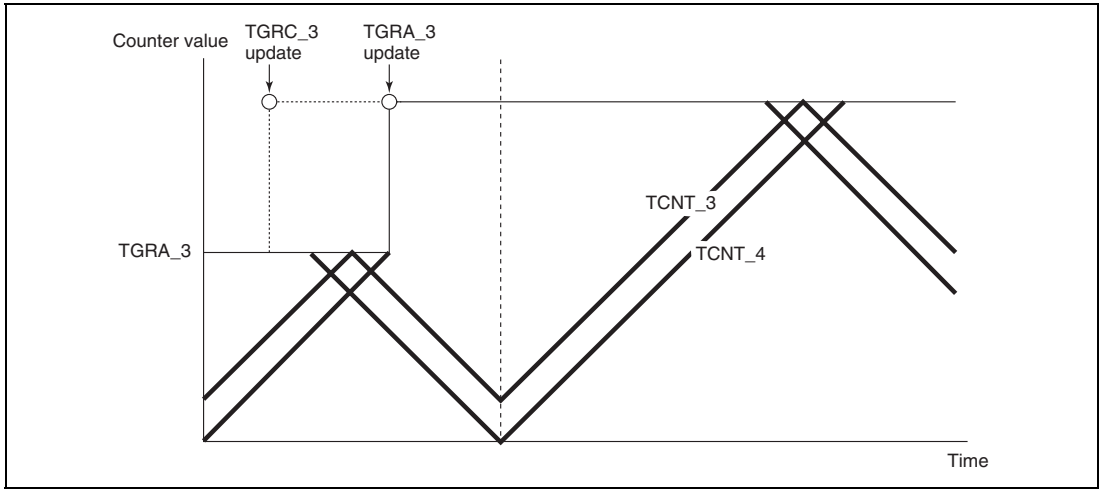


Figure 9.42 Example of PWM Cycle Updating

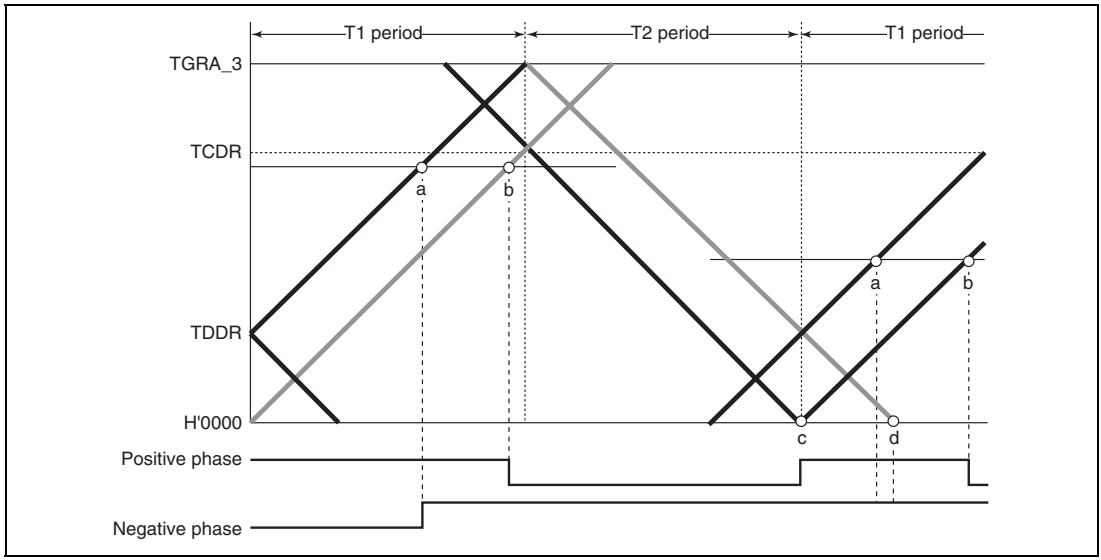


Figure 9.50 Example of Complementary PWM Mode 0% and 100% Waveform Output (2)

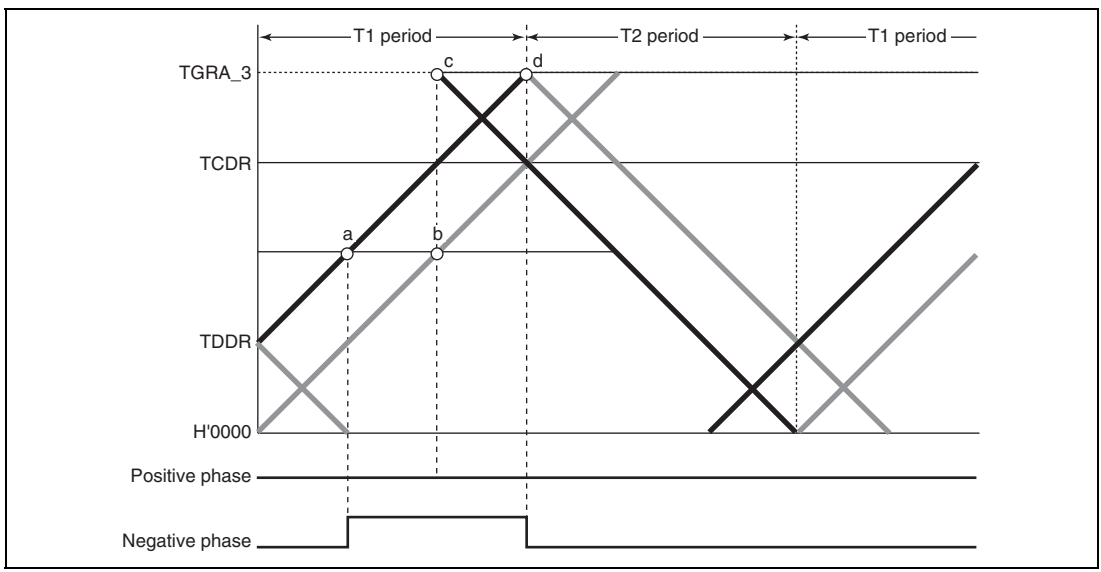


Figure 9.51 Example of Complementary PWM Mode 0% and 100% Waveform Output (3)

10.2 Input/Output Pins

Table 10.1 Pin Configuration

Name	Abbreviation	I/O	Description
Port output enable input pins 0, 1, 3	$\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$*	Input	Input request signals to place high-current pins for MTU2 in high-impedance state*
Port output enable input pin 8	$\overline{\text{POE8}}$	Input	Inputs a request signal to place pins for channel 0 in MTU2 in high-impedance state*

Note: * When the $\overline{\text{POE3}}$ function is selected in the PFC, the pin is pulled up inside the LSI if nothing is input to it. The $\overline{\text{POE3}}$ pin is supported only by the SH7125.

Table 10.2 shows output-level comparisons with pin combinations.

Table 10.2 Pin Combinations

Pin Combination	I/O	Description
PE9/TIOC3B and PE11/TIOC3D	Output	The high-current pins for the MTU2 are placed in high-impedance state when the pins simultaneously output an active level (low level when the output level select P (OLSP) bit of the timer output control register (TOCR) in the MTU2 is 0 or high level when the bit is 1) for one or more cycles of the peripheral clock (Pϕ). This active level comparison is done when the MTU2 output function or general output function is selected in the pin function controller. If another function is selected, the output level is not checked. Pin combinations for output comparison and high-impedance control can be selected by POE registers.
PE12/TIOC4A and PE14/TIOC4C		
PE13/TIOC4B and PE15/TIOC4D		

12.2 Input/Output Pins

The SCI has the serial pins summarized in table 12.1.

Table 12.1 Pin Configuration

Channel	Pin Name*[1]	I/O	Function
0	SCK0	I/O	SCI0 clock input/output
	RXD0	Input	SCI0 receive data input
	TXD0	Output	SCI0 transmit data output
1	SCK1*[2]	I/O	SCI1 clock input/output
	RXD1	Input	SCI1 receive data input
	TXD1	Output	SCI1 transmit data output
2	SCK2	I/O	SCI2 clock input/output
	RXD2	Input	SCI2 receive data input
	TXD2	Output	SCI2 transmit data output

Notes: 1. Pin names SCK, RXD, and TXD are used in the description for all channels, omitting the channel designation.

2. This pin is supported only by the SH7125. Channel 1 in the SH7124 is only for asynchronous mode.

12.4.4 Multiprocessor Communication Function

Use of the multiprocessor communication function enables data transfer to be performed among a number of processors sharing communication lines by means of asynchronous serial communication using the multiprocessor format, in which a multiprocessor bit is added to the transfer data. When multiprocessor communication is carried out, each receiving station is addressed by a unique ID code. The serial communication cycle consists of two component cycles: an ID transmission cycle that specifies the receiving station, and a data transmission cycle. The multiprocessor bit is used to differentiate between the ID transmission cycle and the data transmission cycle. If the multiprocessor bit is 1, the cycle is an ID transmission cycle, and if the multiprocessor bit is 0, the cycle is a data transmission cycle. Figure 12.15 shows an example of inter-processor communication using the multiprocessor format. The transmitting station first sends the ID code of the receiving station with which it wants to perform serial communication as data with a 1 multiprocessor bit added. It then sends transmit data as data with a 0 multiprocessor bit added. The receiving station skips data until data with a 1 multiprocessor bit is sent. When data with a 1 multiprocessor bit is received, the receiving station compares that data with its own ID. The station whose ID matches then receives the data sent next. Stations whose ID does not match continue to skip data until data with a 1 multiprocessor bit is again received.

The SCI uses the MPIE bit in SCSCR to implement this function. When the MPIE bit is set to 1, transfer of receive data from SCRSR to SCRDR, error flag detection, and setting the SCSSR status flags, RDRF, FER, and OER to 1 are inhibited until data with a 1 multiprocessor bit is received. On reception of receive character with a 1 multiprocessor bit, the MPB bit in SCSSR is set to 1 and the MPIE bit is automatically cleared, thus normal reception is resumed. If the RIE bit in SCSCR is set to 1 at this time, an RXI interrupt is generated.

When the multiprocessor format is selected, the parity bit setting is invalid. All other bit settings are the same as those in normal asynchronous mode. The clock used for multiprocessor communication is the same as that in normal asynchronous mode.

14.4 Interrupts

14.4.1 CMT Interrupt Sources

The CMT has channels and each of them to which a different vector address is allocated has compare match interrupt. When both the interrupt request flag (CMF) and interrupt enable bit (CMIE) are set to 1, the corresponding interrupt request is output. When the interrupt is used to activate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 6, Interrupt Controller (INTC).

14.4.2 Timing of Setting Compare Match Flag

When CMCOR and CMCNT match, a compare match signal is generated and the CMF bit in CMCSR is set to 1. The compare match signal is generated in the last cycle in which the values match (when the CMCNT value is updated to H'0000). That is, after a match between CMCOR and CMCNT, the compare match signal is not generated until the next CMCNT counter clock input. Figure 14.4 shows the timing of CMF bit setting.

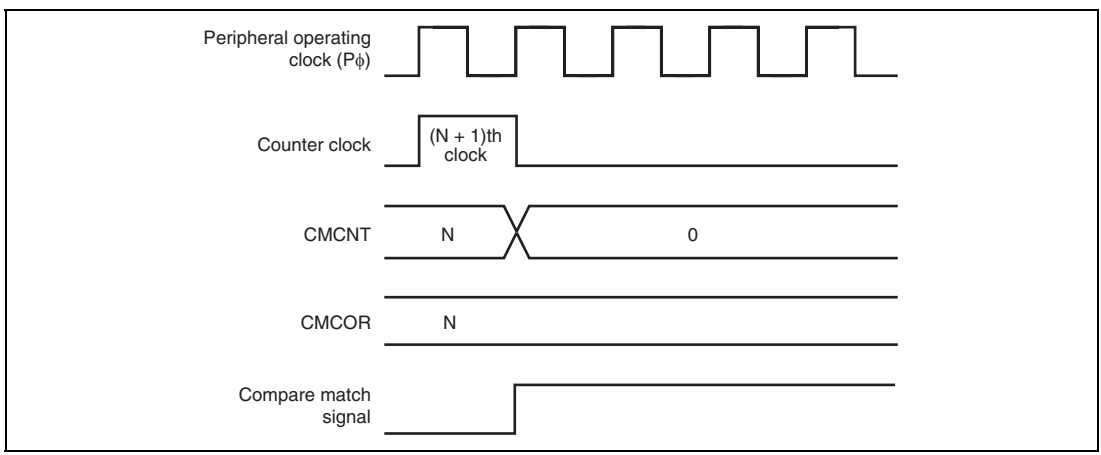


Figure 14.4 Timing of CMF Setting

14.4.3 Timing of Clearing Compare Match Flag

The CMF bit in CMCSR is cleared by reading 1 from this bit, then writing 0.

17.3 Input/Output Pins

Flash memory is controlled by the pins as shown in table 17.3.

Table 17.3 Pin Configuration

Pin Name	Symbol	I/O	Function
Power-on reset	$\overline{\text{RES}}$	Input	Reset
Flash programming enable	FWE	Input	Hardware protection when programming flash memory
Mode 1	MD1	Input	Sets operating mode of this LSI
Transmit data	TXD1 (PA4)	Output	Serial transmit data output (used in boot mode)
Receive data	RXD1 (PA3)	Input	Serial receive data input (used in boot mode)

17.4 Register Descriptions

17.4.1 Registers

The registers/parameters, which control flash memory when the on-chip flash memory is valid are shown in table 17.4.

There are several operating modes for accessing flash memory, for example, read mode/program mode. The correspondence of operating modes and registers/parameters for use is shown in table 17.5.

(2.3) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter indicates the return value of the initialization result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	-	-	-	BR	FQ	SF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	Undefined	R/W	Unused Return 0.
2	BR	Undefined	R/W	User Branch Error Detect Returns the check result whether the specified user branch destination address is in the area other than the storage area of the programming/erasing program which has been downloaded. 0: User branch address setting is normal 1: User branch address setting is abnormal
1	FQ	Undefined	R/W	Frequency Error Detect Returns the check result whether the specified operating frequency of the CPU is in the range of the supported operating frequency. 0: Setting of operating frequency is normal 1: Setting of operating frequency is abnormal
0	SF	Undefined	R/W	Success/Fail Indicates whether initialization is completed normally. 0: Initialization has ended normally (no error) 1: Initialization has ended abnormally (error occurs)

(1) SCI Interface Setting by Host

When boot mode is initiated, this LSI measures the low period of asynchronous SCI-communication data (H'00), which is transmitted consecutively by the host. The SCI transmit/receive format is set to 8-bit data, 1 stop bit, and no parity. This LSI calculates the bit rate of transmission by the host by means of the measured low period and transmits the bit adjustment end sign (1 byte of H'00) to the host. The host must confirm that this bit adjustment end sign (H'00) has been received normally and transmits 1 byte of H'55 to this LSI. When reception is not executed normally, boot mode is initiated again (reset) and the operation described above must be executed. The bit rate between the host and this LSI is not matched because of the bit rate of transmission by the host and system clock frequency of this LSI. To operate the SCI normally, the transfer bit rate of the host must be set to 9,600 bps or 19,200 bps.

The system clock frequency, which can automatically adjust the transfer bit rate of the host and the bit rate of this LSI is shown in table 17.7. Boot mode must be initiated in the range of this system clock. Note that the internal clock division ratio of ×1/3 is not supported in boot mode.

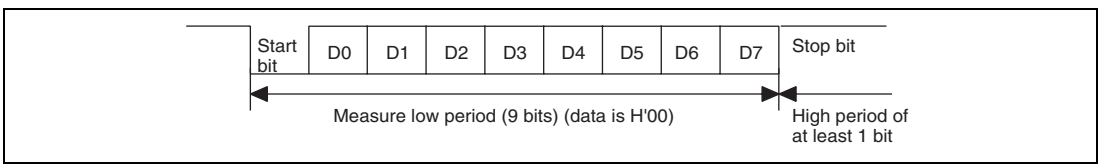


Figure 17.7 Automatic Adjustment Operation of SCI Bit Rate

Table 17.7 Peripheral Clock (Pϕ) Frequency that Can Automatically Adjust Bit Rate of This LSI

Host Bit Rate	Peripheral Clock (Pϕ) Frequency Which Can Automatically Adjust LSI's Bit Rate
9,600 bps	20 to 25 MHz
19,200 bps	20 to 25 MHz

Note: The internal clock division ratio of ×1/3 is not supported in boot mode.

Table 17.15 Error Codes

Code	Description
H'00	No error
H'11	Sum check error
H'21	Non-matching device code error
H'22	Non-matching clock mode error
H'24	Bit-rate selection failure
H'25	Input frequency error
H'26	Frequency multiplier error
H'27	Operating frequency error
H'29	Block number error
H'2A	Address error
H'2B	Data length error (size error)
H'51	Erasure error
H'52	Non-erased error
H'53	Programming error
H'54	Selection processing error
H'80	Command error
H'FF	Bit-rate matching acknowledge error

17.8.2 Areas for Storage of the Procedural Program and Data for Programming

In the descriptions in the previous section, storable areas for the programming/erasing procedure programs and program data are assumed to be in on-chip RAM. However, the procedure programs and data can be executed in other areas as long as the following conditions are satisfied.

1. The on-chip programming/erasing program is downloaded from the address set by FTDAR in on-chip RAM, therefore, this area is not available for use.
2. The on-chip programming/erasing program will use 128 bytes or more as a stack. Make sure this area is reserved.
3. Since download by setting the SCO bit to 1 will cause the MATs to be switched, it should be executed in on-chip RAM.
4. The flash memory is accessible until the start of programming or erasing, that is, until the result of downloading has been decided. When in a mode in which the external address space is not accessible, such as single-chip mode, the required procedure programs, interrupt vector

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ADCSR_1	ADF	ADIE	—	—	TRGE	—	CONADF	STC	A/D (Channel 1)
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_1	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
FCCS	FWE	—	—	FLER	—	—	—	SCO	FLASH
FPCS	—	—	—	—	—	—	—	PPVS	
FECS	—	—	—	—	—	—	—	EPVB	
FKEY	K[7:0]								
FTDAR	TDER	TDA[6:0]							
CMSTR	—	—	—	—	—	—	—	—	CMT
	—	—	—	—	—	—	STR1	STR0	
CMCSR_0	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_0									
CMCOR_0									
CMCSR_1	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_1									
CMCOR_1									
ICSR1	POE3F	—	POE1F	POE0F	—	—	—	PIE1	POE
	POE3M[1:0]		—	—	POE1M[1:0]		POE0M[1:0]		
OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1	
	—	—	—	—	—	—	—	—	
ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3	
	—	—	—	—	—	—	POE8M[1:0]		
SPOER	—	—	—	—	—	—	MTU2CH0HIZ	MTU2CH34HIZ	

21.3.1 Clock Timing

Table 21.5 Clock Timing

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = -20$ to +85°C (consumer specifications),
$T_a = -40$ to +85°C (industrial specifications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
EXTAL clock input frequency	f_{EX}	10	12.5	MHz	Figure 21.1
EXTAL clock input cycle time	t_{EXcyc}	80	100	ns	
EXTAL clock input low pulse width	t_{EXL}	20	—	ns	
EXTAL clock input high pulse width	t_{EXH}	20	—	ns	
EXTAL clock input rising time	t_{EXr}	—	5	ns	
EXTAL clock input falling time	t_{EXf}	—	5	ns	
CK (Bϕ) clock frequency (reference values)	f_{OP}	10	40	MHz	*
CK (Bϕ) clock cycle time (reference values)	t_{cyc}	25	100	ns	
Power-on oscillation stabilization time	t_{OSC1}	10	—	ms	Figure 21.2
Oscillation stabilization time on return from standby 1	t_{OSC2}	10	—	ms	Figure 21.3
Oscillation stabilization time on return from standby 2	t_{OSC3}	10	—	ms	Figure 21.4

Note: * Depends on the frequency control register (FRQCR).

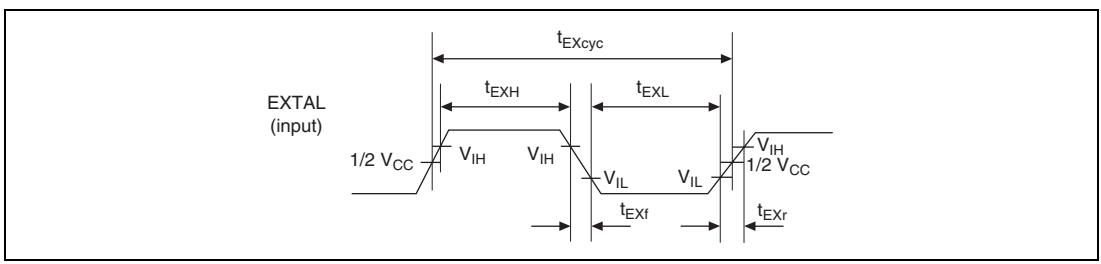


Figure 21.1 Timing of EXTAL Input Clock Signal

21.3.5 Watchdog Timer (WDT) Timing

Table 21.9 Watchdog Timer (WDT) Timing

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = -20$ to +85°C (consumer specifications),
$T_a = -40$ to +85°C (industrial specifications)

Item	Symbol	Min.	Max.	Unit	Reference Figure
$\overline{\text{WDTOVF}}$ delay time (reference values)	t_{WOVD}	—	50	ns	Figure 21.11

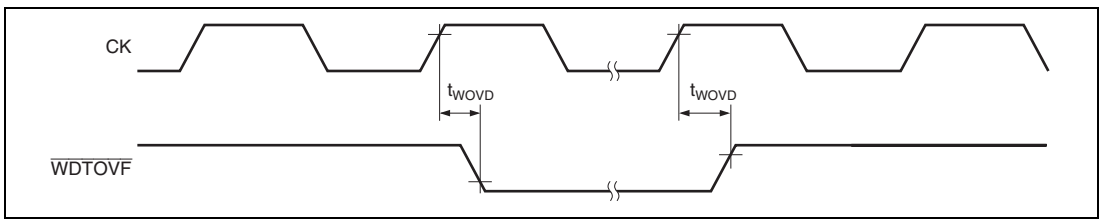
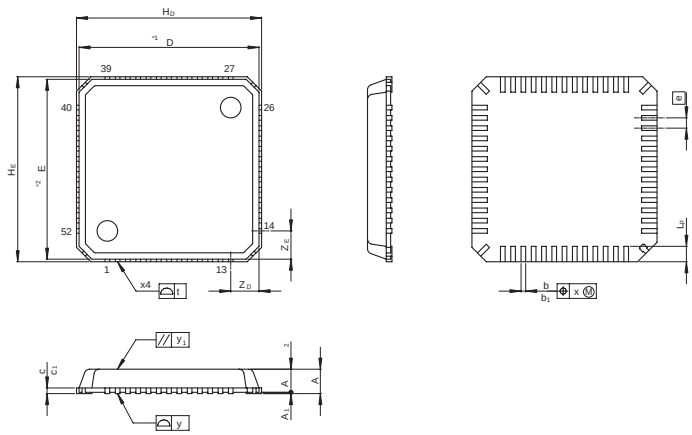


Figure 21.11 WDT Timing

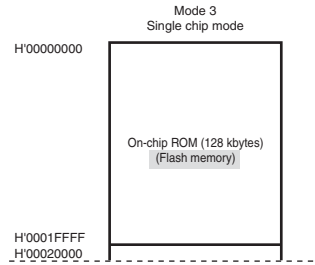
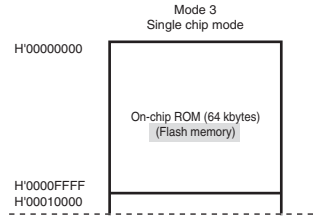
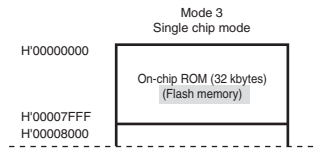
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VQFN52-7x7-0.40	PVQN0052LE-A	-	0.095g

NOTE)
1. DIMENSIONS"*1"AND"*2"
DO NOT INCLUDE MOLD FLASH.



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
A_2	—	0.89	—
A	—	—	0.95
A_1	0.005	0.02	0.04
b	0.13	0.18	0.23
b_1	—	0.16	—
e	—	0.4	—
L_p	0.50	0.60	0.70
x	—	—	0.05
y	—	—	0.05
y_1	—	—	0.20
t	—	—	0.20
H_D	—	7.2	—
H_E	—	7.2	—
Z_D	—	1.1	—
Z_E	—	1.1	—
c	0.17	0.22	0.25
c_1	—	0.20	—

Figure C.5 VQFN-52

Item	Page	Revision (See Manual for Details)
3.1 Selection of Operating Modes Table 3.1 Selection of Operating Modes	49	Table amended Pin Setting / On-Chip ROM Mode No. / FWE / MD1 / Mode Name / (Flash memory) Note added Note: 2. Prohibited in SH71251A, SH71250A, SH71241A and SH71240A.
3.4 Address Map Figure 3.1 Address Map in SH7125, SH7124 (128 Kbytes Flash Memory Version)	51	Figure amended 
Figure 3.2 Address Map in SH7125, SH7124 (64 Kbytes Flash Memory Version)	52	Figure amended 
Figure 3.3 Address Map in SH71251A and SH71241A (32 Kbytes Flash Memory Version)	53	Figure amended 
Figure 3.4 Address Map in SH71250A and SH71240A (16 Kbytes Flash Memory Version)	54	Figure added