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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71250an50npv

4.6 Oscillator

Clock pulses can be supplied from a connected crystal resonator or an external clock.

4.6.1 Connecting Crystal Resonator

A crystal resonator can be connected as shown in figure 4.2. Use the damping resistance (Rd) listed in table 4.6. Use a crystal resonator that has a resonance frequency of 10 to 12.5 MHz. It is recommended to consult the crystal resonator manufacturer concerning the compatibility of the crystal resonator and the LSI.

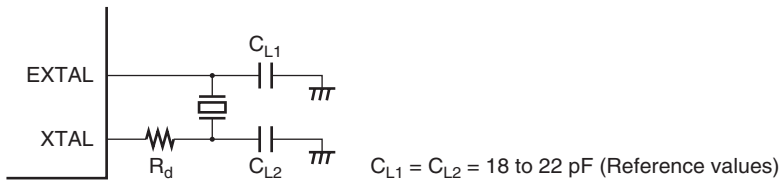


Figure 4.2 Connection of Crystal Resonator (Example)

Table 4.6 Damping Resistance Values (Reference Values)

Frequency (MHz)	10	12.5
Rd (Ω) (Reference Values)	0	0

Figure 4.3 shows an equivalent circuit of the crystal resonator. Use a crystal resonator with the characteristics listed in table 4.7.

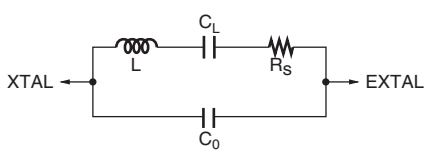
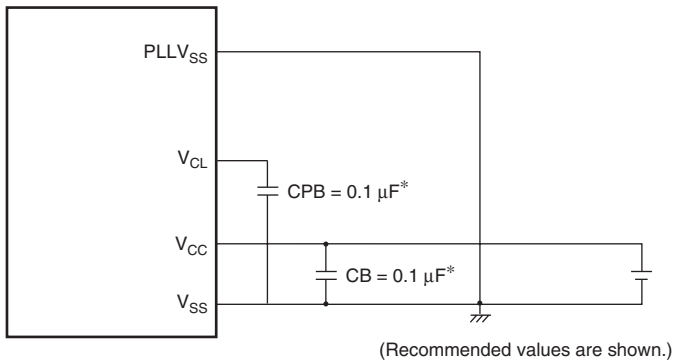


Figure 4.3 Crystal Resonator Equivalent Circuit

A circuitry shown in figure 4.6 is recommended as an external circuitry around the PLL. Separate the PLL power lines (PLLVss) and the system power lines (Vcc, Vss) at the board power supply source, and be sure to insert bypass capacitors CB and CPB close to the pins.



Note: * CB and CPB are laminated ceramic type.

Figure 4.6 Recommended External Circuitry around PLL

Bit	Bit Name	Initial Value	R/W	Description
3	IRQ11S	0	R/W	IRQ1 Sense Select
2	IRQ10S	0	R/W	Set the interrupt request detection mode for pin IRQ1. 00: Interrupt request is detected at the low level of pin IRQ1 01: Interrupt request is detected at the falling edge of pin IRQ1 10: Interrupt request is detected at the rising edge of pin IRQ1 11: Interrupt request is detected at both the falling and rising edges of pin IRQ1
1	IRQ01S	0	R/W	IRQ0 Sense Select (SH7125)
0	IRQ00S	0	R/W	Set the interrupt request detection mode for pin IRQ0. 00: Interrupt request is detected at the low level of pin IRQ0 01: Interrupt request is detected at the falling edge of pin IRQ0 10: Interrupt request is detected at the rising edge of pin IRQ0 11: Interrupt request is detected at both the falling and rising edges of pin IRQ0 Reserved (SH7124) These bits are always read as 0. The write value should always be 0.

Item	Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Interrupt sources	7 sources	4 sources	4 sources	5 sources	5 sources	3 sources
	• Compare match or input capture 0A	• Compare match or input capture 1A*2	• Compare match or input capture 2A*2	• Compare match or input capture 3A	• Compare match or input capture 4A	• Compare match or input capture 5U
	• Compare match or input capture 0B	• Compare match or input capture 1B*2	• Compare match or input capture 2B*2	• Compare match or input capture 3B	• Compare match or input capture 4B	• Compare match or input capture 5V
	• Compare match or input capture 0C	• Overflow • Underflow	• Overflow • Underflow	• Compare match or input capture 3C	• Compare match or input capture 4C	• Compare match or input capture 5W
	• Compare match or input capture 0D			• Compare match or input capture 3D	• Compare match or input capture 4D	
	• Compare match 0E			• Overflow	• Overflow or underflow	
	• Compare match 0F					
	• Overflow					

Bit	Bit Name	Initial Value	R/W	Description
0	ITB4VE	0*	R/W	TCIV_4 Interrupt Skipping Link Enable Select whether to link A/D converter start requests (TRG4BN) with TCIV_4 interrupt skipping operation. 0: Does not link with TCIV_4 interrupt skipping 1: Links with TCIV_4 interrupt skipping

Notes: 1. TADCR must not be accessed in eight bits; it should always be accessed in 16 bits.
2. When interrupt skipping is disabled (the T3AEN and T4VEN bits in the timer interrupt skipping set register (TITCR) are cleared to 0 or the skipping count set bits (3ACOR and 4VCOR) in TITCR are cleared to 0), do not link A/D converter start requests with interrupt skipping operation (clear the ITA3AE, ITA4VE, ITB3AE, and ITB4VE bits in the timer A/D converter start request control register (TADCR) to 0).
3. If link with interrupt skipping is enabled while interrupt skipping is disabled, A/D converter start requests will not be issued.
* Do not set to 1 when complementary PWM mode is not selected.

Table 9.29 Setting of Transfer Timing by BF1 and BF0 Bits

Bit 7	Bit 6	
BF1	BF0	Description
0	0	Does not transfer data from the cycle set buffer register to the cycle set register.
0	1	Transfers data from the cycle set buffer register to the cycle set register at the crest of the TCNT_4 count.*[1]
1	0	Transfers data from the cycle set buffer register to the cycle set register at the trough of the TCNT_4 count.*[2]
1	1	Transfers data from the cycle set buffer register to the cycle set register at the crest and trough of the TCNT_4 count.*[2]

Notes: 1. Data is transferred from the cycle set buffer register to the cycle set register when the crest of the TCNT_4 count is reached in complementary PWM mode, when compare match occurs between TCNT_3 and TGRA_3 in reset-synchronized PWM mode, or when compare match occurs between TCNT_4 and TGRA_4 in PWM mode 1 or normal operation mode.
2. These settings are prohibited when complementary PWM mode is not selected.

Bit	Bit Name	Initial Value	R/W	Description
2	SYNC2	0	R/W	Timer Synchronous operation 2 to 0
1	SYNC1	0	R/W	These bits are used to select whether operation is independent of or synchronized with other channels.
0	SYNC0	0	R/W	When synchronous operation is selected, the TCNT synchronous presetting of multiple channels, and synchronous clearing by counter clearing on another channel, are possible. To set synchronous operation, the SYNC bits for at least two channels must be set to 1. To set synchronous clearing, in addition to the SYNC bit, the TCNT clearing source must also be set by means of bits CCLR0 to CCLR2 in TCR. 0: TCNT_2 to TCNT_0 operates independently (TCNT presetting /clearing is unrelated to other channels) 1: TCNT_2 to TCNT_0 performs synchronous operation TCNT synchronous presetting/synchronous clearing is possible

Bit	Bit Name	Initial Value	R/W	Description
0	OE3B	0	R/W	Master Enable TIOC3B This bit enables/disables the TIOC3B pin MTU2 output. 0: MTU2 output is disabled (inactive level)* 1: MTU2 output is enabled

Note: * The inactive level is determined by the settings in timer output control registers 1 and 2 (TOCR1 and TOCR2). For details, refer to section 9.3.18, Timer Output Control Register 1 (TOCR1), and section 9.3.19, Timer Output Control Register 2 (TOCR2). Set these bits to 1 to enable MTU2 output in other than complementary PWM or reset-synchronized PWM mode. When these bits are set to 0, low level is output.

9.3.18 Timer Output Control Register 1 (TOCR1)

TOCR1 is an 8-bit readable/writable register that enables/disables PWM synchronized toggle output in complementary PWM mode/reset synchronized PWM mode, and controls output level inversion of PWM output.

Bit:	7	6	5	4	3	2	1	0
	-	PSYE	-	-	TOCL	TOCS	OLSN	OLSP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R/(W)*	R/W	R/W	R/W

Note: * This bit can be set to 1 only once after a power-on reset. After 1 is written, 0 cannot be written to the bit.

Bit	Bit Name	Initial value	R/W	Description
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PSYE	0	R/W	PWM Synchronous Output Enable This bit selects the enable/disable of toggle output synchronized with the PWM period. 0: Toggle output is disabled 1: Toggle output is enabled
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Examples of Phase Counting Mode Operation: In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

1. Phase counting mode 1

   Figure 9.30 shows an example of phase counting mode 1 operation, and table 9.48 summarizes the TCNT up/down-count conditions.

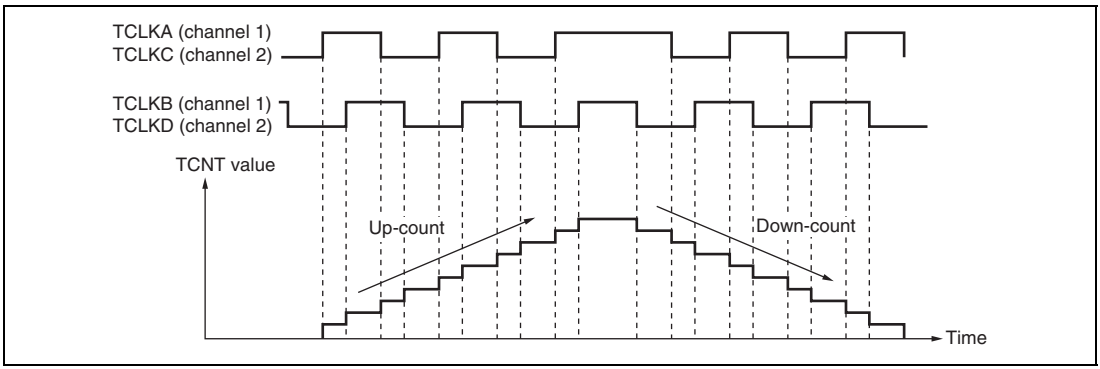


Figure 9.30 Example of Phase Counting Mode 1 Operation

Table 9.48 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

[Legend]

↑: Rising edge

↓: Falling edge

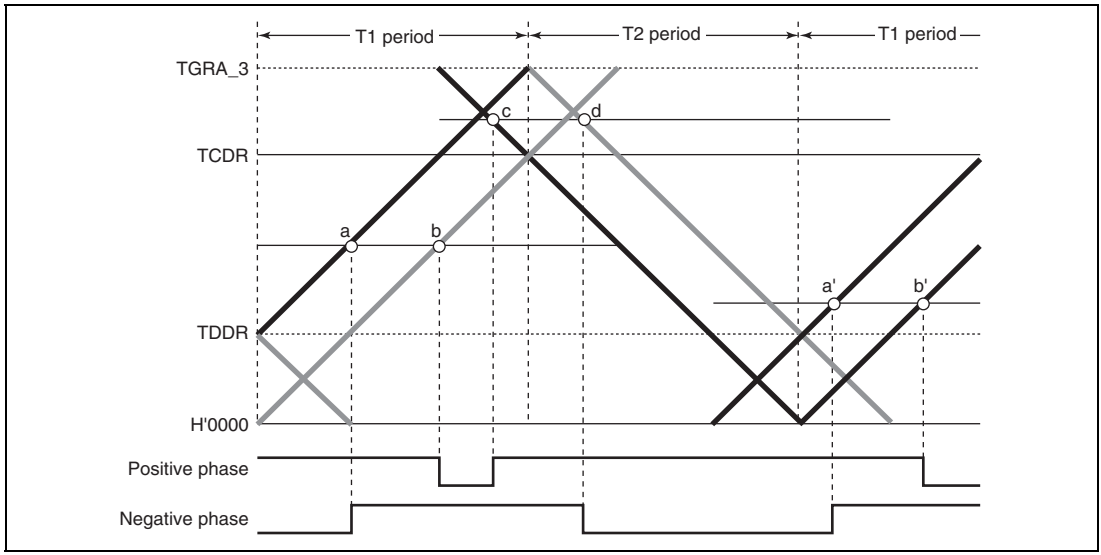


Figure 9.46 Example of Complementary PWM Mode Waveform Output (1)

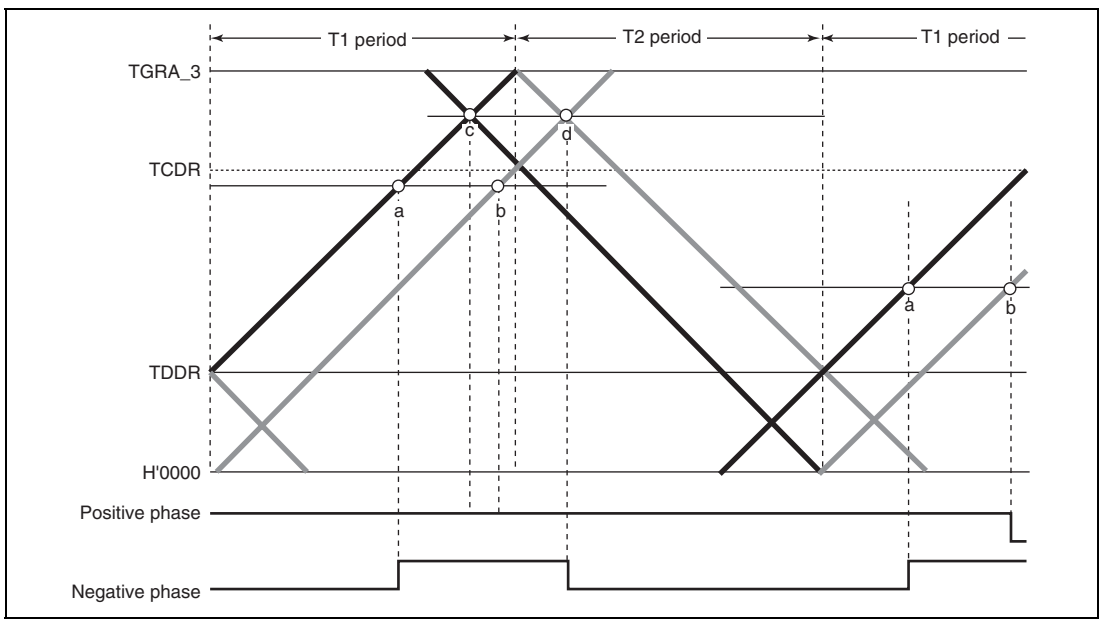


Figure 9.47 Example of Complementary PWM Mode Waveform Output (2)

9.7.13 Counter Value during Complementary PWM Mode Stop

When counting operation is suspended with TCNT_3 and TCNT_4 in complementary PWM mode, TCNT_3 has the timer dead time register (TDDR) value, and TCNT_4 is held at H'0000.

When restarting complementary PWM mode, counting begins automatically from the initialized state. This explanatory diagram is shown in figure 9.119.

When counting begins in another operating mode, be sure that TCNT_3 and TCNT_4 are set to the initial values.

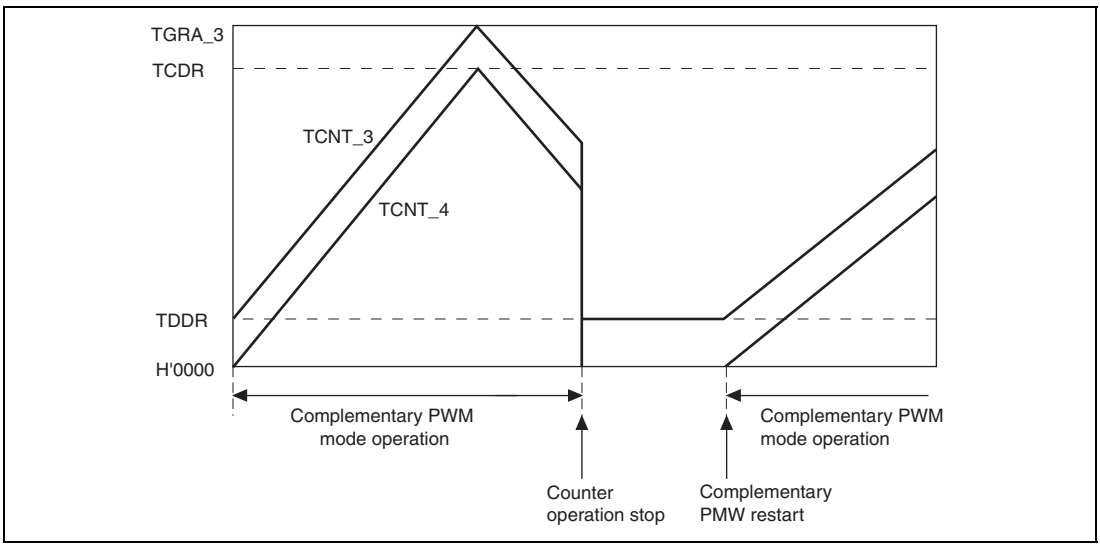


Figure 9.119 Counter Value during Complementary PWM Mode Stop

9.7.14 Buffer Operation Setting in Complementary PWM Mode

In complementary PWM mode, conduct rewrites by buffer operation for the PWM cycle setting register (TGRA_3), timer cycle data register (TCDR), and duty setting registers (TGRB_3, TGRA_4, and TGRB_4).

In complementary PWM mode, channel 3 and channel 4 buffers operate in accordance with bit settings BFA and BFB of TMDR_3. When the BFA bit in TMDR_3 is set to 1, TGRC_3 functions as a buffer register for TGRA_3. At the same time, TGRC_4 functions as the buffer register for TGRA_4, and TCBR functions as the TCDR's buffer register.

10.4.2 Output-Level Compare Operation

Figure 10.4 shows an example of the output-level compare operation for the combination of TIOC3B and TIOC3D. The operation is the same for the other pin combinations.

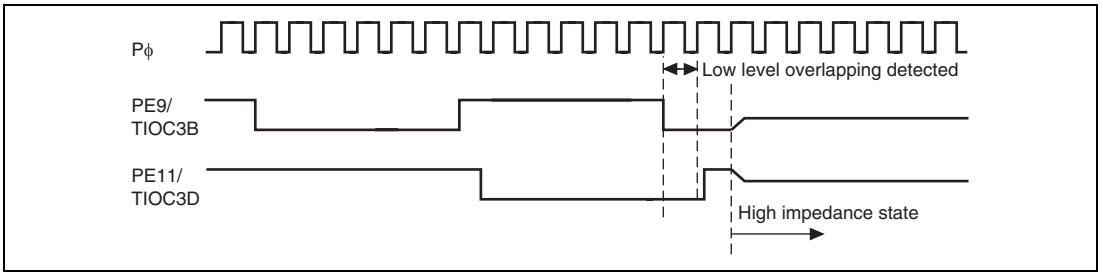


Figure 10.4 Output-Level Compare Operation

10.4.3 Release from High-Impedance State

High-current pins that have entered high-impedance state due to input-level detection can be released either by returning them to their initial state with a power-on reset, or by clearing all of the flags in bits 12 to 15 (POE0F to POE3F and POE8F) in ICSR1. However, note that when low-level sampling is selected by bits 0 to 7 in ICSR1, just writing 0 to a flag is ignored (the flag is not cleared); flags can be cleared by writing 0 to it only after a high level is input to the POE pin and is sampled.

High-current pins that have entered high-impedance state due to output-level detection can be released either by returning them to their initial state with a power-on reset, or by clearing the flag in bit 15 (OCF1) in OCSR1. However, note that just writing 0 to a flag is ignored (the flag is not cleared); flags can be cleared only after an inactive level is output from the high-current pins. Inactive-level outputs can be achieved by setting the MTU2 internal registers.

(2) Clock

An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SCSMR) and bits CKE1 and CKE0 in the serial control register (SCSCR) (table 12.14).

When an external clock is input at the SCK pin, it must have a frequency equal to 16 times the desired bit rate.

When the SCI operates on an internal clock, it can output a clock signal at the SCK pin. The frequency of this output clock is equal to 16 times the desired bit rate.

(3) Transmitting and Receiving Data

SCI Initialization (Asynchronous Mode):

Before transmitting or receiving, clear the TE and RE bits to 0 in the serial control register (SCSCR), then initialize the SCI as follows.

When changing the operation mode or the communication format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing the TE bit to 0 sets the TDRE flag to 1 and initializes the transmit shift register (SCTSR). Clearing the RE bit to 0, however, does not initialize the RDRF, PER, FER, and ORER flags or receives data register (SCRDR), which retains their previous contents.

When an external clock is used, the clock should not be stopped during initialization or subsequent operation. SCI operation becomes unreliable if the clock is stopped.

13.7 Usage Notes

13.7.1 Module Standby Mode Setting

Operation of the A/D converter can be disabled or enabled using the standby control register. The initial setting is for operation of the A/D converter to be halted. Register access is enabled by clearing module standby mode. For details, refer to section 19, Power-Down Modes.

13.7.2 Permissible Signal Source Impedance

This LSI's analog input is designed such that conversion accuracy is guaranteed for an input signal for which the signal source impedance is 1 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 1 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. However, for A/D conversion in single mode with a large capacitance provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/μs or greater) (see figure 13.7). When converting a high-speed analog signal or converting in scan mode, a low-impedance buffer should be inserted.

13.7.3 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute precision. Be sure to make the connection to an electrically stable GND such as AVss.

Care is also required to insure that filter circuits do not interfere in the accuracy by the printed circuit digital signals on the mounting board (i.e, acting as antennas).

14.4 Interrupts

14.4.1 CMT Interrupt Sources

The CMT has channels and each of them to which a different vector address is allocated has compare match interrupt. When both the interrupt request flag (CMF) and interrupt enable bit (CMIE) are set to 1, the corresponding interrupt request is output. When the interrupt is used to activate a CPU interrupt, the priority of channels can be changed by the interrupt controller settings. For details, see section 6, Interrupt Controller (INTC).

14.4.2 Timing of Setting Compare Match Flag

When CMCOR and CMCNT match, a compare match signal is generated and the CMF bit in CMCSR is set to 1. The compare match signal is generated in the last cycle in which the values match (when the CMCNT value is updated to H'0000). That is, after a match between CMCOR and CMCNT, the compare match signal is not generated until the next CMCNT counter clock input. Figure 14.4 shows the timing of CMF bit setting.

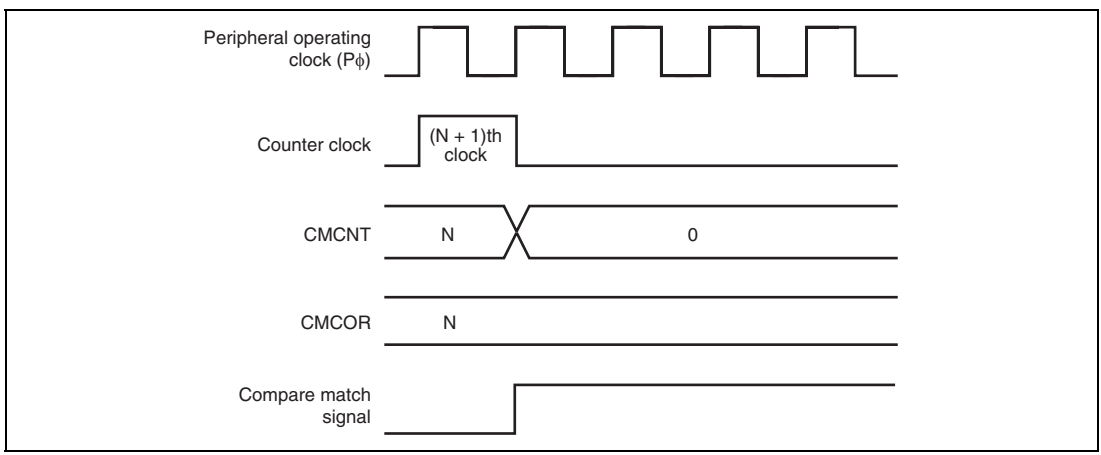


Figure 14.4 Timing of CMF Setting

14.4.3 Timing of Clearing Compare Match Flag

The CMF bit in CMCSR is cleared by reading 1 from this bit, then writing 0.

Table 15.2 SH7124 Multiplexed Pins

Port	Function 1 (Related Module)	Function 2 (Related Module)	Function 3 (Related Module)	Function 4 (Related Module)	Function 5 (Related Module)
A	PA0 I/O (port)	$\overline{\text{POE0}}$ input (POE)	RXD0 input (SCI)	—	—
	PA1 I/O (port)	$\overline{\text{POE1}}$ input (POE)	TXD0 output (SCI)	—	—
	PA3 I/O (port)	IRQ1 input (INTC)	RXD1 input (SCI)	$\overline{\text{TRST}}$ input (H-UDI)*2	—
	PA4 I/O (port)	IRQ2 input (INTC)	TXD1 output (SCI)	TMS input (H-UDI)*2	—
	PA6 I/O (port)	TCLKA input (MTU2)	—	—	—
	PA7 I/O (port)	TCLKB input (MTU2)	SCK2 I/O (SCI)	TCK input (H-UDI)*2	—
	PA8 I/O (port)	TCLKC input (MTU2)	RXD2 input (SCI)	TDI input (H-UDI)*2	—
	PA9 I/O (port)	TCLKD input (MTU2)	TXD2 output (SCI)	$\overline{\text{POE8}}$ input (POE)	TDO output (H-UDI)*2
B	PB1 I/O (port)	TIC5W input (MTU2)	—	—	—
	PB3 I/O (port)	IRQ1 input (INTC)	$\overline{\text{POE1}}$ input (POE)	TIC5V input (MTU2)	—
	PB5 I/O (port)	IRQ3 input (INTC)	TIC5U input (MTU2)	—	—
E	PE0 I/O (port)	TIOC0A I/O (MTU2)	—	—	—
	PE1 I/O (port)	TIOC0B I/O (MTU2)	RXD0 input (SCI)	—	—
	PE2 I/O (port)	TIOC0C I/O (MTU2)	TXD0 output (SCI)	—	—
	PE3 I/O (port)	TIOC0D I/O (MTU2)	SCK0 I/O (SCI)	—	—
	PE8 I/O (port)	TIOC3A I/O (MTU2)	—	—	—
	PE9 I/O (port)	TIOC3B I/O (MTU2)	—	—	—
	PE10 I/O (port)	TIOC3C I/O (MTU2)	—	—	—
	PE11 I/O (port)	TIOC3D I/O (MTU2)	—	—	—
	PE12 I/O (port)	TIOC4A I/O (MTU2)	—	—	—
	PE13 I/O (port)	TIOC4B I/O (MTU2)	$\overline{\text{MRES}}$ input (INTC)	—	—
	PE14 I/O (port)	TIOC4C I/O (MTU2)	—	—	—
	PE15 I/O (port)	TIOC4D I/O (MTU2)	$\overline{\text{IRQOUT}}$ output (INTC)	—	—

	Pin Name	
	Single-Chip Mode (MCU Mode 3)	
Pin No.	Initial Function	PFC Selected Function Possibilities
22	PA4/(TMS*[1])	PA4/IRQ2/TXD1
21	PA6	PA6/TCLKA
20	PA7/(TCK*[1])	PA7/TCLKB/SCK2
18	PA8/(TDI*[1])	PA8/TCLKC/RXD2
16	PA9/(TDO*[1])	PA9/TCLKD/TXD2/$\overline{\text{POE8}}$
38	PB1	PB1/TIC5W
37	PB3	PB3/IRQ1/$\overline{\text{POE1}}$/TIC5V
36	PB5	PB5/IRQ3/TIC5U
15	PE0	PE0/TIOC0A
14	PE1	PE1/TIOC0B/RXD0
13	PE2	PE2/TIOC0C/TXD0
12	PE3	PE3/TIOC0D/SCK0
11	PE8	PE8/TIOC3A
9	PE9	PE9/TIOC3B
10	PE10	PE10/TIOC3C
7	PE11	PE11/TIOC3D
5	PE12	PE12/TIOC4A
3	PE13	PE13/TIOC4B/$\overline{\text{MRES}}$
2	PE14	PE14/TIOC4C
1	PE15	PE15/TIOC4D/$\overline{\text{IRQOUT}}$
47	PF0/AN0	PF0/AN0
46	PF1/AN1	PF1/AN1
45	PF2/AN2	PF2/AN2
44	PF3/AN3	PF3/AN3
43	PF4/AN4	PF4/AN4
42	PF5/AN5	PF5/AN5
41	PF6/AN6	PF6/AN6
40	PF7/AN7	PF7/AN7

Notes: 1. Fixed to TMS, $\overline{\text{TRST}}$, TDI, TDO, TCK, and $\overline{\text{ASEBRKAK}}$/$\overline{\text{ASEBRK}}$ when using the E10A (in $\overline{\text{ASEMD0}}$ = low).

2. E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.

- Port E Control Register L1 (PECRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PE3 MD2	PE3 MD1	PE3 MD0	-	PE2 MD2	PE2 MD1	PE2 MD0	-	PE1 MD2	PE1 MD1	PE1 MD0	-	-	PE0 MD1	PE0 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PE3MD2	0	R/W	PE3 Mode
13	PE3MD1	0	R/W	Select the function of the PE3/TIOC0D/SCK0 pin.
12	PE3MD0	0	R/W	000: PE3 I/O (port) 001: TIOC0D I/O (MTU2) 110: SCK0 I/O (SCI) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PE2MD2	0	R/W	PE2 Mode
9	PE2MD1	0	R/W	Select the function of the PE2/TIOC0C/TXD0 pin.
8	PE2MD0	0	R/W	000: PE2 I/O (port) 001: TIOC0C I/O (MTU2) 110: TXD0 output (SCI) Other than above: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	PE1MD2	0	R/W	PE1 Mode
5	PE1MD1	0	R/W	Select the function of the PE1/TIOC0B/RXD0 pin.
4	PE1MD0	0	R/W	000: PE1 I/O (port) 001: TIOC0B I/O (MTU2) 110: RXD0 input (SCI) Other than above: Setting prohibited

- PEPRL (SH7124)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PE15 PR	PE14 PR	PE13 PR	PE12 PR	PE11 PR	PE10 PR	PE9 PR	PE8 PR	-	-	-	-	PE3 PR	PE2 PR	PE1 PR	PE0 PR
Initial value:	*	*	*	*	*	*	*	*	0	0	0	0	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	PE15PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
14	PE14PR	Pin state	R	
13	PE13PR	Pin state	R	
12	PE12PR	Pin state	R	
11	PE11PR	Pin state	R	
10	PE10PR	Pin state	R	
9	PE9PR	Pin state	R	
8	PE8PR	Pin state	R	
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	PE3PR	Pin state	R	The pin state is returned regardless of the PFC setting. These bits cannot be modified.
2	PE2PR	Pin state	R	
1	PE1PR	Pin state	R	
0	PE0PR	Pin state	R	

17.2 Overview

17.2.1 Block Diagram

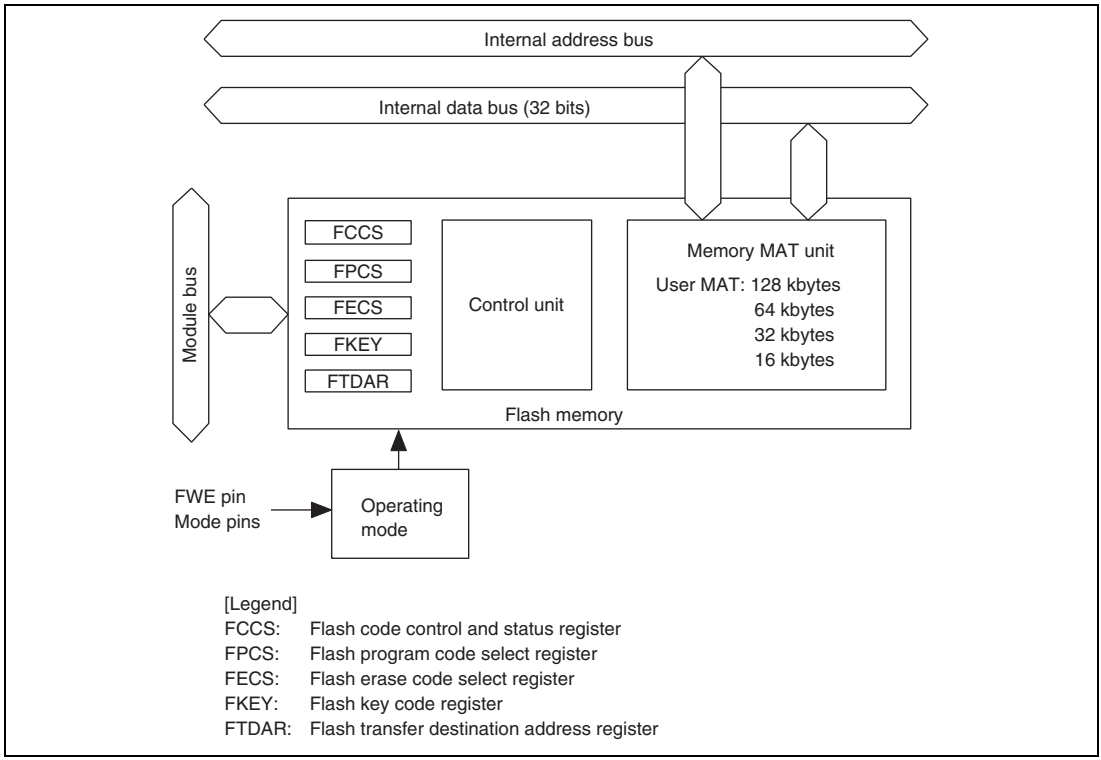


Figure 17.1 Block Diagram of Flash Memory

21.3.6 Serial Communication Interface (SCI) Timing

Table 21.10 Serial Communication Interface (SCI) Timing

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = -20$ to +85°C (consumer specifications),
$T_a = -40$ to +85°C (industrial specifications)

Item		Symbol	Min.	Max.	Unit	Reference Figure
Input clock cycle (asynchronous)		t_{scyc}	4	—	t_{pcyc}	Figure 21.12
Input clock cycle (clock synchronous)		t_{scyc}	6	—	t_{pcyc}	
Input clock pulse width		t_{sckw}	0.4	0.6	t_{scyc}	
Input clock rising time		t_{sckr}	—	1.5	t_{pcyc}	
Input clock falling time		t_{sckf}	—	1.5	t_{pcyc}	
Transmit data delay time	Asynchronous	t_{TXD}	—	4 t_{pcyc} + 10	ns	Figure 21.13
Receive data setup time		t_{RXS}	4 t_{pcyc}	—	ns	
Receive data hold time		t_{RXH}	4 t_{pcyc}	—	ns	
Transmit data delay time	Clock synchronous	t_{TXD}	—	3 t_{pcyc} + 10	ns	
Receive data setup time		t_{RXS}	2 t_{pcyc} + 50	—	ns	
Receive data hold time		t_{RXH}	2 t_{pcyc}	—	ns	

Note: t_{pcyc} indicates the peripheral clock (Pϕ) cycle.

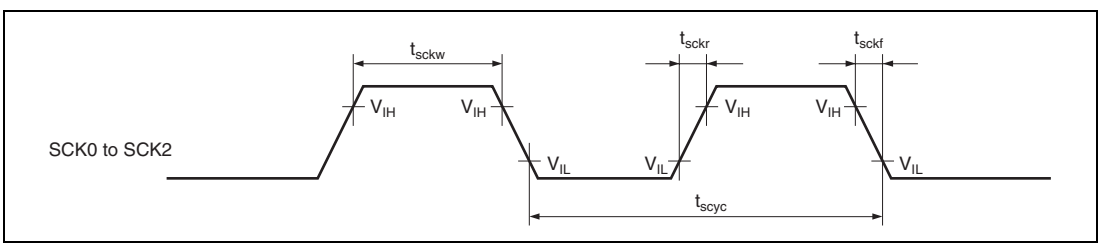


Figure 21.12 Input Clock Timing