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Details

Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71251ad50npv

Section 4 Clock Pulse Generator (CPG)

This LSI has a clock pulse generator (CPG) that generates an internal clock ($I\phi$), a bus clock ($B\phi$), a peripheral clock ($P\phi$), and a clock ($MP\phi$) for the MTU2 module. The CPG also controls power-down modes.

4.1 Features

- Five clocks generated independently

An internal clock ($I\phi$) for the CPU; a peripheral clock ($P\phi$) for the on-chip peripheral modules; a bus clock ($B\phi = CK$) for the external bus interface; and a MTU2 clock ($MP\phi$) for the on-chip MTU2 module.

- Frequency change function

Frequencies of the internal clock ($I\phi$), bus clock ($B\phi$), peripheral clock ($P\phi$), and MTU2 clock ($MP\phi$) can be changed independently using the divider circuit within the CPG. Frequencies are changed by software using the frequency control register (FRQCR) setting.

- Power-down mode control

The clock can be stopped in sleep mode and standby mode and specific modules can be stopped using the module standby function.

- Oscillation stop detection

If the clock supplied through the clock input pin stops for any reason, the timer pins can be automatically placed in the high-impedance state.

The clock pulse generator blocks function as follows:

PLL Circuit: The PLL circuit multiplies the clock frequency input from the crystal oscillator or the EXTAL pin by 8. The multiplication ratio is fixed at $\times 8$.

Crystal Oscillator: The crystal oscillator is an oscillator circuit when a crystal resonator is connected to the XTAL and EXTAL pins.

Divider: The divider generates clocks with the frequencies to be used by the internal clock ($I\phi$), bus clock ($B\phi$), peripheral clock ($P\phi$), and MTU2 clock ($MP\phi$).

The frequencies can be selected from 1/2, 1/4 (initial value), and 1/8 times the frequency output from the PLL circuit. The division ratio should be specified in the frequency control register (FRQCR).

Oscillation Stop Detection Circuit: This circuit detects an abnormal condition in the crystal oscillator.

Clock Frequency Control Circuit: The clock frequency control circuit controls the clock frequency according to the setting in the frequency control register (FRQCR).

Standby Control Circuit: The standby control circuit controls the state of the on-chip oscillator circuit and other modules in sleep or standby mode.

Frequency Control Register (FRQCR): The frequency control register (FRQCR) has control bits for the frequency division ratios of the internal clock ($I\phi$), bus clock ($B\phi$), peripheral clock ($P\phi$), and MTU2 clock ($MP\phi$).

Oscillation Stop Detection Control Register (OSCCR): The oscillation stop detection control register (OSCCR) has an oscillation stop detection flag and a bit for selecting flag status output through an external pin.

Standby Control Registers 1 to 6 (STBCR1 to STBCR6): The standby control register (STBCR) has bits for controlling the power-down modes. For details, see section 19, Power-Down Modes.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	IFC[2:0]	011	R/W	Internal Clock ($I\phi$) Frequency Division Ratio Specify the division ratio of the internal clock ($I\phi$) frequency with respect to the output frequency of PLL circuit. If a prohibited value is specified, subsequent operation is not guaranteed. 000: Setting prohibited 001: $\times 1/2$ 010: Setting prohibited 011: $\times 1/4$ (initial value) 100: $\times 1/8$ Other than above: Setting prohibited
11 to 9	BFC[2:0]	011	R/W	Bus Clock ($B\phi$) Frequency Division Ratio Specify the division ratio of the bus clock ($B\phi$) frequency with respect to the output frequency of PLL circuit. If a prohibited value is specified, subsequent operation is not guaranteed. 000: Setting prohibited 001: $\times 1/2$ 010: Setting prohibited 011: $\times 1/4$ (initial value) 100: $\times 1/8$ Other than above: Setting prohibited

5.7 Stack States after Exception Handling Ends

The stack states after exception handling ends are shown in table 5.11.

Table 5.11 Stack Status after Exception Handling Ends

Types	Stack State
Address error (when the instruction that caused an exception is placed in the delay slot)	<div><div>SP →</div><div><div>Address of delayed branch instruction</div><div>32 bits</div></div><div><div>SR</div><div>32 bits</div></div></div>
Address error (other than above)	<div><div>SP →</div><div><div>Address of instruction that caused exception</div><div>32 bits</div></div><div><div>SR</div><div>32 bits</div></div></div>
Interrupt	<div><div>SP →</div><div><div>Address of instruction after executed instruction</div><div>32 bits</div></div><div><div>SR</div><div>32 bits</div></div></div>
Trap instruction	<div><div>SP →</div><div><div>Address of instruction after TRAPA instruction</div><div>32 bits</div></div><div><div>SR</div><div>32 bits</div></div></div>

7.2.11 Break Control Register (BRCR)

BRCR sets the following conditions:

1. Channels A and B are used in two independent channel conditions or under the sequential condition.
2. A break is set before or after instruction execution.
3. Specify whether to include the number of execution times on channel B in comparison conditions.
4. Determine whether to include data bus on channels A and B in comparison conditions.
5. Enable PC trace.
6. Specify whether to request the user break interrupt when channels A and B match with comparison conditions.

BRCR is a 32-bit readable/writable register that has break conditions match flags and bits for setting a variety of break conditions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	UBIDB	-	UBIDA	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCM FCA	SCM FCB	SCM FDA	SCM FDB	PCTE	PCBA	-	-	DBEA	PCBB	DBEB	-	SEQ	-	-	ETBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	UBIDB	0	R/W	User Break Disable B Enables or disables the user break interrupt request when the channel B break conditions are satisfied. 0: User break interrupt request is enabled when break conditions are satisfied 1: User break interrupt request is disabled when break conditions are satisfied

<Channel B>

Address: H'0003722E, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read/word

After an instruction with address H'0003722E is executed, a user break occurs before an instruction with address H'0003722E is executed.

(Example 1-3)

- Register specifications

BARA = H'00027128, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000000, BDMRA = H'00000000, BARB = H'00031415, BAMRB = H'00000000, BBRB = H'0054, BDRB = H'00000000, BDMRB = H'00000000, BR CR = H'00000000

Specified conditions: Channel A/channel B independent mode

<Channel A>

Address: H'00027128, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

<Channel B>

Address: H'00031415, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

On channel A, no user break occurs since instruction fetch is not a write cycle. On channel B, no user break occurs since instruction fetch is performed for an even address.

(Example 1-4)

- Register specifications

BARA = H'00037226, BAMRA = H'00000000, BBRA = H'005A, BDRA = H'00000000, BDMRA = H'00000000, BARB = H'0003722E, BAMRB = H'00000000, BBRB = H'0056, BDRB = H'00000000, BDMRB = H'00000000, BR CR = H'00000008

Specified conditions: Channel A/channel B sequential mode

<Channel A>

Address: H'00037226, Address mask: H'00000000

Data: H'00000000, Data mask: H'00000000

Bus cycle: L bus/instruction fetch (before instruction execution)/write/word

9.2 Input/Output Pins

Table 9.2 Pin Configuration

Channel	Pin Name	I/O	Function
Common	TCLKA	Input	External clock A input pin (Channel 1 phase counting mode A phase input)
	TCLKB	Input	External clock B input pin (Channel 1 phase counting mode B phase input)
	TCLKC	Input	External clock C input pin (Channel 2 phase counting mode A phase input)
	TCLKD	Input	External clock D input pin (Channel 2 phase counting mode B phase input)
0	TIOC0A	I/O	TGRA_0 input capture input/output compare output/PWM output pin
	TIOC0B	I/O	TGRB_0 input capture input/output compare output/PWM output pin
	TIOC0C	I/O	TGRC_0 input capture input/output compare output/PWM output pin
	TIOC0D	I/O	TGRD_0 input capture input/output compare output/PWM output pin
1	TIOC1A*	I/O	TGRA_1 input capture input/output compare output/PWM output pin
	TIOC1B*	I/O	TGRB_1 input capture input/output compare output/PWM output pin
2	TIOC2A*	I/O	TGRA_2 input capture input/output compare output/PWM output pin
	TIOC2B*	I/O	TGRB_2 input capture input/output compare output/PWM output pin
3	TIOC3A	I/O	TGRA_3 input capture input/output compare output/PWM output pin
	TIOC3B	I/O	TGRB_3 input capture input/output compare output/PWM output pin
	TIOC3C	I/O	TGRC_3 input capture input/output compare output/PWM output pin
	TIOC3D	I/O	TGRD_3 input capture input/output compare output/PWM output pin
4	TIOC4A	I/O	TGRA_4 input capture input/output compare output/PWM output pin
	TIOC4B	I/O	TGRB_4 input capture input/output compare output/PWM output pin
	TIOC4C	I/O	TGRC_4 input capture input/output compare output/PWM output pin
	TIOC4D	I/O	TGRD_4 input capture input/output compare output/PWM output pin
5	TIC5U	Input	TGRU_5 input capture input/external pulse input pin
	TIC5V	Input	TGRV_5 input capture input/external pulse input pin
	TIC5W	Input	TGRW_5 input capture input/external pulse input pin

Note: * Supported only by the SH7125.



10. Complementary PWM Mode PWM Output Generation Method

In complementary PWM mode, 3-phase output is performed of PWM waveforms with a non-overlap time between the positive and negative phases. This non-overlap time is called the dead time.

A PWM waveform is generated by output of the output level selected in the timer output control register in the event of a compare-match between a counter and data register. While TCNTS is counting, data register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of on and off compare-match occurrence may vary, but the compare-match that turns off each phase takes precedence to secure the dead time and ensure that the positive phase and negative phase on times do not overlap. Figures 9.46 to 9.48 show examples of waveform generation in complementary PWM mode.

The positive phase/negative phase off timing is generated by a compare-match with the solid-line counter, and the on timing by a compare-match with the dotted-line counter operating with a delay of the dead time behind the solid-line counter. In the T1 period, compare-match **a** that turns off the negative phase has the highest priority, and compare-matches occurring prior to **a** are ignored. In the T2 period, compare-match **c** that turns off the positive phase has the highest priority, and compare-matches occurring prior to **c** are ignored.

In normal cases, compare-matches occur in the order **a** → **b** → **c** → **d** (or **c** → **d** → **a'** → **b'**), as shown in figure 9.46.

If compare-matches deviate from the **a** → **b** → **c** → **d** order, since the time for which the negative phase is off is less than twice the dead time, the figure shows the positive phase is not being turned on. If compare-matches deviate from the **c** → **d** → **a'** → **b'** order, since the time for which the positive phase is off is less than twice the dead time, the figure shows the negative phase is not being turned on.

If compare-match **c** occurs first following compare-match **a**, as shown in figure 9.47, compare-match **b** is ignored, and the negative phase is turned off by compare-match **d**. This is because turning off of the positive phase has priority due to the occurrence of compare-match **c** (positive phase off timing) before compare-match **b** (positive phase on timing) (consequently, the waveform does not change since the positive phase goes from off to off).

Similarly, in the example in figure 9.48, compare-match **a'** with the new data in the temporary register occurs before compare-match **c**, but other compare-matches occurring up to **c**, which turns off the positive phase, are ignored. As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare-matches at turn-off timings take precedence, and turn-on timing compare-matches that occur before a turn-off timing compare-match are ignored.

Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Reset-Synchronized PWM Mode: Figure 9.148 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in reset-synchronized PWM mode after re-setting.

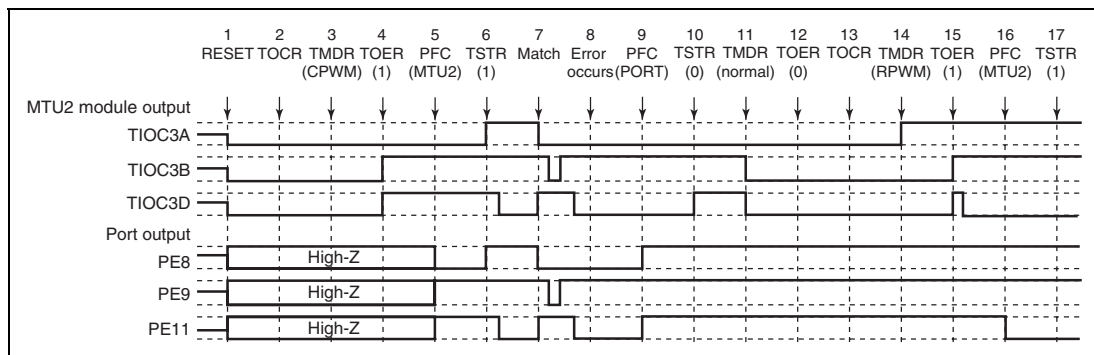


Figure 9.148 Error Occurrence in Complementary PWM Mode, Recovery in Reset-Synchronized PWM Mode

1 to 10 are the same as in figure 9.144.

11. Set normal mode. (MTU2 output goes low.)
12. Disable channel 3 and 4 output with TOER.
13. Select the reset-synchronized PWM mode output level and cyclic output enabling/disabling with TOCR.
14. Set reset-synchronized PWM.
15. Enable channel 3 and 4 output with TOER.
16. Set MTU2 output with the PFC.
17. Operation is restarted by TSTR.

10.4 Operation

Table 10.4 shows the target pins for high-impedance control and conditions to place the pins in high-impedance state.

Table 10.4 Target Pins and Conditions for High-Impedance Control

Pins	Conditions	Detailed Conditions
MTU2 high-current pins (PE9/TIOC3B and PE11/TIOC3D)	Input level detection, output level comparison, or SPOER setting	MTU2P1CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE12/TIOC4A and PE14/TIOC4C)	Input level detection, output level comparison, or SPOER setting	MTU2P2CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 high-current pins (PE13/TIOC4B and PE15/TIOC4D)	Input level detection, output level comparison, or SPOER setting	MTU2P3CZE • ((POE3F + POE1F + POE0F) + (OSF1 • OCE1) + (MTU2CH34HIZ))
MTU2 channel 0 pin (PE0/TIOC0A)	Input level detection or SPOER setting	MTU2PE0ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE1/TIOC0B)	Input level detection or SPOER setting	MTU2PE1ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE2/TIOC0C)	Input level detection or SPOER setting	MTU2PE2ZE ((POE8F • POE8E) + (MTU2CH0HIZ))
MTU2 channel 0 pin (PE3/TIOC0D)	Input level detection or SPOER setting	MTU2PE3ZE ((POE8F • POE8E) + (MTU2CH0HIZ))

10.4.1 Input Level Detection Operation

If the input conditions set by ICSR1 occur on the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$ *, and $\overline{\text{POE8}}$ pins, the high-current pins and the pins for channel 0 of the MTU2 are placed in high-impedance state. Note however, that these high-current and MTU2 pins enter high-impedance state only when general input/output function or MTU2 function is selected for these pins.

(1) Falling Edge Detection

When a change from a high to low level is input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$ *, and $\overline{\text{POE8}}$ pins, the high-current pins and the pins for channel 0 of the MTU2 are placed in high-impedance state. Figure 10.2 shows a sample timing after the level changes in input to the $\overline{\text{POE0}}$, $\overline{\text{POE1}}$, $\overline{\text{POE3}}$ *, and $\overline{\text{POE8}}$ pins until the respective pins enter high-impedance state.

Note: * This pin is supported only by the SH7125.

11.3 Register Descriptions

The WDT has the following two registers. Refer to section 20, List of Registers, for the details of the addresses of these registers and the state of registers in each operating mode.

Table 11.2 Register Configuration

Register Name	Abbrevia- tion	R/W	Initial Value	Address	Access Size
Watchdog timer counter	WTCNT	R/W	H'00	H'FFFFE810	8, 16
Watchdog timer control/status register	WTCSR	R/W	H'00	H'FFFFE812	8, 16

11.3.1 Watchdog Timer Counter (WTCNT)

WTCNT is an 8-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a reset in watchdog timer mode and an interrupt in interval time mode. The WTCNT counter is not initialized by an internal reset due to the WDT overflow. The WTCNT counter is initialized to H'00 only by a power-on reset using the RES pin. Use a word access to write to the WTCNT counter, with H'5A in the upper byte. Use a byte access to read WTCNT.

Note: WTCNT differs from other registers in that it is more difficult to write to. See section 11.3.3, Notes on Register Access, for details.

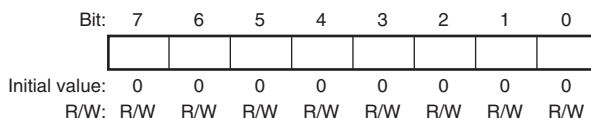
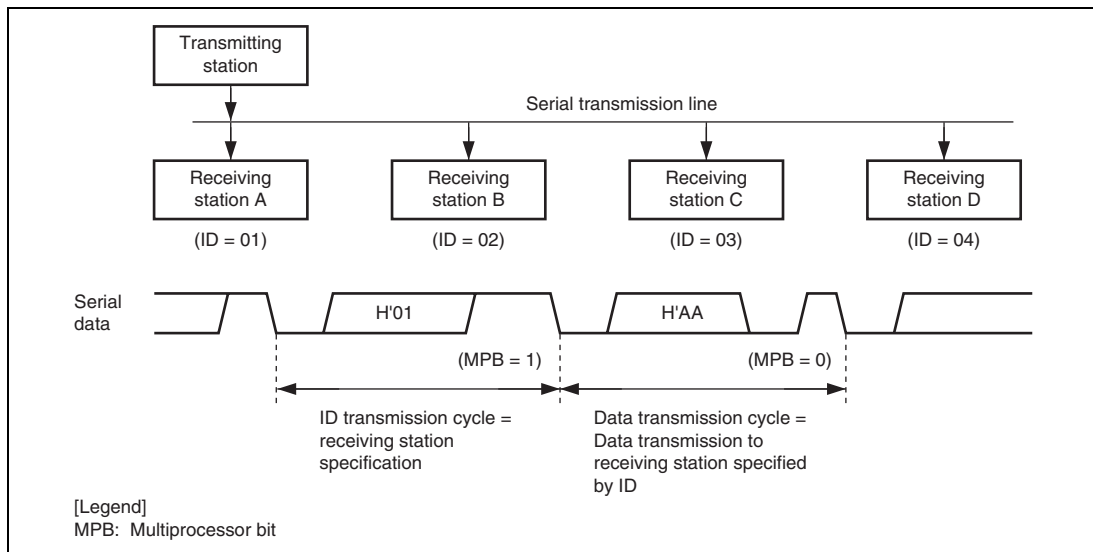


Table 12.5 Bit Rates and SCBRR Settings in Asynchronous Mode (2)

Bit Rate (bits/s)	P ϕ (MHz)																	
	22			24			26			28			30			32		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	97	-0.35	3	106	-0.44	3	114	0.36	3	123	0.23	3	132	0.13	3	141	0.03
150	3	71	-0.54	3	77	0.16	3	84	-0.43	3	90	0.16	3	97	-0.35	3	103	0.16
300	2	142	0.16	2	155	0.16	2	168	0.16	2	181	0.16	2	194	0.16	2	207	0.16
600	2	71	-0.54	2	77	0.16	2	84	-0.43	2	90	0.16	2	97	-0.35	2	103	0.16
1200	1	142	0.16	1	155	0.16	1	168	0.16	1	181	0.16	1	194	0.16	1	207	0.16
2400	1	71	-0.54	1	77	0.16	1	84	-0.43	1	90	0.16	1	97	-0.35	1	103	0.16
4800	0	142	0.16	0	155	0.16	0	168	0.16	0	181	0.16	0	194	0.16	0	207	0.16
9600	0	71	-0.54	0	77	0.16	0	84	-0.43	0	90	0.16	0	97	-0.35	0	103	0.16
14400	0	47	-0.54	0	51	0.16	0	55	0.76	0	60	-0.39	0	64	0.16	0	68	0.64
19200	0	35	-0.54	0	38	0.16	0	41	0.76	0	45	-0.93	0	48	-0.35	0	51	0.16
28800	0	23	-0.54	0	25	0.16	0	27	0.76	0	29	1.27	0	32	-1.36	0	34	-0.79
31250	0	21	0.00	0	23	0.00	0	25	0.00	0	27	0.00	0	29	0.00	0	31	0.00
38400	0	17	-0.54	0	19	-2.34	0	20	0.76	0	22	-0.93	0	23	1.73	0	25	0.16



**Figure 12.15 Example of Communication Using Multiprocessor Format
(Transmission of Data H'AA to Receiving Station A)**

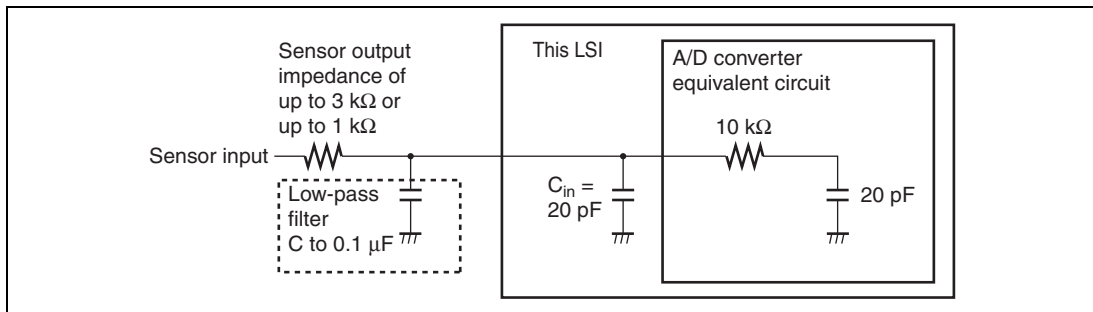


Figure 13.7 Example of Analog Input Circuit

13.7.4 Range of Analog Power Supply and Other Pin Settings

If the conditions below are not met, the reliability of the device may be adversely affected.

- **Analog input voltage range**
The voltage applied to analog input pin ANn during A/D conversion should be in the range $AV_{SS} \leq V_{AN} \leq AV_{ref}$.
- **Relationship between AVcc, AVss and Vcc, Vss**
Set $V_{CC} \leq AV_{CC} \leq 5.5V$, $AV_{SS} = V_{SS}$ for the relationship between AVcc, AVss and Vcc, Vss.
If the A/D converter is not used, the AVcc and AVss pins must not be left open.

13.7.5 Notes on Board Design

In board design, digital circuitry and analog circuitry should be as mutually isolated as possible, and layout in which digital circuit signal lines and analog circuit signal lines cross or are in close proximity should be avoided as far as possible. Failure to do so may result in incorrect operation of the analog circuitry due to inductance, adversely affecting A/D conversion values. Also, digital circuitry must be isolated from the analog input signals (AN0 to AN7), and analog power supply (AVcc) by the analog ground (AVss). Also, the analog ground (AVss) should be connected at one point to a stable ground (Vss) on the board.

Bit	Bit Name	Initial Value	R/W	Description
14	PE15MD2	0	R/W	PE15 Mode
13	PE15MD1	0	R/W	Select the function of the PE15/TIOC4D/ $\overline{\text{IRQOUT}}$ pin.
12	PE15MD0	0	R/W	000: PE15 I/O (port) 001: TIOC4D I/O (MTU2) 011: $\overline{\text{IRQOUT}}$ output (INTC) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PE14MD2	0	R/W	PE14 Mode
9	PE14MD1	0	R/W	Select the function of the PE14/TIOC4C pin.
8	PE14MD0	0	R/W	000: PE14 I/O (port) 001: TIOC4C I/O (MTU2) Other than above: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PE13MD1	0	R/W	PE13 Mode
4	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/ $\overline{\text{MRES}}$ pin. 00: PE13 I/O (port) 01: TIOC4B I/O (MTU2) 10: $\overline{\text{MRES}}$ input (INTC) Other than above: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	PE12MD2	0	R/W	PE12 Mode
1	PE12MD1	0	R/W	Select the function of the PE12/TIOC4A pin.
0	PE12MD0	0	R/W	000: PE12 I/O (port) 001: TIOC4A I/O (MTU2) Other than above: Setting prohibited

SH7124:

- Port E Control Register L4 (PECRL4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PE15 MD2	PE15 MD1	PE15 MD0	-	PE14 MD2	PE14 MD1	PE14 MD0	-	-	PE13 MD1	PE13 MD0	-	PE12 MD2	PE12 MD1	PE12 MD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PE15MD2	0	R/W	PE15 Mode
13	PE15MD1	0	R/W	Select the function of the PE15/TIOC4D/ $\overline{\text{IRQOUT}}$ pin.
12	PE15MD0	0	R/W	000: PE15 I/O (port) 001: TIOC4D I/O (MTU2) 011: $\overline{\text{IRQOUT}}$ output (INTC) Other than above: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	PE14MD2	0	R/W	PE14 Mode
9	PE14MD1	0	R/W	Select the function of the PE14/TIOC4C pin.
8	PE14MD0	0	R/W	000: PE14 I/O (port) 001: TIOC4C I/O (MTU2) Other than above: Setting prohibited
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PE13MD1	0	R/W	PE13 Mode
4	PE13MD0	0	R/W	Select the function of the PE13/TIOC4B/ $\overline{\text{MRES}}$ pin. 00: PE13 I/O (port) 01: TIOC4B I/O (MTU2) 10: $\overline{\text{MRES}}$ input (INTC) Other than above: Setting prohibited

Table 17.5 Register/Parameter and Target Mode

		Download	Initiali- zation	Program- ming	Erase	Read
Programming/ erasing interface registers	FCCS	√	—	—	—	—
	FPCS	√	—	—	—	—
	PECS	√	—	—	—	—
	FKEY	√	—	√	√	—
	FTDAR	√	—	—	—	—
Programming/ erasing interface parameters	DPFR	√	—	—	—	—
	FPFR	—	√	√	√	—
	FPEFEQ	—	√	—	—	—
	FUBRA	—	√	—	—	—
	FMPAR	—	—	√	—	—
	FMPDR	—	—	√	—	—
	FEBS	—	—	—	√	—

- Command H'3F (1 byte): New bit rate selection
- Size (1 byte): The total length of the bit rate, input frequency, number of multipliers, and multiplier fields
- Bit rate (2 bytes): New bit rate
The bit rate value divided by 100 should be set here (for example, to select 19200 bps, the set H'00C0, which is 192 in decimal notation).
- Input frequency (2 bytes): The frequency of the clock signal fed to the boot program
This should be the frequency in MHz to the second decimal place, multiplied by 100 (for example, if the frequency is 28.882 MHz, the values is truncated to the second decimal place and multiplied by 100, making 2888; so H'0B48 should be set in this field).
- Number of multipliers (1 byte): The number of selectable frequency multipliers and divisors for the device.
This is normally 2, which indicates the main operating frequency and the operating frequency of the peripheral modules.
- Multiplier 1 (1 byte): Multiplier or divisor for the main operating frequency
Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for $\times 4$)
Divisor: Two's complement negative numerical value in the case of frequency division (e.g. H'FE [-2] for $\times 1/2$)
- Multiplier 2 (1 byte): Multiplier or divisor for the peripheral operating frequency
Multiplier: Numerical value of the frequency multiplier (e.g. H'04 for $\times 4$)
Divisor: Two's complement negative numerical value in the case of frequency division (e.g. H'FE [-2] for $\times 1/2$)
- SUM (1 byte): Checksum

Response

H'06

- Response H'06 (1 byte): Response to the new-bit-rate selection command
This is the ACK code and is returned if the specified bit rate has been selected.

Error

response

H'BF	ERROR
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- Error response H'BF (1 byte): Error response to new bit rate selection
- ERROR (1 byte): Error code
H'11: Sum-check error
H'24: Bit rate selection error (the specified bit rate is not selectable).
H'25: Input frequency error (the specified input frequency is not within the range from the minimum to the maximum value).

19.3.4 Standby Control Register 4 (STBCR4)

STBCR4 is an 8-bit readable/writable register that controls the operation of modules in power-down mode.

Bit:	7	6	5	4	3	2	1	0
	-	MSTP 22	MSTP 21	-	-	-	MSTP 17	MSTP 16
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
6	MSTP22	1	R/W	Module Stop Bit 22 When this bit is set to 1, the supply of the clock to the MTU2 is halted. 0: MTU2 operates 1: Clock supply to MTU2 halted
5	MSTP21	1	R/W	Module Stop Bit 21 When this bit is set to 1, the supply of the clock to the CMT is halted. 0: CMT operates 1: Clock supply to CMT halted
4, 3	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
2	—	1	R/W	Reserved This bit is always read as 1. The write value should always be 1.
1	MSTP17	1	R/W	Module Stop Bit 17 When this bit is set to 1, the supply of the clock to the A/D_1 is halted. 0: A/D_1 operates 1: Clock supply to A/D_1 halted