Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI
Peripherals	POR, PWM, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	External
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN
Supplier Device Package	64-VQFN (8.2x8.2)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71251an50npv

The instruction code, operation, and execution cycles of the instructions are listed in the following tables, classified by type.

Instruction	Instruction Code	Summary of Operation	Execution Cycles	T Bit
Indicated by mnemonic.	Indicated in MSB ↔ LSB order.	Indicates summary of operation.	Value when no wait cycles are inserted*1	Value of T bit after instruction is executed Explanation of Symbols —: No change
Explanation of Symbols OP.Sz SRC, DEST OP: Operation code Sz: Size SRC: Source DEST: Destination Rm: Source register Rn: Destination register imm: Immediate data disp: Displacement*2	Explanation of Symbols mmmm: Source register nnnn: Destination register 0000: R0 0001: R1 ····· 1111: R15 iiii: Immediate data dddd: Displacement	Explanation of Symbols →, ←: Transfer direction (xx): Memory operand M/Q/T: Flag bits in SR &: Logical AND of each bit |: Logical OR of each bit ^: Exclusive logical OR of each bit –: Logical NOT of each bit <<n: n-bit left shift >>n: n-bit right shift		

Notes: 1. The table shows the minimum number of execution states. In practice, the number of instruction execution states will be increased in cases such as the following:
- When there is contention between an instruction fetch and a data access
- When the destination register of a load instruction (memory → register) is also used by the following instruction

2. Scaled (×1, ×2, or ×4) according to the instruction operand size, etc.
For details, see SH-1/SH-2/SH-DSP Software Manual.

Table 9.24 TIORH_3 (Channel 3)

				Description	
Bit 3 IOA3	**Bit 2 IOA2**	**Bit 1 IOA1**	**Bit 0 IOA0**	**TGRA_3 Function**	**TIOC3A Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	x	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

Bit	Bit Name	Initial Value	R/W	Description
4	TCFV	0	R/(W)*[1]	Overflow Flag Status flag that indicates that TCNT overflow has occurred. Only 0 can be written, for flag clearing. [Setting condition] • When the TCNT value overflows (changes from H'FFFF to H'0000) In channel 4, when the TCNT_4 value underflows (changes from H'0001 to H'0000) in complementary PWM mode, this flag is also set. [Clearing condition] • When 0 is written to TCFV after reading TCFV = 1*[2]
3	TGFD	0	R/(W)*[1]	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0, 3, and 4. Only 0 can be written, for flag clearing. In channels 1 and 2, bit 3 is reserved. It is always read as 0 and the write value should always be 0. [Setting conditions] • When TCNT = TGRD and TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal and TGRD is functioning as input capture register [Clearing condition] • When 0 is written to TGFD after reading TGFD = 1*[2]

Example of Synchronous Operation in SH7125:

Figure 9.13 shows an example of synchronous operation.

In this example, synchronous operation and PWM mode 1 have been designated for channels 0 to 2, TGRB_0 compare match has been set as the channel 0 counter clearing source, and synchronous clearing has been set for the channel 1 and 2 counter clearing source.

Three-phase PWM waveforms are output from pins TIOC0A, TIOC1A, and TIOC2A. At this time, synchronous presetting, and synchronous clearing by TGRB_0 compare match, are performed for channel 0 to 2 TCNT counters, and the data set in TGRB_0 is used as the PWM cycle.

For details of PWM modes, see section 9.4.5, PWM Modes.

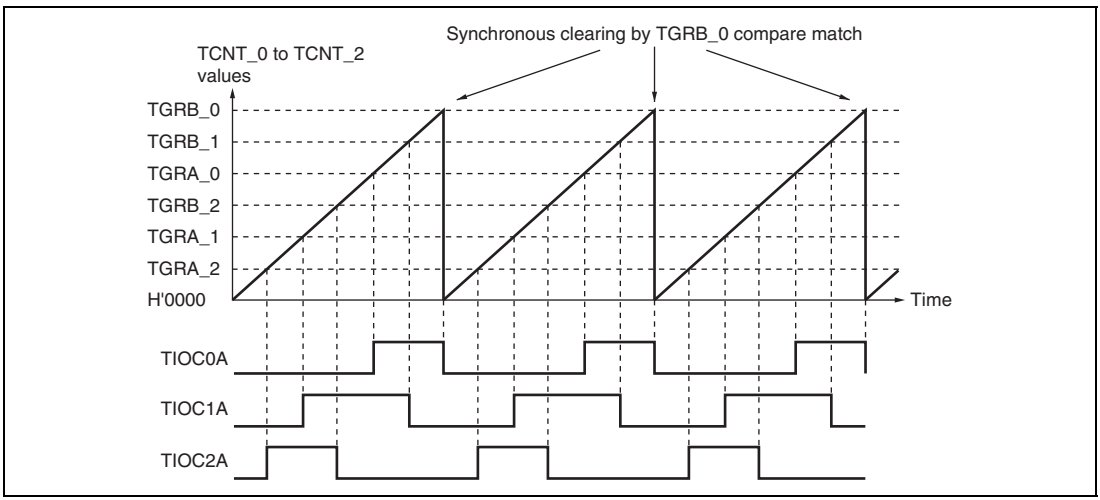


Figure 9.13 Example of Synchronous Operation

Example of PWM Mode Setting Procedure: Figure 9.25 shows an example of the PWM mode setting procedure.

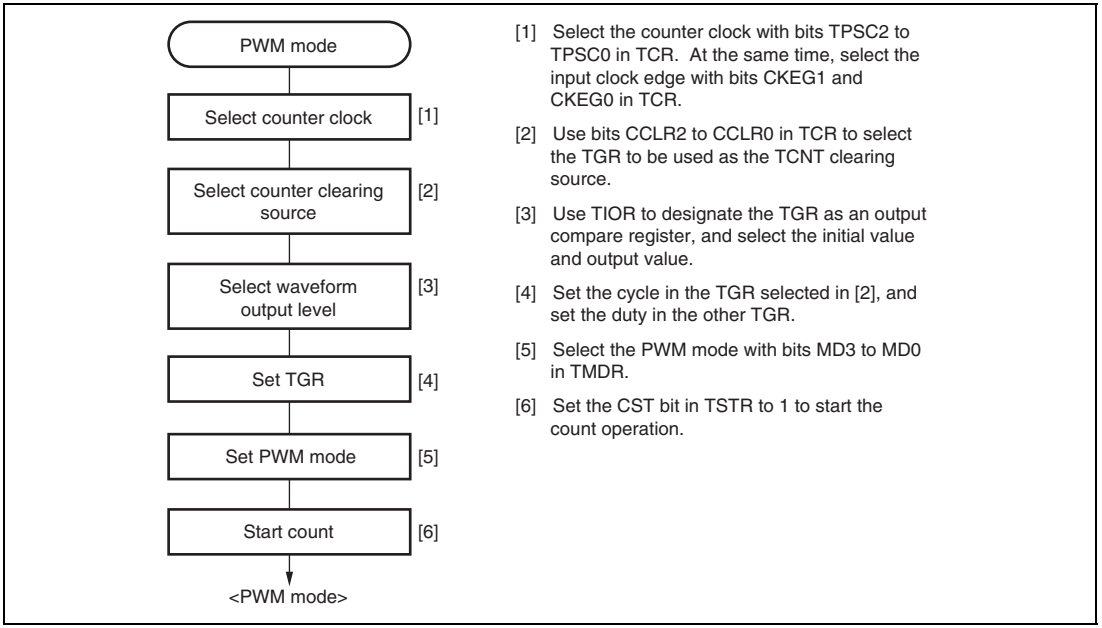


Figure 9.25 Example of PWM Mode Setting Procedure

Examples of PWM Mode Operation: Figure 9.26 shows an example of PWM mode 1 operation.

In this example, TGRA compare match is set as the TCNT clearing source, 0 is set for the TGRA initial output value and output value, and 1 is set as the TGRB output value.

In this case, the value set in TGRA is used as the period, and the values set in the TGRB registers are used as the duty levels.

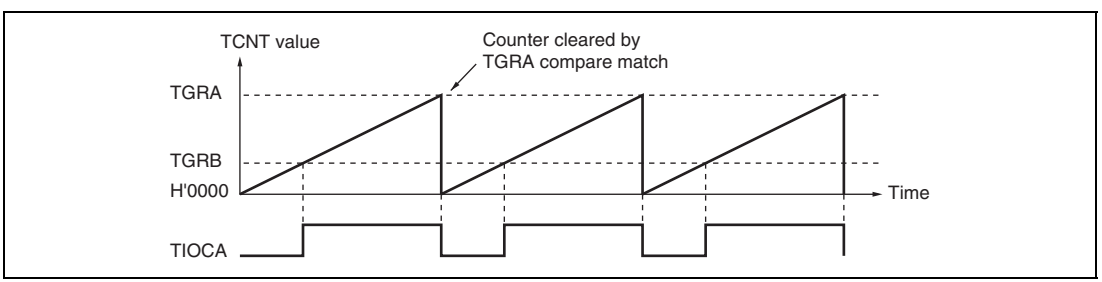


Figure 9.26 Example of PWM Mode Operation (1)

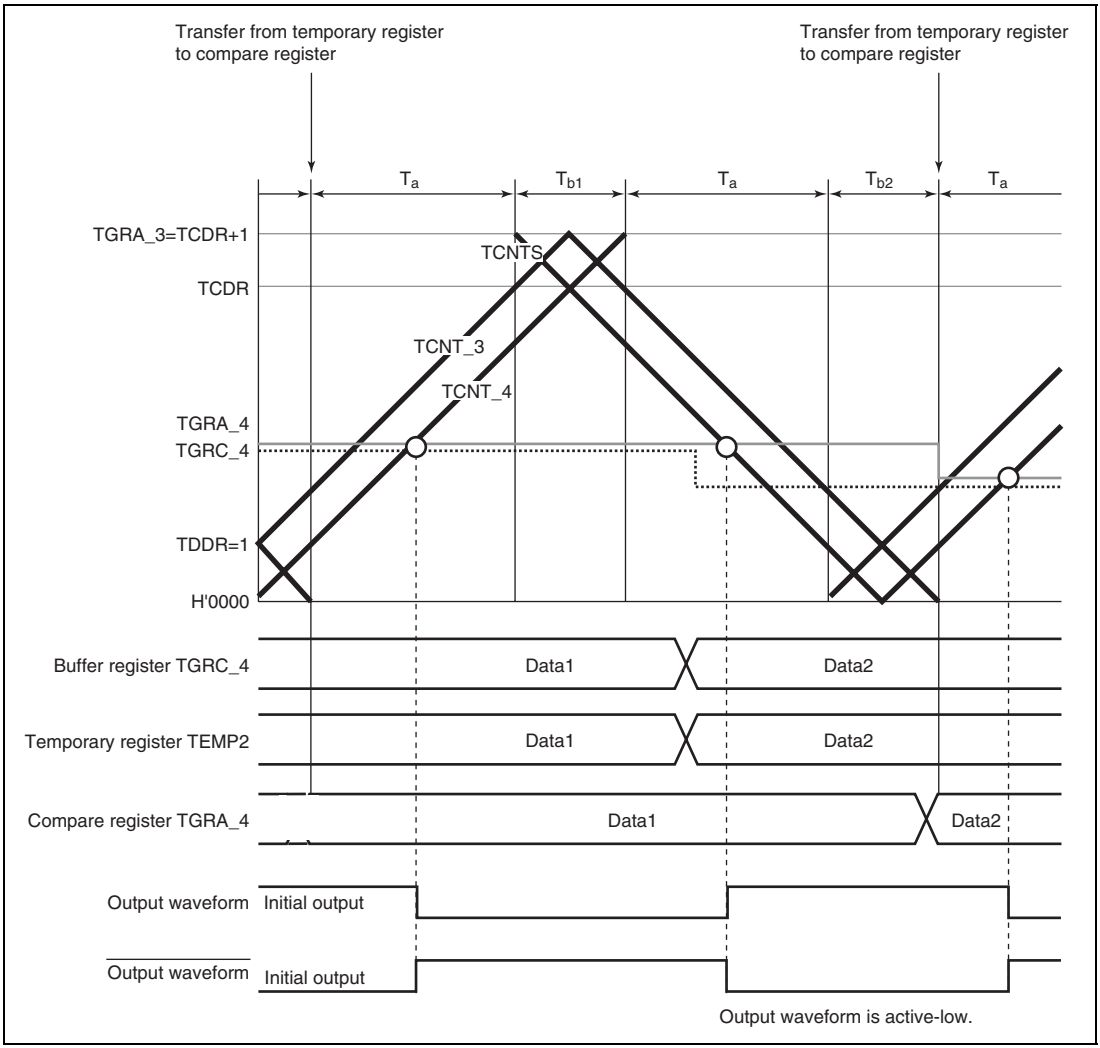


Figure 9.41 Example of Operation without Dead Time

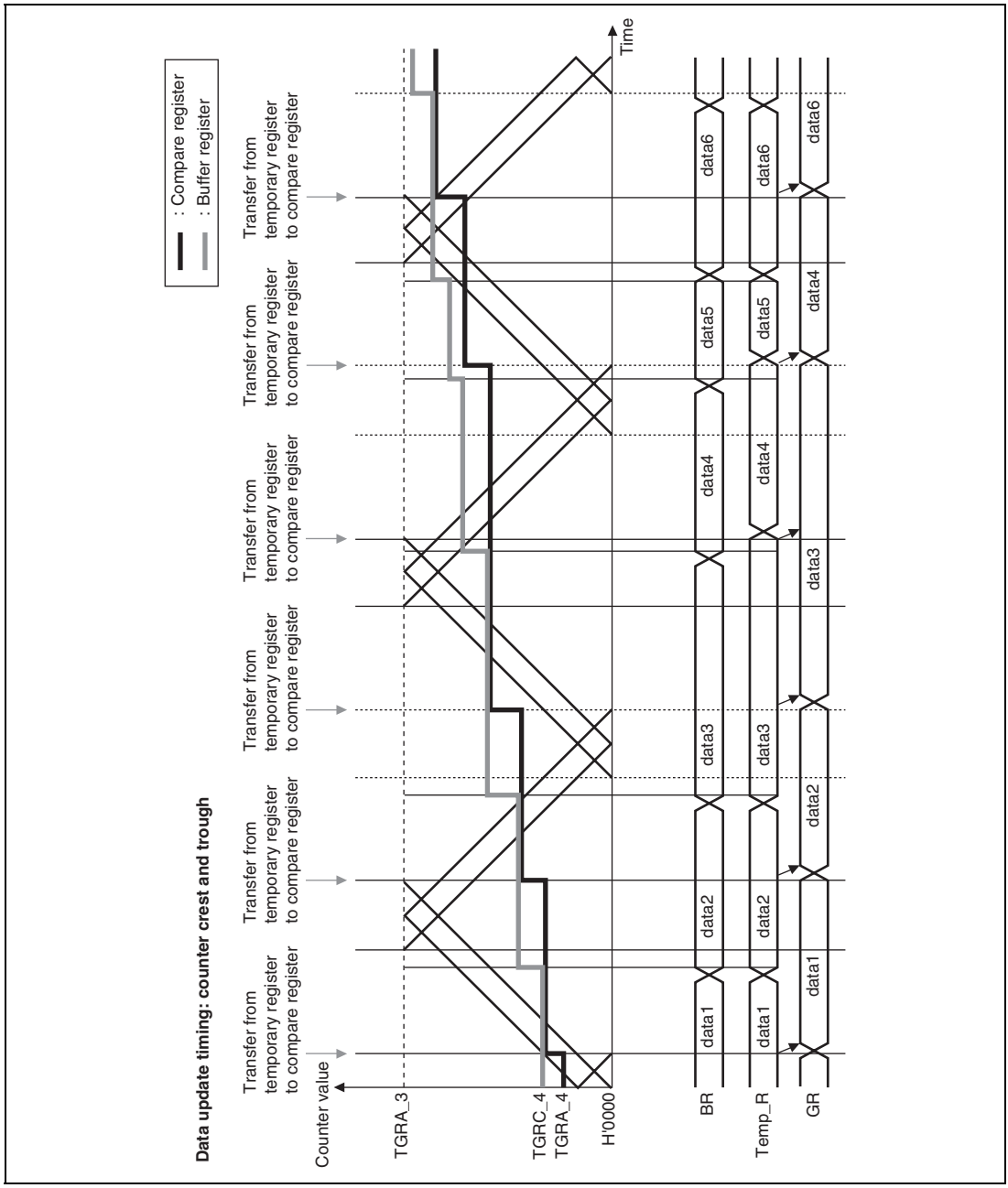


Figure 9.43 Example of Data Update in Complementary PWM Mode

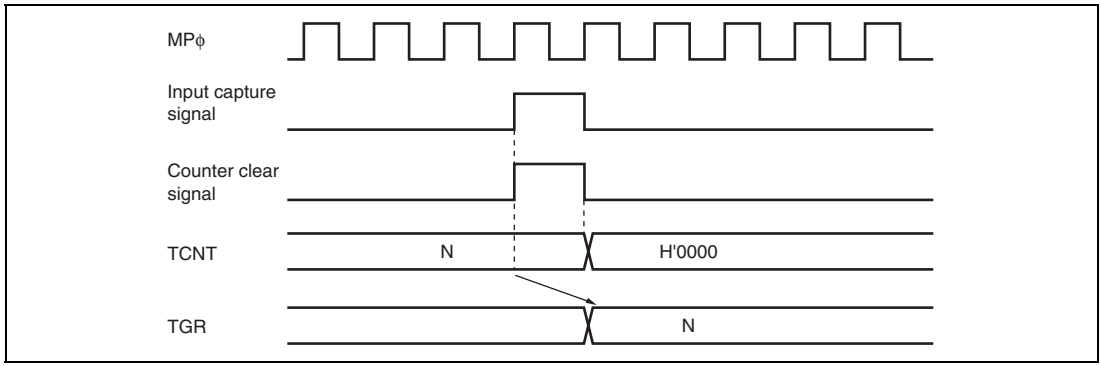


Figure 9.92 Counter Clear Timing (Input Capture)

Buffer Operation Timing: Figures 9.93 to 9.95 show the timing in buffer operation.

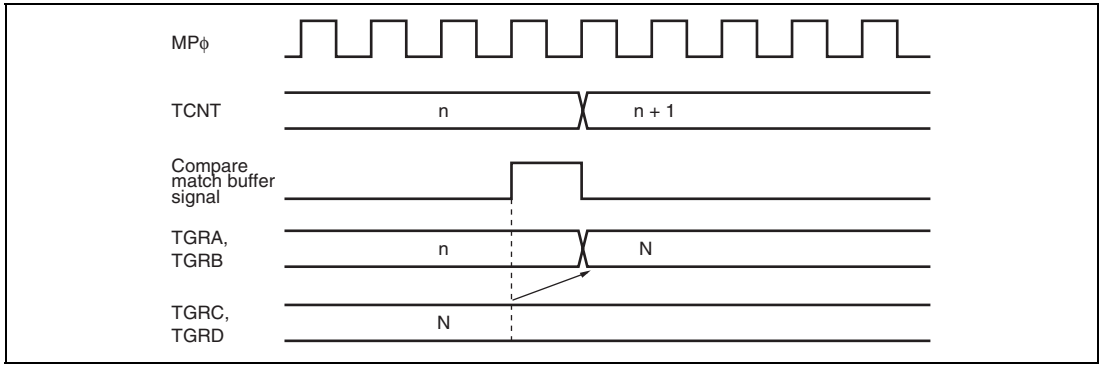


Figure 9.93 Buffer Operation Timing (Compare Match)

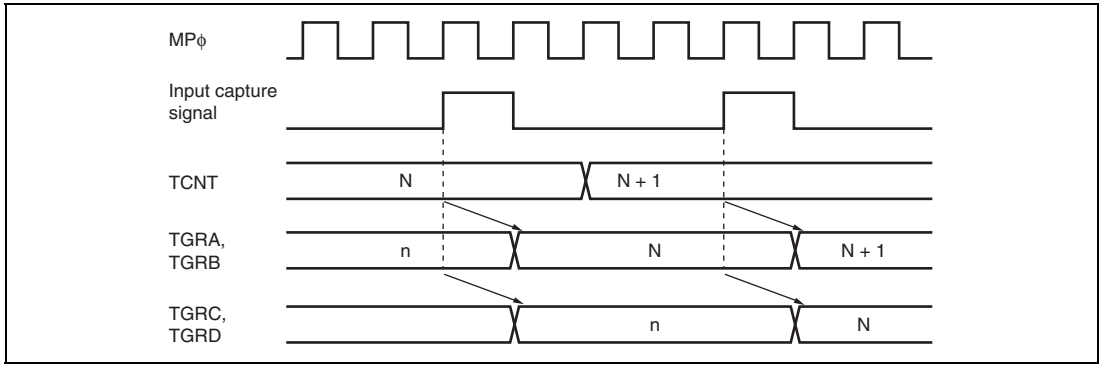


Figure 9.94 Buffer Operation Timing (Input Capture)

10.3 Register Descriptions

The POE has the following registers. For details on register addresses and register states during each processing, refer to section 20, List of Registers.

Table 10.3 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Input level control/status register 1	ICSR1	R/W	H'0000	H'FFFFD000	8, 16, 32
Output level control/status register 1	OCSR1	R/W	H'0000	H'FFFFD002	8, 16
Input level control/status register 3	ICSR3	R/W	H'0000	H'FFFFD008	8, 16, 32
Software port output enable register	SPOER	R/W	H'00	H'FFFFD00A	8
Port output enable control register 1	POECR1	R/W	H'00	H'FFFFD00B	8
Port output enable control register 2	POECR2	R/W	H'7700	H'FFFFD00C	8, 16

- Port B Control Register L2 (PBCRL2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	PB5MD2	PB5MD1	PB5MD0	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	PB5MD2	0	R/W	PB5 Mode
5	PB5MD1	0	R/W	Select the function of the PB5/IRQ3/TIC5U pin.
4	PB5MD0	0	R/W	000: PB5 I/O (port) 001: IRQ3 input (INTC) 011: TIC5U input (MTU2) Other than above: Setting prohibited
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

- Port B Control Register L1 (PBCRL1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	PB3MD2	PB3MD1	PB3MD0	-	-	-	-	-	PB1MD2	PB1MD1	PB1MD0	-	-	-	-
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

- PBPRL (SH7124)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	-	PB5PR	-	PB3PR	-	PB1PR	-
Initial value:	0	0	0	0	0	0	0	0	0	0	*	0	*	0	*	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	PB5PR	Pin state	R	The pin state is returned regardless of the PFC setting. This bit cannot be modified.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	PB3PR	Pin state	R	The pin state is returned regardless of the PFC setting. This bit cannot be modified.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	PB1PR	Pin state	R	The pin state is returned regardless of the PFC setting. This bit cannot be modified.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	Undefined	R/W	Unused Return 0.
7 to 0	EBS[7:0]	Undefined	R/W	• 128-kbyte flash memory Set the erase-block number in the range from 0 to 9. 0 corresponds to the EB0 block and 9 corresponds to the EB9 block. An error occurs when a number other than 0 to 9 (H'00 to H'09) is set. • 64-kbyte flash memory Set the erase-block number in the range from 0 to 8. 0 corresponds to the EB0 block and 8 corresponds to the EB8 block. An error occurs when a number other than 0 to 8 (H'00 to H'08) is set.

(4.2) Flash pass/fail result parameter (FPFR: general register R0 of CPU)

This parameter returns the value of the erasing processing result.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-	-	MD	EE	FK	EB	-	-	SF
Initial value:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	Undefined	R/W	Unused Return 0.

(7) Inquiry on user MATs

In response to the inquiry on user MATs, the boot program returns the number of user MAT areas and their addresses.

Command	H'25

— Command H'25 (1 byte): Inquiry on user MAT information

Response	H'35	Size	No. of areas	
	First address of the area			Last address of the area
	…			
	SUM			

— Response H'35 (1 byte): Response to the inquiry on user MATs
— Size (1 byte): The total length of the number of areas and first and last address fields.
— Number of areas (1 byte): The number of user MAT areas.
H'01 is returned if the entire user MAT area is continuous.
— First address of the area (4 bytes)
— Last address of the area (4 bytes)
As many pairs of first and last address field are included as there are areas.
— SUM (1 byte): Checksum

(8) Inquiry on erasure blocks

In response to the inquiry on erasure blocks, the boot program returns the number of erasure blocks in the user MAT and the addresses where each block starts and ends.

Command	H'26

— Command H'26 (1 byte): Inquiry on erasure blocks

Response	H'36	Size	No. of blocks	
	First address of the block			Last address of the block
	…			
	SUM			

Section 19 Power-Down Modes

This LSI supports the following power-down modes: sleep mode, software standby mode, and module standby mode.

19.1 Features

- Supports sleep mode, software standby mode, and module standby mode.

19.1.1 Types of Power-Down Modes

This LSI has the following power-down modes.

- Sleep mode
- Software standby mode
- Module standby mode

Table 19.1 shows the methods to make a transition from the program execution state, as well as the CPU and peripheral module states in each mode and the procedures for canceling each mode.

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
TIER_1	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	MTU2
TSR_1	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_1									
TGRA_1									
TGRB_1									
TICCR	—	—	—	—	I2BE	I2AE	I1BE	I1AE	
TCR_2	—	CCLR[1:0]		CKEG[1:0]		TPSC[2:0]			
TMDR_2	—	—	—	—	MD[3:0]				
TIOR_2	IOB[3:0]				IOA[3:0]				
TIER_2	TTGE	—	TCIEU	TCIEV	—	—	TGIEB	TGIEA	
TSR_2	TCFD	—	TCFU	TCFV	—	—	TGFB	TGFA	
TCNT_2									
TGRA_2									
TGRB_2									
TCNTU_5									
TGRU_5									
TCRU_5	—	—	—	—	—	—	TPSC[1:0]		
TIORU_5	—	—	—	IOC[4:0]					
TCNTV_5									
TGRV_5									
TCRV_5	—	—	—	—	—	—	TPSC[1:0]		

Register Abbreviation	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0	Module
ADCSR_1	ADF	ADIE	—	—	TRGE	—	CONADF	STC	A/D (Channel 1)
	CKSL[1:0]		ADM[1:0]		ADCS	CH[2:0]			
ADCR_1	—	—	ADST	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
FCCS	FWE	—	—	FLER	—	—	—	SCO	FLASH
FPCS	—	—	—	—	—	—	—	PPVS	
FECS	—	—	—	—	—	—	—	EPVB	
FKEY	K[7:0]								
FTDAR	TDER	TDA[6:0]							
CMSTR	—	—	—	—	—	—	—	—	CMT
	—	—	—	—	—	—	STR1	STR0	
CMCSR_0	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_0									
CMCOR_0									
CMCSR_1	—	—	—	—	—	—	—	—	
	CMF	CMIE	—	—	—	—	CKS[1:0]		
CMCNT_1									
CMCOR_1									
ICSR1	POE3F	—	POE1F	POE0F	—	—	—	PIE1	POE
	POE3M[1:0]		—	—	POE1M[1:0]		POE0M[1:0]		
OCSR1	OSF1	—	—	—	—	—	OCE1	OIE1	
	—	—	—	—	—	—	—	—	
ICSR3	—	—	—	POE8F	—	—	POE8E	PIE3	
	—	—	—	—	—	—	POE8M[1:0]		
SPOER	—	—	—	—	—	—	MTU2CH0HIZ	MTU2CH34HIZ	

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output high voltage	TIOC3B, TIOC3D, TIOC4A to TIOC4D	V_{OH}	V_{CC} – 0.8	—	—	V	I_{OH} = –5 mA, V_{CC} = 4.5 V to 5.5 V
	$\overline{WDTOVF}$		V_{CC} – 0.5	—	—	V	I_{OH} = –100 µA
	All other output pins		V_{CC} – 0.5	—	—	V	I_{OH} = –200 µA
			V_{CC} – 1.0	—	—	V	I_{OH} = –1 mA
			V_{CC} – 1.5	—	—	V	I_{OH} = –2 mA (reference values)
Output low voltage	TIOC3B, TIOC3D, TIOC4A to TIOC4D	V_{OL}	—	—	1.0	V	I_{OL} = 15 mA, V_{CC} = 4.5 V to 5.5 V
			—	—	0.6	V	I_{OL} = 10 mA, V_{CC} = 4.5 V to 5.5 V
			—	—	0.44	V	I_{OL} = 8 mA, V_{CC} = 4.5 V to 5.5 V
	All other output pins		—	—	0.4	V	I_{OL} = 1.6 mA
Input capacitance	All input pins	C_{in}	—	—	20	pF	V_{in} = 0 V f = 1 MHz Ta = 25°C
Supply current	Normal operation	I_{CC}	—	52	70	mA	Iϕ = 50 MHz (SH7125, SH7124)
			—	35	50	mA	Iϕ = 50 MHz (SH71251A, SH71241A, SH71250A, SH71240A)
	Sleep		—	33	50	mA	Iϕ = 50 MHz (SH7125, SH7124)
			—	22	30	mA	Iϕ = 50 MHz (SH71251A, SH71241A, SH71250A, SH71240A)
	Software standby		—	—	5	mA	$T_a \leq 50°C$
			—	—	15	mA	$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	3	5	mA	The value per module
	Waiting for A/D conversion		—	—	2	mA	The value per module
	Standby		—	—	15	µA	

[Operating Precautions]

1. When the A/D converter is not used, do not leave the AV_{CC} and AV_{SS} pins open.
2. The supply current was measured when V_{IH} (Min.) = V_{CC} - 0.5 V, V_{IL} (Max.) = 0.5 V, with all output pins unloaded.

Table 21.3 Permitted Output Current Values

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = –20$ to +85°C (consumer specifications),
$T_a = –40$ to +85°C (industrial specifications)

Item	Symbol	Min.	Typ.	Max.	Unit
Permissible current in low-level output (per pin)	I_{OL}	—	—	2.0*	mA
Permissible current in low-level output (total)	ΣI_{OL}	—	—	80	mA
Permissible current in high-level output (per pin)	$–I_{OH}$	—	—	2.0*	mA
Permissible current in high-level output (total)	$\Sigma –I_{OH}$	—	—	25	mA

[Operating Precautions]

To assure LSI reliability, do not exceed the output values listed in table 21.3.

Note: * I_{OL} = 15 mA (Max.)/$–I_{OH}$ = 5 mA (Max.) for pins PE9 and PE11 to PE15. However, at least three pins are permitted to have simultaneously $I_{OL}/–I_{OH} > 2.0$ mA among these pins.

21.3 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

Table 21.4 Maximum Operating Frequency

Conditions: $V_{CC} = AV_{CC} = 4.0$ V to 5.5 V, $V_{SS} = PLLV_{SS} = AV_{SS} = 0$ V,
$T_a = –20$ to +85°C (consumer specifications),
$T_a = –40$ to +85°C (industrial specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Operating frequency	CPU (Iϕ)	f	10	—	50	MHz	
	Peripheral module (Pϕ)		10	—	40		

Item	Page	Revision (See Manual for Details)
15.1.2 Port A Control Registers L1 to L4 (PACRL1 to PACRL4) • Port A Control Register L1 (PACRL1)	529	Table amended

Bit	Bit Name	Initial Value	R/W	Description
14	PA3MD2	0	R/W	PA3 Mode
13	PA3MD1	0	R/W	Select the function of the PA3/IRQ1/RXD1/$\overline{\text{TRST}}$ pin.
12	PA3MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to $\overline{\text{TRST}}$ input. 000: PA3 I/O (port) 001: RXD1 input (SCI) 111: IRQ1 input (INTC) Other than above: Setting prohibited

	530	Note added Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.
• Port A Control Register L3 (PACRL3)	531	Table amended

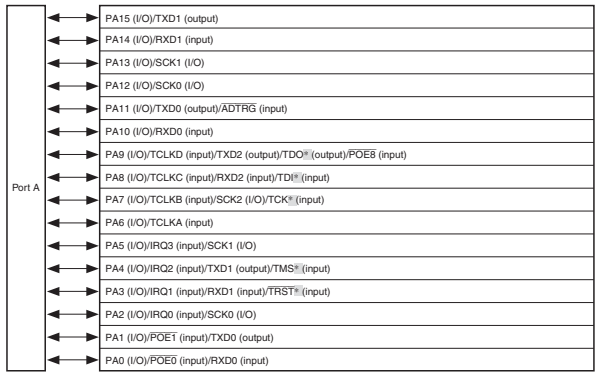
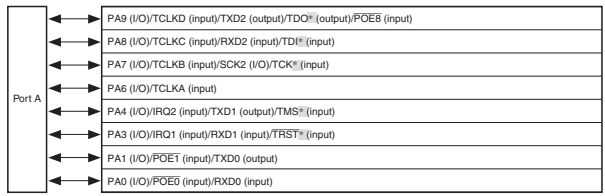
Bit	Bit Name	Initial Value	R/W	Description
6	PA9MD2	0	R/W	PA9 Mode
5	PA9MD1	0	R/W	Select the function of the
4	PA9MD0	0	R/W	PA9/TCLKD/TXD2/TDO/$\overline{\text{POE8}}$ pin. When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDO output. 000: PA9 I/O (port) 001: TCLKD input (MTU2) 110: TXD2 output (SCI) 111: $\overline{\text{POE8}}$ input (POE) Other than above: Setting prohibited

	532	Table amended

Bit	Bit Name	Initial Value	R/W	Description
2	PA8MD2	0	R/W	PA8 Mode
1	PA8MD1	0	R/W	Select the function of the PA8/TCLKC/RXD2/TDI pin.
0	PA8MD0	0	R/W	When the E10A* is in use ($\overline{\text{ASEMD0}}$ = low), function is fixed to TDI input. 000: PA8 I/O (port) 001: TCLKC input (MTU2) 110: RXD2 input (SCI) Other than above: Setting prohibited

Note added

Note: * E10A cannot be used on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.

Item	Page	Revision (See Manual for Details)
16.1 Port A	554	Figure amended
Figure 16.1 Port A (SH7125)		 Note: * The TDO, TDI, TCK, TMS, and TRST pins are not supported on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.
Figure 16.2 Port A (SH7124)	554	Figure amended
		 Note: * The TDO, TDI, TCK, TMS, and TRST pins are not supported on the 32 Kbyte (SH71251A and SH71241A) and 16 Kbyte (SH71250A and SH71240A) versions.
16.5 Usage Notes 16.5.1 Handling of Unused Pins	577	Newly added
17. Flash Memory (ROM)	579	Description amended This LSI has 128-Kbyte, 64-Kbyte, 32-Kbyte, or 16-Kbyte on-chip flash memory. The flash memory has the following features.