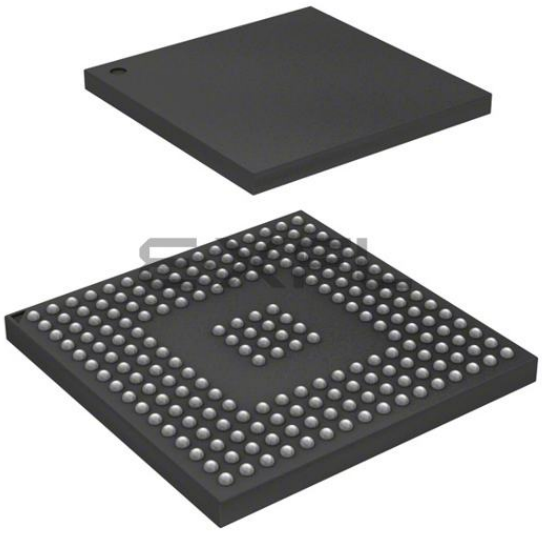
Infineon Technologies - SAF-TC1130-L100EB BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1130-l100eb-bb

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Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1/2, SSC0/1, CCU60, IIC, EBU and SCU.	
P2.0	P12	I/O	PUC	RXD0	ASC0 receiver input/output line
		O		CSEMU	EBU Chip Select Output for Emulator Region
P2.1	P11	O	PUC	TXD0	ASC0 transmitter output line
		I		TESTMODE	Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	O	PUC	COUT60_3	CCU60 compare channel 3 output
		I/O		MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	CC60_0	CCU60 input/output of capture compare channel 0
		I/O		MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	O	PUC	COUT60_0	CCU60 output of capture/compare channel 0
		I/O		SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	CC60_1	CCU60 input/output of capture/ compare channel 1
		I/O		RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	COUT60_1	CCU60 output of capture/compare channel 1
		O		TXD1A	ASC1 transmitter output line A
P2.10	L13	I/O	PUC	CC60_2	CCU60 input/output of capture/ compare channel 2
		I/O		RXD2A	ASC2 receiver input/output line A
P2.11	G16	O	PUC	COUT60_2	CCU60 output of capture/compare channel 2
		O		TXD2A	ASC2 transmitter output line A
P2.12	K15	I/O	—	SDA0	IIC Serial Data line 0
		I		CTRAP0	CCU60 trap input
		O		SLSO0_3	SSC0 Slave Select output 3

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
$\overline{\text{TRST}}$	T11	I	PDC	**JTAG Module Reset/Enable Input** A low level at this pin resets and disables the JTAG module. A high level enables the JTAG module.
TCK	T12	I	PUC	**JTAG Module Clock Input**
TDI	T13	I	PUC	**JTAG Module Serial Data Input**
TDO	T10	O	—	**JTAG Module Serial Data Output**
TMS	T9	I	PUC	**JTAG Module State Machine Control Input**
$\overline{\text{TRCLK}}$	T8	O	—	**Trace Clock for OCDS_L2 Lines**
HWCFG0 **HWCFG1** **HWCFG2**	M14 L14 T6	I I I	PUC PUC PDC	**Hardware Configuration Inputs** The Configuration Inputs define the boot options of the TC1130 after a hardware invoked reset operation.
$\overline{\text{BRKIN}}$	T5	I	PUC	**OCDS Break Input** A low level on this pin causes a break in the chip's execution when the OCDS is enabled. In addition, the level of this pin during power-on reset determines the boot configuration.
MII_ TXCLK	T2	I	PDC	**Ethernet Controller Transmit Clock** MII_TXD[3:0] and MII_TXEN are driven off the rising edge of the MII_TXCLK by the core and sampled by the PHY on the rising edge of the MII_TXCLK.
MII_ RXCLK	R2	I	PDC	**Ethernet Controller Receive Clock** MII_RXCLK is a continuous clock. Its frequency is 25 MHz for 100 Mbit/sec operation, and 2.5 MHz for 10 Mbit/sec. MII_RXD[3:0], MII_RXDV and MII_EXER are driven by the PHY off the falling edge of MII_RXCLK and sampled on the rising edge of MII_RXCLK.
MII_ MDIO	R1	I/O	PDA	**Ethernet Controller Management Data Input/ Output** When a read command is being executed, the data that is clocked out of the PHY will be presented on the input line. When the Core is clocking control or data onto the MII_MDIO line, the signal will carry the information.
D+	T14	I/O	—	**USB D+ Data Line**

Table 3-1 TC1130 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
–	Reserved	F000 1200$_H$ - F000 12FF$_H$	256 Bytes
–	Reserved	F000 1300$_H$ - F000 13FF$_H$	256 Bytes
–	Reserved	F000 1400$_H$ - F000 14FF$_H$	256 Bytes
–	Reserved	F000 1500$_H$ - F000 15FF$_H$	256 Bytes
–	Reserved	F000 1600$_H$ - F000 16FF$_H$	256 Bytes
–	Reserved	F000 1700$_H$ - F000 17FF$_H$	256 Bytes
–	Reserved	F000 1800$_H$ - F000 18FF$_H$	256 Bytes
–	Reserved	F000 1900$_H$ - F000 19FF$_H$	256 Bytes
CCU60	Capture/Compare Unit 0	F000 2000$_H$ - F000 20FF$_H$	256 Bytes
CCU61	Capture/Compare Unit 1	F000 2100$_H$ - F000 21FF$_H$	256 Bytes
–	Reserved	F000 2200$_H$ - F000 3BFF$_H$	–
DMA	Direct Memory Access Controller	F000 3C00$_H$ - F000 3EFF$_H$	3 × 256 Bytes
–	Reserved	F000 3F00$_H$ - F000 3FFF$_H$	–
CAN	MultiCAN Controller	F000 4000$_H$ - F000 5FFF$_H$	8 Kbytes
–	Reserved	F000 6000$_H$ - F00E 1FFF$_H$	–
USB	USB RAM based Registers	F00E 2000$_H$ - F00E 219F$_H$	416 Bytes
USB	USB RAM	F00E 21A0$_H$ - F00E 27FF$_H$	1.6 Kbytes
USB	USB Registers	F00E 2800$_H$ - F00E 28FF$_H$	256 Bytes
–	Reserved	F00E 2900$_H$ - F00F FFFF$_H$	–
Units on SMIF Interface of DMA Controller			
–	Reserved	F010 0000$_H$ - F010 00FF$_H$	256 Bytes
SSC0	Synchronous Serial Interface 0	F010 0100$_H$ - F010 01FF$_H$	256 Bytes
SSC1	Synchronous Serial Interface 1	F010 0200$_H$ - F010 02FF$_H$	256 Bytes
ASC0	Async./Sync. Serial Interface 0	F010 0300$_H$ - F010 03FF$_H$	256 Bytes
ASC1	Async./Sync. Serial Interface 1	F010 0400$_H$ - F010 04FF$_H$	256 Bytes
ASC2	Async./Sync. Serial Interface 2	F010 0500$_H$ - F010 05FF$_H$	256 Bytes
I2C	Inter IC	F010 0600$_H$ - F010 06FF$_H$	256 Bytes
–	Reserved	F010 0700$_H$ - F010 BFFF$_H$	–
MLI0	Micro Link Interface 0	F010 C000$_H$ - F010 C0FF$_H$	256 Bytes
MLI1	Micro Link Interface 1	F010 C100$_H$ - F010 C1FF$_H$	256 Bytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
MLI1_ LP3	MLI1 Large Transfer Window 3	F027 0000$_H$ - F027 FFFF$_H$	64 Kbytes
–	Reserved	F028 0000$_H$ - F200 00FF$_H$	–
ECU	Ethernet Controller Unit	F200 0100$_H$ - F200 05FF$_H$	1280Bytes
–	Reserved	F200 0600$_H$ - F7E0 FEFF$_H$	–
CPU (Part of System Peripheral Bus)			
CPU SFRs	CPU Slave Interface	F7E0 FF00$_H$ - F7E0 FFFF$_H$	256 Bytes
	Reserved	F7E1 0000$_H$ - F7E1 7FFF$_H$	–
	MMU	F7E1 8000$_H$ - F7E1 80FF$_H$	256 Bytes
	Reserved	F7E1 8100$_H$ - F7E1 BFFF$_H$	–
	Memory Protection Registers	F7E1 C000$_H$ -F7E1 EFFF$_H$	12 Kbytes
	Reserved	F7E1 F000$_H$ - F7E1 FCFF$_H$	–
	Core Debug Register (OCDS)	F7E1 FD00$_H$ -F7E1 FDFF$_H$	256 Bytes
	Core Special Function Registers (CSFRs)	F7E1 FE00$_H$ -F7E1 FEFF$_H$	256 Bytes
	General Purpose Register (GPRs)	F7E1 FF00$_H$ - F7E1 FFFF$_H$	256 Bytes
–	Reserved	F7E2 0000$_H$ - F7FF FFFF$_H$	–
Local Memory Buses (LMB)			
EBU	External Bus Interface Unit	F800 0000$_H$ - F800 03FF$_H$	1 Kbyte
DMU	Data Memory Unit	F800 0400$_H$ - F800 04FF$_H$	256 Bytes
–	Reserved	F800 0500$_H$ - F87F FBFF$_H$	–
DMI	Data Memory Interface Unit	F87F FC00$_H$ - F87F FCFF$_H$	256 Bytes
PMI	Program Memory Interface Unit	F87F FD00$_H$ - F87F FDFF$_H$	256 Bytes
LBCU	Local Memory Bus Control Unit	F87F FE00$_H$ - F87F FEFF$_H$	256 Bytes
LFI	LMB to FPI Bus Bridge	F87F FF00$_H$ - F87F FFFF$_H$	256 Bytes
–	Reserved	F880 0000$_H$ - FFFF FFFF$_H$	–

3.4 On-Chip Bus System

The TC1130 includes two bus systems:

- Local Memory Bus (LMB)
- Flexible Peripheral Interface Bus (FPI)

The LMB-to-FPI (LFI) bridge interconnects the FPI bus and LMB Bus.

3.4.1 Local Memory Bus (LMB)

The Local Memory Bus interconnects the memory units and functional units, such as CPU and DMU. The main objective of the LMB bus is to support devices with fast response time. This allows the DMI and PMI fast access to local memory and reduces load on the FPI bus. The TriCore™ system itself is located on the LMB bus. Via External Bus Unit, it interconnects TC1130 and external components.

The Local Memory Bus is a synchronous, pipelined, split bus with variable block size transfer support. It supports 8, 16, 32 and 64 bits single beat transactions and variable length 64 bits block transfers.

Features:

The LMB provides the following features:

- Synchronous, Pipelined, Multimaster, 64-bit high performance bus
- Optimized for high speed and high performance
- 32-bit address, 64-bit data buses
- Central, simple per cycle arbitration
- Slave controlled wait state insertion
- Address pipelining (max depth - 2)
- Supports Split transactions
- Supports Variable block size transfer
- Supports Locked transaction (read-modify-write)

3.4.2 Flexible Peripheral Interconnect Bus (FPI)

The FPI Bus is an on-chip bus that is used in modular and highly integrated microprocessors and microcontrollers (**systems-on-chips**). FPI Bus is designed for memory mapped data transfers between its bus agents. Bus agents are on-chip function blocks (modules), equipped with an FPI Bus interface and connected via FPI Bus signals. An FPI Bus agent acts as an FPI Bus master when it initiates data read or data write operations once bus ownership has been granted to the agent. An FPI Bus agent that is addressed by an FPI Bus operation acts as an FPI Bus slave when it performs the requested data read or write operation.

3.6 Direct Memory Access (DMA)

The Direct Memory Access Controller executes DMA transactions from a source address location to a destination address location, without intervention of the CPU. One DMA transaction is controlled by one DMA channel. Each DMA channel has assigned its own channel register set. The total of 8 channels are provided by one DMA sub-block.

The DMA module is connected to 3 bus interfaces in TC1130, the Flexible Peripheral Interconnect Bus (FPI), the DMA Bus and the Micro Link Bus. It can do transfers on each of the buses as well as between the buses.

In addition, it bridges accesses from the Flexible Peripheral Interconnect Bus to the peripherals on the DMA Bus, allowing easy access to these peripherals by CPU. Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation specific and managed outside the DMA controller kernel.

Features:

- 8 independent DMA channels
  - Up to 8 selectable request inputs per DMA channel
  - Programmable priority of DMA channels within a DMA sub-block (2 levels)
  - Software and hardware DMA request generation
  - Hardware requests by selected peripherals and external inputs
- Programmable priority of the DMA sub-block on the bus interfaces
- Buffer capability for move actions on the buses (min. 1 move per bus is buffered).
- Individually programmable operation modes for each DMA channel
  - Single mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated.
  - Programmable address modification
- Full 32-bit addressing capability of each DMA channel
  - 4-Gbyte address range
  - Support of circular buffer addressing mode
- Programmable data width of a DMA transaction: 8-bit, 16-bit, or 32-bit
- Micro Link supported
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA module)
- All buses/interfaces connected to the DMA module must work at the same frequency
- Read/write requests of the FPI Bus Side to the Remote Peripherals are bridged to the DMA Bus (only the DMA is master on the DMA bus)

3.8 Parallel Ports

The TC1130 has 72 digital input/output port lines, which are organized into four parallel 16-bit ports and one parallel 8-bit port, Port P0 to Port P4 with 3.3 V nominal voltage.

The digital parallel ports can be used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. An overview on the port-to-peripheral unit assignment is shown in **Figure 3-4**.

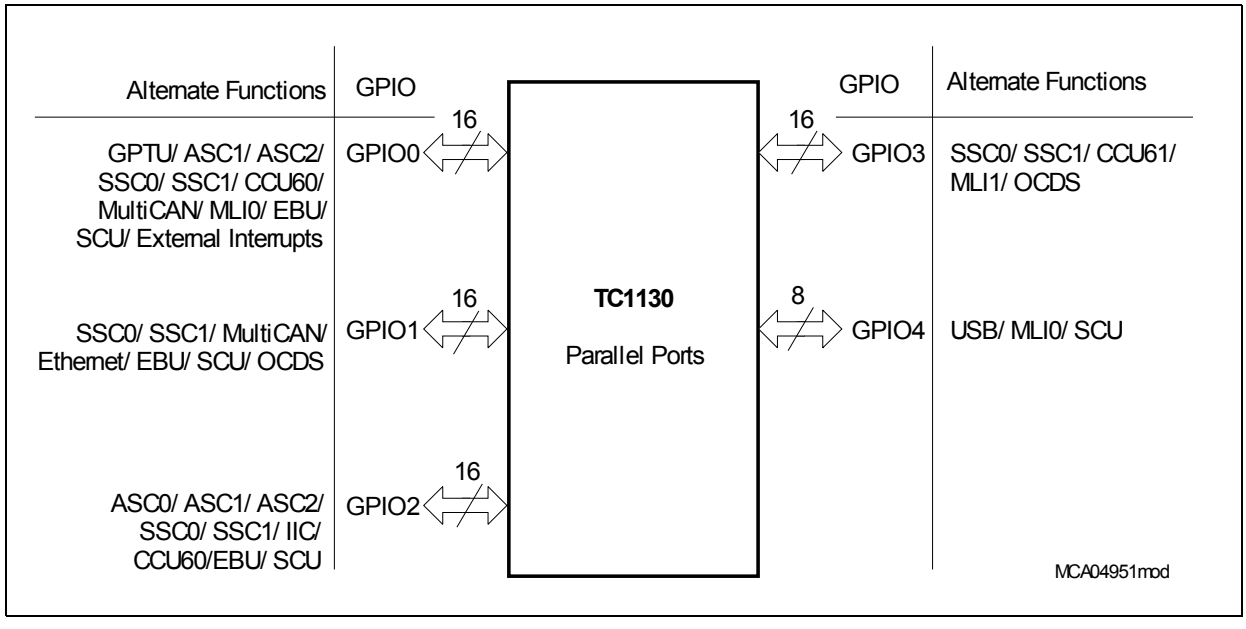

Figure 3-4 Parallel Ports of the TC1130

3.16 Capture/Compare Unit 6 (CCU6)

Figure 3-12 shows a global view of the functional blocks of two Capture/Compare Units (CCU60 and CCU61).

Both of the CCU6 modules are further supplied with clock control, interrupt control, address decoding, and port control logic. One DMA request can be generated by each CCU6 module.

Each CCU6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features:

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Features:

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported

Additional Features:

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

3.25 Power Supply

The TC1130 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-18 shows the TC1130's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

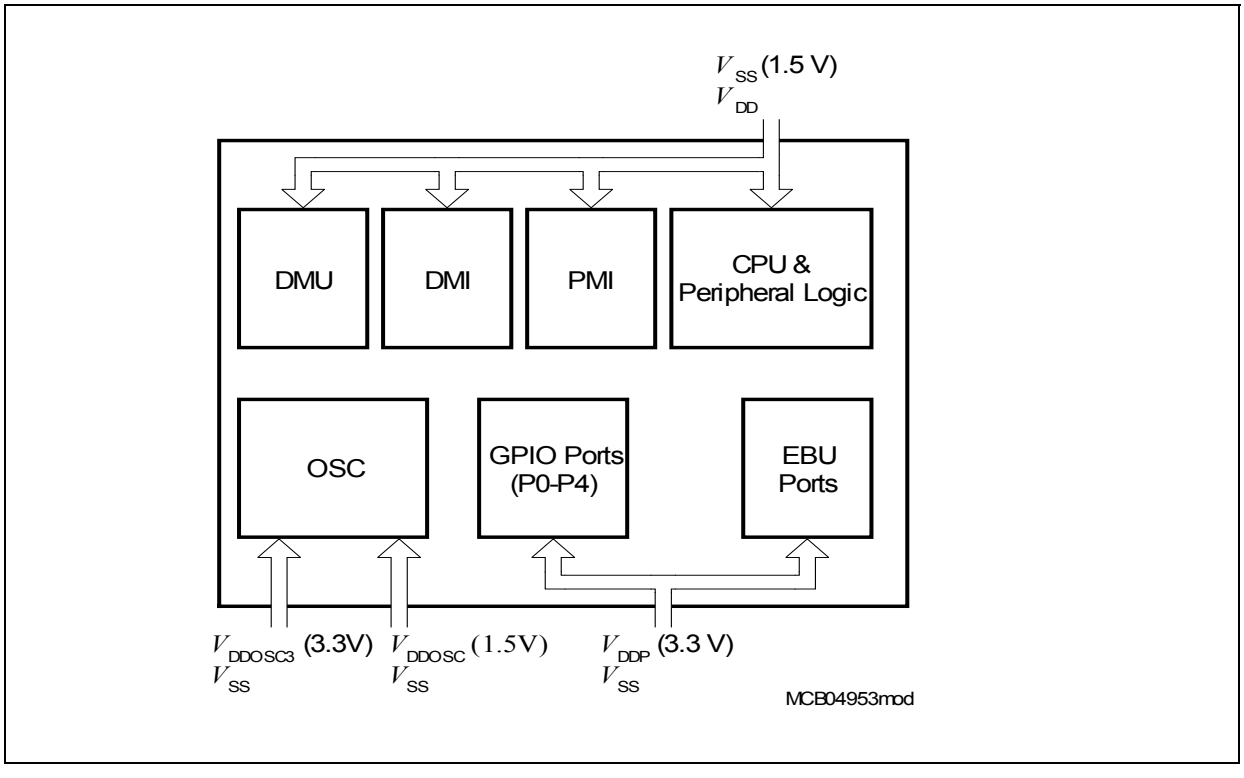

Figure 3-18 TC1130 Power Supply Concept

3.26 Power Sequencing

During power-up, reset pin $\overline{\text{PORST}}$ has to be held active until both power supply voltages have reached at least their minimum values.

During the power-up time (rising of the supply voltages from 0 to their regular operating values), it must be ensured that the core V_{DD} power supply reaches its operating value first, and then followed by the GPIO V_{DDP} power supply. During the rising time of the core voltage, it must be ensured that $0 < V_{DD}-V_{DDP} < 0.5$ V.

During power-down, the core power supply V_{DD} and GPIO power supply V_{DDP} must be switched off completely until all capacitances are discharged to zero before the next power-up.

Note: The state of the pins are undefined when only the port voltage V_{DDP} is switched on.

4.2.4 IIC Characteristics

Each IIC Pin is an open drain output pin with different characteristics than other pins. The related characteristics are given in the following table.

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Output low voltage	V_{OL}	CC	–	0.4 0.6	V	3 mA sink current 6 mA sink current
Input high voltage[1)]	V_{IH}	SR	$0.7V_{DDP}$	$V_{DDP}+0.5$	V	–
Input low voltage[1)]	V_{IL}	SR	-0.5	$0.3V_{DDP}$	V	–

1) Not subject to production test, verified by design/characterization.

Note: No 5 V IIC interface is supported with these pads. Only voltages lower than 3.63 V must be applied to these pads.

Note: IIC pins have no pull-up and pull-down devices.

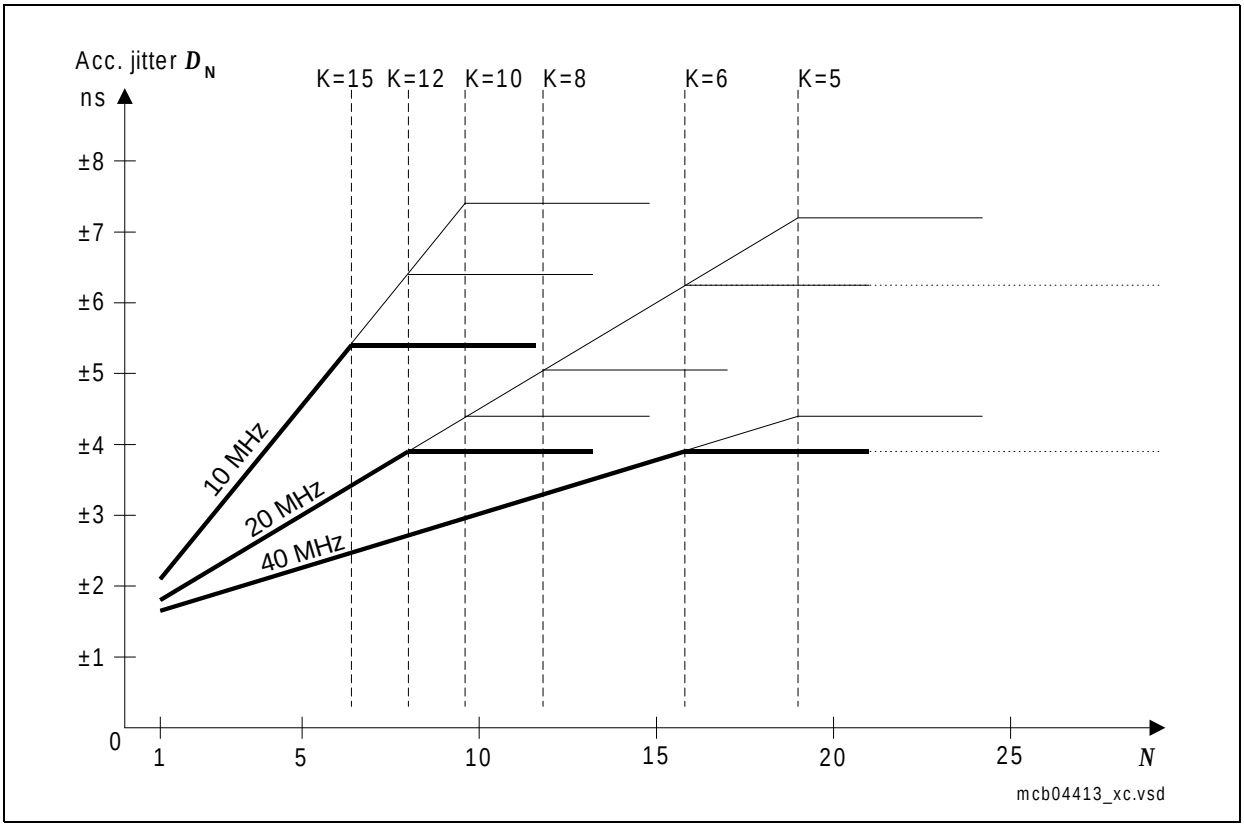

Figure 4-3 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

Table 4-1 VCO Bands for PLL Operation

PLL_CLC.VCOSEL	VCO Frequency Range	Base Frequency Range [1]
00	400 ... 500 MHz	250 ... 320 MHz
01	500 ... 600 MHz	300 ... 400 MHz
10	600 ... 700 MHz	350 ... 480 MHz
11	Reserved [2]	

[1] Base Frequency Range is the free running operation frequency of the PLL, when no input clock is available.

[2] This option cannot be used.

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	29	–	ns
TCK clock rise time	t_3	SR	–	0.4	ns
TCK clock fall time	t_4	SR	–	0.4	ns

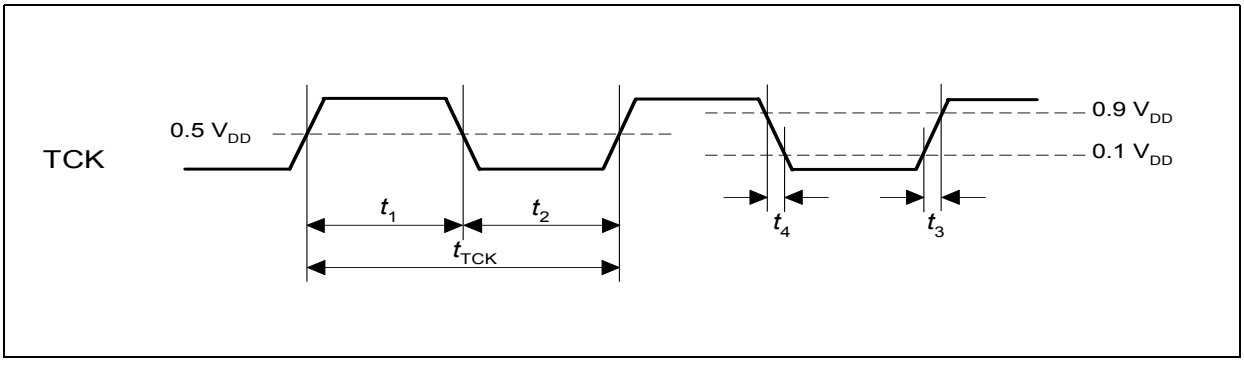

Figure 4-7 TCK Clock Timing

Parameter	Symbol		Limits		Unit
			min	max	
TMS setup to TCK ↑	t_1	SR	7.85	–	ns
TMS hold to TCK ↑	t_2	SR	3.0	–	ns
TDI setup to TCK ↑	t_1	SR	10.9	–	ns
TDI hold to TCK ↑	t_2	SR	3.0	–	ns
TDO valid output from TCK ↓	t_3	CC	–	10.7	ns
TDO high impedance to valid output from TCK ↓	t_4	CC	–	23.0	ns
TDO valid output to high impedance from TCK ↓	t_5	CC	–	26.0	ns

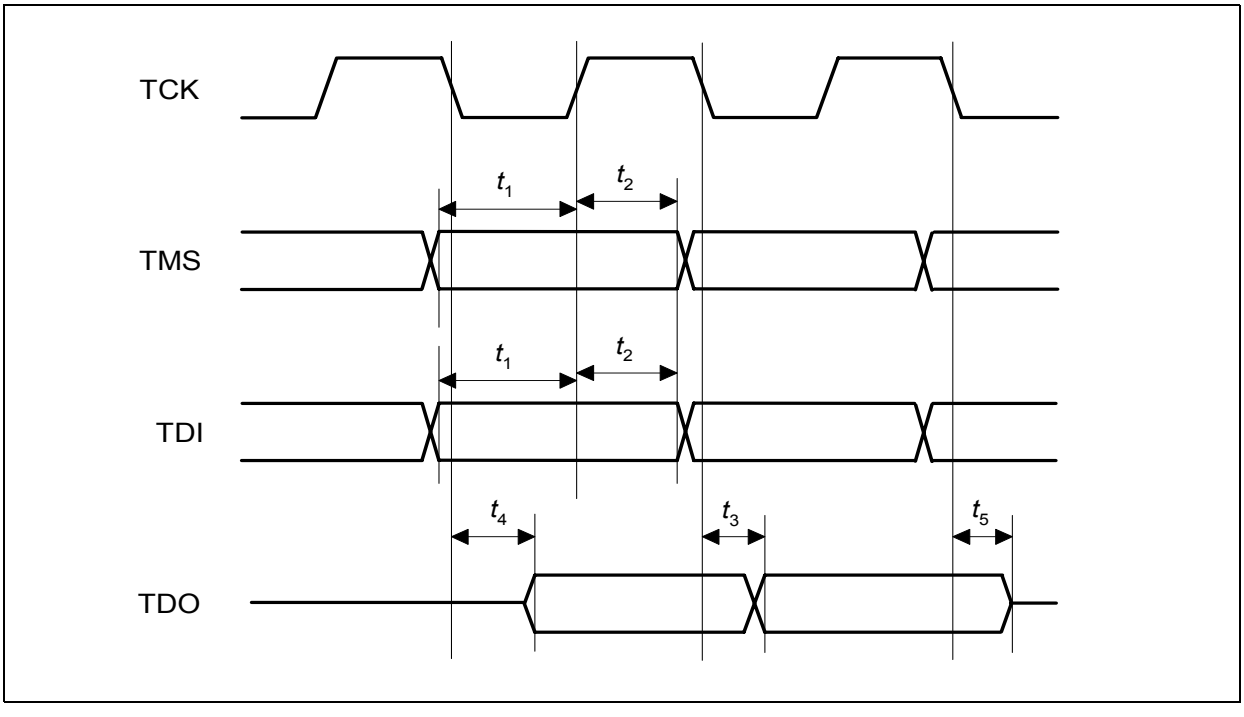

Figure 4-8 JTAG Timing

4.3.8.4 Timing for Burst Flash Access Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
Address output valid time from BFCLKO	t_1	CC	–	11.0	ns
Address output hold time from BFCLKO	t_2	CC	10.0	–	ns
$\overline{\text{CSx}}$ output valid time from BFCLKO	t_3	CC	–	9.0	ns
$\overline{\text{RD}}$ output valid time from BFCLKO	t_4	CC	–	10.0	ns
$\overline{\text{ADV}}$ output valid time from BFCLKO	t_5	CC	–	10.0	ns
$\overline{\text{ADV}}$ output hold time from BFCLKO	t_6	CC	3.0	–	ns
$\overline{\text{BAA}}$ output valid time from BFCLKO	t_7	CC	–	10.0	ns
$\overline{\text{BAA}}$ output hold time from BFCLKO	t_8	CC	3.0	–	ns
AD(31:0) input setup time to BFCLKO	t_9	SR	5.0	–	ns
AD(31:0) input hold time from BFCLKO	t_{10}	SR	3.0	–	ns
$\overline{\text{WAIT}}$ input setup time to BFCLKO	t_{11}	SR	5.0	–	ns
$\overline{\text{WAIT}}$ input hold time from BFCLKO	t_{12}	SR	3.0	–	ns

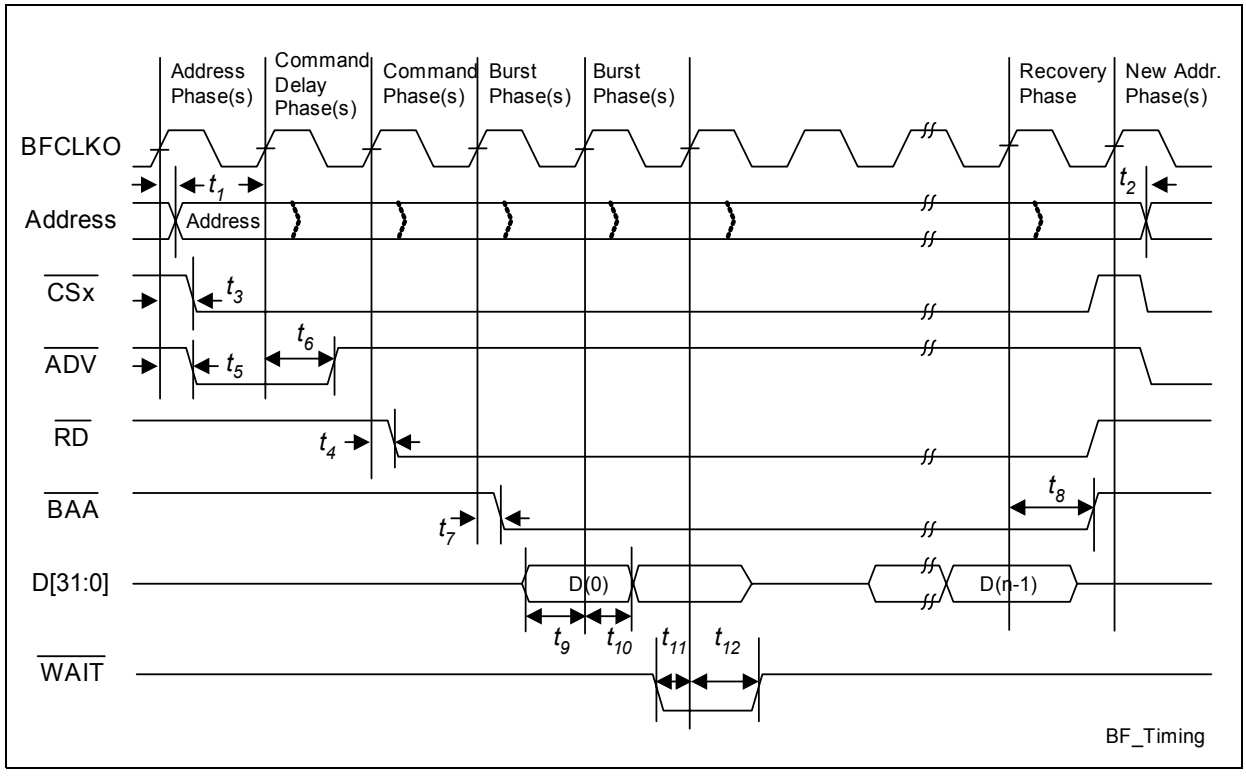

Figure 4-12 Burst Flash Access Timing

Note: Output delays are always referenced to BFCLKO. The reference clock for input characteristics depends on bit BFCON.FDBKEN.
BFCON.FDBKEN = 0: BFCLKO is the input reference clock.
BFCON.FDBKEN = 1: BFCLKI is the input reference clock (EBULMB clock feedback enabled).

4.3.8.6 Timing for Multiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF)[1)]

Parameter	Symbol		Limits		Unit
			min	max	
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output valid time from output clock ↑	t_1	CC	–	9	ns
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output hold time from output clock ↑	t_2	CC	0.0	–	ns
AD(31:0) output valid time from output clock ↑	t_3	CC	–	9	ns
AD(31:0) output hold time from output clock ↑	t_4	CC	0.0	–	ns
AD(31:0) input setup time to output clock ↑	t_5	SR	1.4	–	ns
AD(31:0) input hold time from output clock ↑	t_6	SR	3	–	ns
$\overline{\text{WAIT}}$ input setup time to output clock ↑	t_9	SR	12	–	ns
$\overline{\text{WAIT}}$ input hold time from output clock ↑	t_{10}	SR	3	–	ns
$\overline{\text{RMW}}$ output valid time from output clock ↑	t_{11}	CC	–	8	ns
$\overline{\text{RMW}}$ output hold time from output clock ↑	t_{12}	CC	1.3	–	ns
ALE width	t_{13}	CC	8.5	–	ns
AD(31:0) output hold time from RD/$\overline{\text{WR}}$ ↑	t_{14}	CC	0	–	ns

1) The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU Specification.

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