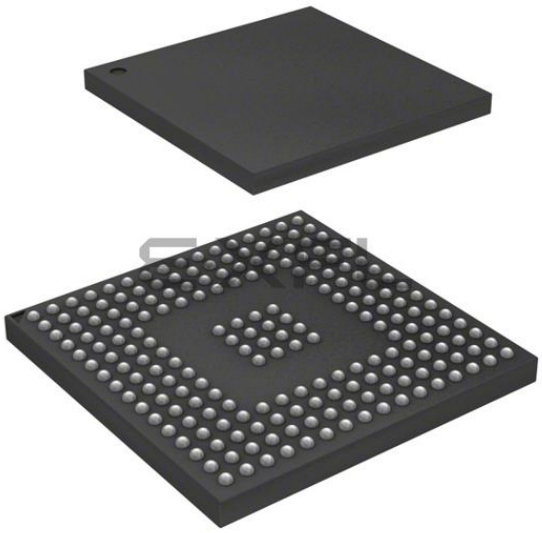
Infineon Technologies - SAF-TC1130-L150EB BB Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/saf-tc1130-l150eb-bb

TC1130 Data Sheet
Advance Information
Revision History: 2005-02 V1.0

Previous Version: none

Page	Subjects (major changes since last revision)

Controller Area Network (CAN): License of Robert Bosch GmbH

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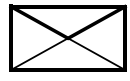


2.4 Pin Definitions and Functions

Table 2-1 Pin Definitions and Functions

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P0		I/O		**Port 0** Port 0 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for GPTU, MultiCAN, ASC1/2, SSC0/1, MLI0, EBU and SCU.	
P0.0	N11	I/O	PUC	GPTU_0	GPTU input/output line 0
		I/O		RXD1B	ASC1 receiver input/output B
P0.1	P15	I/O	PUC	GPTU_1	GPTU input/output line 1
		O		TXD1B	ASC1 transmitter output B
P0.2	P10	I/O	PUC	GPTU_2	GPTU input/output line 2
		I/O		RXD2B	ASC2 receiver input/output B
P0.3	M15	I/O	PUC	GPTU_3	GPTU input/output line 3
		O		TXD2B	ASC2 transmitter output B
P0.4	R11	I/O	PUC	GPTU_4	GPTU input/output line 4
		I		SLSI1	SSC1 Slave Select input
		O		BREQ	EBU Bus Request Output
P0.5	R12	I/O	PUC	GPTU_5	GPTU input/output line 5
		I		HOLD	EBU Hold Request Input
		I		CC60_T12HR	CCU60 Timer 12 hardware run
		O		BRKOUT_B	OCDS Break Out B
P0.6	R10	I/O	PUC	GPTU_6	GPTU input/output line 6
		I/O		HLDA	EBU Hold Acknowledge Input/Output
		I		CC60_T13HR	CCU60 Timer 13 hardware run
		O		SLSO0_0	SSC0 Slave Select output 0
P0.7	N10	I/O	PUC	GPTU_7	GPTU input/output line 7
		O		SLSO1_0	SSC1 Slave Select output 0
P0.8	R13	I	PUC	RXDCAN0_A	CAN node 0 receiver input A
		I		REQ0	External Trigger Input 0
		O		TCLK0A	MLI0 transmit channel clock output A
P0.9	R15	O	PUC	TXDCAN0_A	CAN node 0 transmitter output A
		I		TREADY0A	MLI0 transmit channel ready input A
		I		REQ1	External Trigger Input 1
P0.10	R14	I	PUC	RXDCAN1_A	CAN node 1 receiver input A
		I		REQ2	External Trigger Input 2
		O		TVALID0A	MLI0 transmit channel valid output A
P0.11	N9	O	PUC	TXDCAN1_A	CAN node 1 transmitter output A
		I		REQ3	External Trigger Input 3
		O		TDATA0A	MLI0 transmit channel data output A

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P2		I/O		**Port 2** Port 2 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for ASC0/1/2, SSC0/1, CCU60, IIC, EBU and SCU.	
P2.0	P12	I/O	PUC	RXD0	ASC0 receiver input/output line
		O		CSEMU	EBU Chip Select Output for Emulator Region
P2.1	P11	O	PUC	TXD0	ASC0 transmitter output line
		I		TESTMODE	Test Mode Select Input
P2.2	P13	I/O	PUC	MRST0	SSC0 master receive/slave transmit input/output
P2.3	P14	I/O	PUC	MTSR0	SSC0 master transmit/slave receive input/output
P2.4	N15	I/O	PUC	SCLK0	SSC0 clock input/output line
P2.5	N14	O	PUC	COUT60_3	CCU60 compare channel 3 output
		I/O		MRST1A	SSC1 master receive/slave transmit input/output A
P2.6	N12	I/O	PUC	CC60_0	CCU60 input/output of capture compare channel 0
		I/O		MTSR1A	SSC1 master transmit/slave receive input/output A
P2.7	K16	O	PUC	COUT60_0	CCU60 output of capture/compare channel 0
		I/O		SCLK1A	SSC1 clock input/output line A
P2.8	J16	I/O	PUC	CC60_1	CCU60 input/output of capture/ compare channel 1
		I/O		RXD1A	ASC1 receiver input/output line A
P2.9	H16	O	PUC	COUT60_1	CCU60 output of capture/compare channel 1
		O		TXD1A	ASC1 transmitter output line A
P2.10	L13	I/O	PUC	CC60_2	CCU60 input/output of capture/ compare channel 2
		I/O		RXD2A	ASC2 receiver input/output line A
P2.11	G16	O	PUC	COUT60_2	CCU60 output of capture/compare channel 2
		O		TXD2A	ASC2 transmitter output line A
P2.12	K15	I/O	—	SDA0	IIC Serial Data line 0
		I		CTRAP0	CCU60 trap input
		O		SLSO0_3	SSC0 Slave Select output 3

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P4		I/O		**Port 4** Port 4 is an 8-bit bi-directional general purpose I/O port which can be alternatively used for USB, MLI0 and SCU.
P4.0	R8	I	PUC	USBCLK 48 MHz input clock
		O		TCLK0B MLI0 transmit channel clock output B
P4.1	R9	I	PUC	RCVI USB data input
		I		TREADY0B MLI0 transmit channel ready input B
P4.2	N7	I	PUC	VPI USB D+ CMOS level mirror of differential signal
		O		TVALID0B MLI0 transmit channel valid output B
P4.3	N6	I	PUC	VMI USB D- CMOS level mirror of differential signal
		O		TDATA0B MLI0 transmit channel data output B
P4.4	P6	O	PUC	VPO USB D+ CMOS level output
		I		RCLK0B MLI0 receive channel clock input B
P4.5	R7	O	PUC	VMO USB D- CMOS level output
		O		RREADY0B MLI0 receive channel ready output B
P4.6	R6	O	PUC	USBOE Direction select for transmit or receive
		I		RVALID0B MLI0 receive channel valid input B
P4.7	P5	I	PUC	RDATA0B MLI0 receive channel data input B
		O		BRKOUT_A OCDS Break Out A
HDRST	N5	I/O	PUA	**Hardware Reset Input/Reset Indication Output** Assertion of this bi-directional open-drain pin causes a synchronous reset of the chip through external circuitry. This pin must be driven for a minimum 4 f_{CPU} clock cycles. The internal reset circuitry drives this pin in response to a power-on, hardware, watchdog and power-down wake-up reset for a specific period of time. For a software reset, activation of this pin is programmable.
PORST	R5	I	PUC	**Power-on Reset Input** A low level on PORST causes an asynchronous reset of the entire chip. PORST is a fully asynchronous level sensitive signal.
NMI	T7	I	PUC	**Non-Maskable Interrupt Input** A high-to-low transition on this pin causes an NMI-Trap request to the CPU.

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address/Data Bus Input/Output Lines
AD0	C8	I/O	PUC	EBU Address/Data Bus Line 0
AD1	C7	I/O	PUC	EBU Address/Data Bus Line 1
AD2	B6	I/O	PUC	EBU Address/Data Bus Line 2
AD3	C6	I/O	PUC	EBU Address/Data Bus Line 3
AD4	C5	I/O	PUC	EBU Address/Data Bus Line 4
AD5	A3	I/O	PUC	EBU Address/Data Bus Line 5
AD6	A2	I/O	PUC	EBU Address/Data Bus Line 6
AD7	C3	I/O	PUC	EBU Address/Data Bus Line 7
AD8	C2	I/O	PUC	EBU Address/Data Bus Line 8
AD9	D2	I/O	PUC	EBU Address/Data Bus Line 9
AD10	F1	I/O	PUC	EBU Address/Data Bus Line 10
AD11	E3	I/O	PUC	EBU Address/Data Bus Line 11
AD12	F3	I/O	PUC	EBU Address/Data Bus Line 12
AD13	G1	I/O	PUC	EBU Address/Data Bus Line 13
AD14	H2	I/O	PUC	EBU Address/Data Bus Line 14
AD15	G3	I/O	PUC	EBU Address/Data Bus Line 15
AD16	D7	I/O	PUC	EBU Address/Data Bus Line 16
AD17	B5	I/O	PUC	EBU Address/Data Bus Line 17
AD18	A4	I/O	PUC	EBU Address/Data Bus Line 18
AD19	B4	I/O	PUC	EBU Address/Data Bus Line 19
AD20	C4	I/O	PUC	EBU Address/Data Bus Line 20
AD21	B3	I/O	PUC	EBU Address/Data Bus Line 21
AD22	B2	I/O	PUC	EBU Address/Data Bus Line 22
AD23	B1	I/O	PUC	EBU Address/Data Bus Line 23
AD24	C1	I/O	PUC	EBU Address/Data Bus Line 24
AD25	D3	I/O	PUC	EBU Address/Data Bus Line 25
AD26	E2	I/O	PUC	EBU Address/Data Bus Line 26
AD27	F2	I/O	PUC	EBU Address/Data Bus Line 27
AD28	F4	I/O	PUC	EBU Address/Data Bus Line 28
AD29	G4	I/O	PUC	EBU Address/Data Bus Line 29
AD30	H3	I/O	PUC	EBU Address/Data Bus Line 30
AD31	G2	I/O	PUC	EBU Address/Data Bus Line 31
$\overline{\text{BC0}}$	A5	O	PUC	**EBU Byte Control Line 0**
$\overline{\text{BC1}}$	A6	O	PUC	**EBU Byte Control Line 1**
$\overline{\text{BC2}}$	B7	O	PUC	**EBU Byte Control Line 2**
BC3	A7	O	PUC	**EBU Byte Control Line 3**

3 Functional Description

3.1 On-Chip Memories

The TC1130 provides the following on-chip memories:

- Program Memory Interface (PMI) with
  - 32-Kbyte Scratch-pad Code RAM (SPRAM)
  - 16-Kbyte Instruction Cache Memory (ICACHE)
- Data Memory Interface (DMI) with
  - 28-Kbyte Scratch-pad Data RAM (SPRAM)
  - 4-Kbyte Data Cache Memory (DCACHE)
- Data Memory Unit (DMU) with
  - 64-Kbyte SRAM
- 16-Kbyte Boot ROM (BROM)

Table 3-1 TC1130 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

- Evaluation of the device address in slave mode
- Bus access arbitration in multimaster mode

Features:

- Extended buffer allows up to 4 send/receive data bytes to be stored
- Selectable baud rate generation
- Support of standard 100 kBaud and extended 400 kBaud data rates
- Operation in 7-bit addressing mode or 10-bit addressing mode
- Flexible control via interrupt service routines or by polling
- Dynamic access to up to 2 physical IIC buses

3.12 Universal Serial Bus Interface (USB)

Figure 3-8 shows a global view of the functional blocks of the Universal Serial Bus interface (USB).

The USB module is further supplied with clock control, interrupt control, address decoding, and port control logic. One DMA request can be generated by USB module.

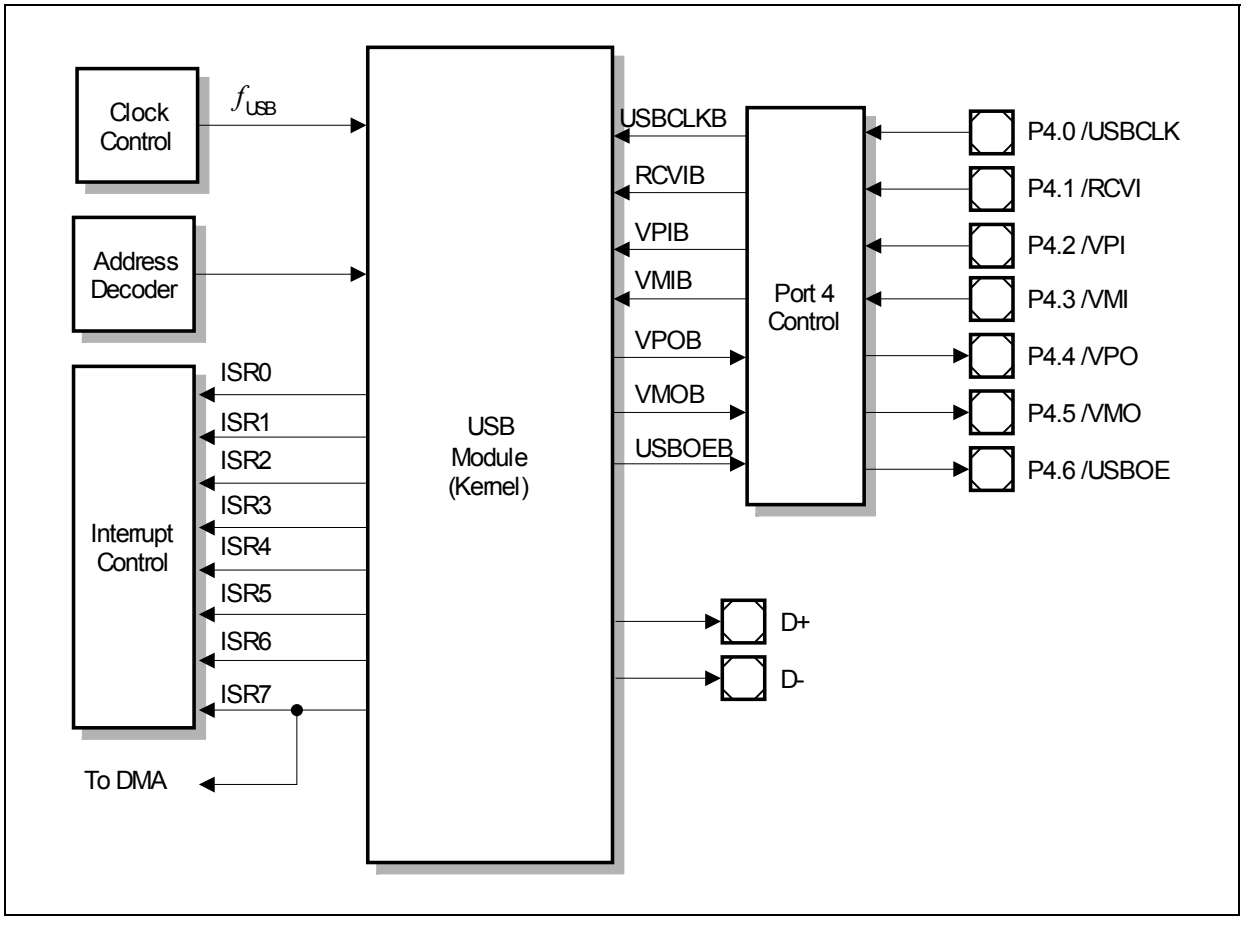


Figure 3-8 General Block Diagram of the USB Interface

The USB handles all transactions between the serial USB bus and the internal (parallel) bus of the microcontroller. The USB module includes several units which are required to support data handling with the USB bus: the on-chip USB transceiver (optionally), the flexible USB buffer block with a 32-bit wide RAM, the buffer control unit with sub modules for USB and CPU memory access control, the UDC_IF device interface for USB protocol handling, the microcontroller interface unit (MCU) with the USB specific special function registers and the interrupt generation unit. A clock generation unit provides the clock signal for the USB module for full speed and low speed USB operation.

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

Features:

- Compliant to ISO 11898
- CAN functionality according to CAN specification V2.0 B (active)
- Dedicated control registers are provided for each CAN node
- A data transfer rate up to 1 MBaud is supported
- Flexible and powerful message transfer control and error handling capabilities are implemented
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter
- Full-CAN functionality: A set of 128 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between two different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed at any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.

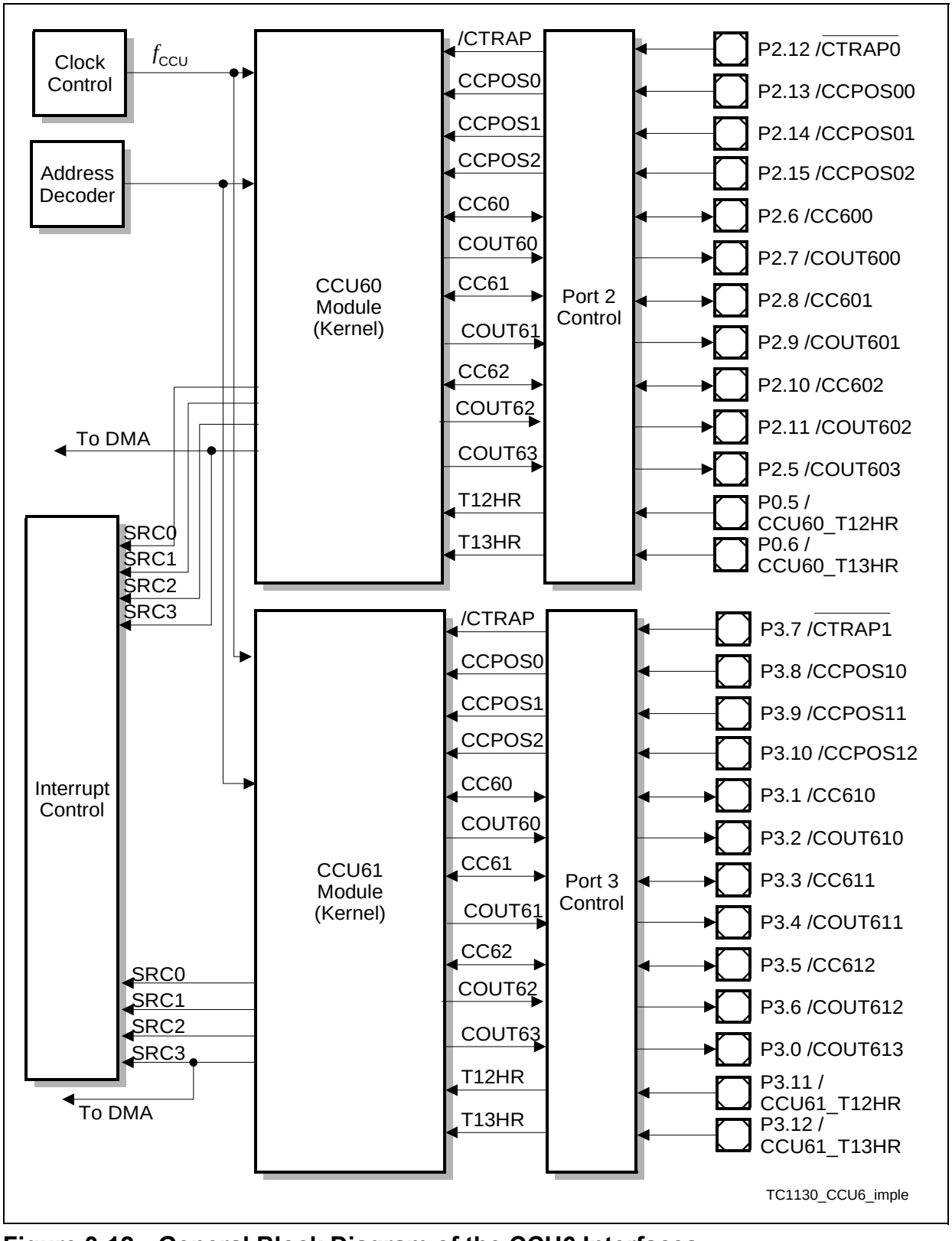


Figure 3-12 General Block Diagram of the CCU6 Interfaces

3.25 Power Supply

The TC1130 provides an ingenious power supply concept in order to improve the EMI behavior as well as to minimize the crosstalk within on-chip modules.

Figure 3-18 shows the TC1130's power supply concept, where certain logic modules are individually supplied with power. This concept improves the EMI behavior by reduction of the noise cross coupling.

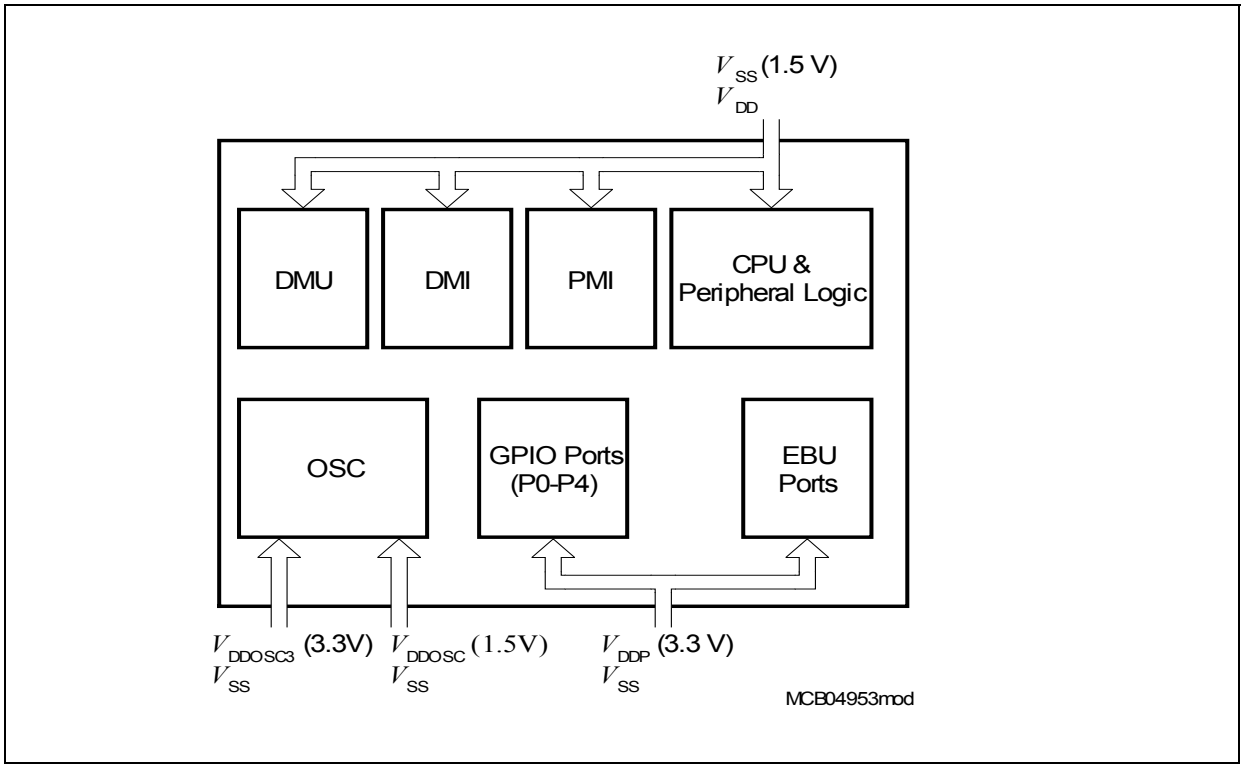


Figure 3-18 TC1130 Power Supply Concept

4.2 DC Parameters

4.2.1 Input/Output Characteristics

V_{SS} = 0 V; T_A = -40°C to +125°C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
GPIO pins, Dedicated pins and EBU pins						
Input low voltage	V_{IL}	SR	-0.3	0.8	V	LvTTL
Input high voltage	V_{IH}	SR	2.0	V_{DDP} + 0.3	V	LvTTL
Output low voltage	V_{OL}	CC	–	0.4	V	I_{OL} = 2mA
Output high voltage	V_{OH}	CC	2.4	–	V	I_{OH} = -2mA
Pull-up current [1]	$\|I_{PUA}\|$	CC	–	149	µA	V_{IN} = 0V
	$\|I_{PUC}\|$	CC	–	7.2	µA	V_{IN} = 0V
Pull-down current [2]	$\|I_{PDA}\|$	CC	–	156	µA	V_{IN} = V_{DDP}
	$\|I_{PDC}\|$	CC	–	15.7	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ1}	CC	–	±350	nA	0 < V_{IN} < V_{DDP}
Pin Capacitance [4]	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) The current is applicable to the pins, for which a pull-up has been specified. Refer to **Table 2-1**. I_{PUx} refers to the pull-up current for type *x in absolute values*.

2) The current is applicable to the pins, for which a pull-down has been specified. Refer to **Table 2-1**. I_{PDx} refers to the pull-down current for type *x in absolute values*.

3) Excluded following pins: $\overline{\text{NMI}}$, $\overline{\text{TRST}}$, TCK, TDI, TMS, MII_TXCLK, MII_RXCLK, MII_MDIO, ALE, P2.1,HWCFG0, HWCFG1, HWCFG2, BRKIN, PORST, HDRST.

4) Not subject to production test, verified by design/characterization.

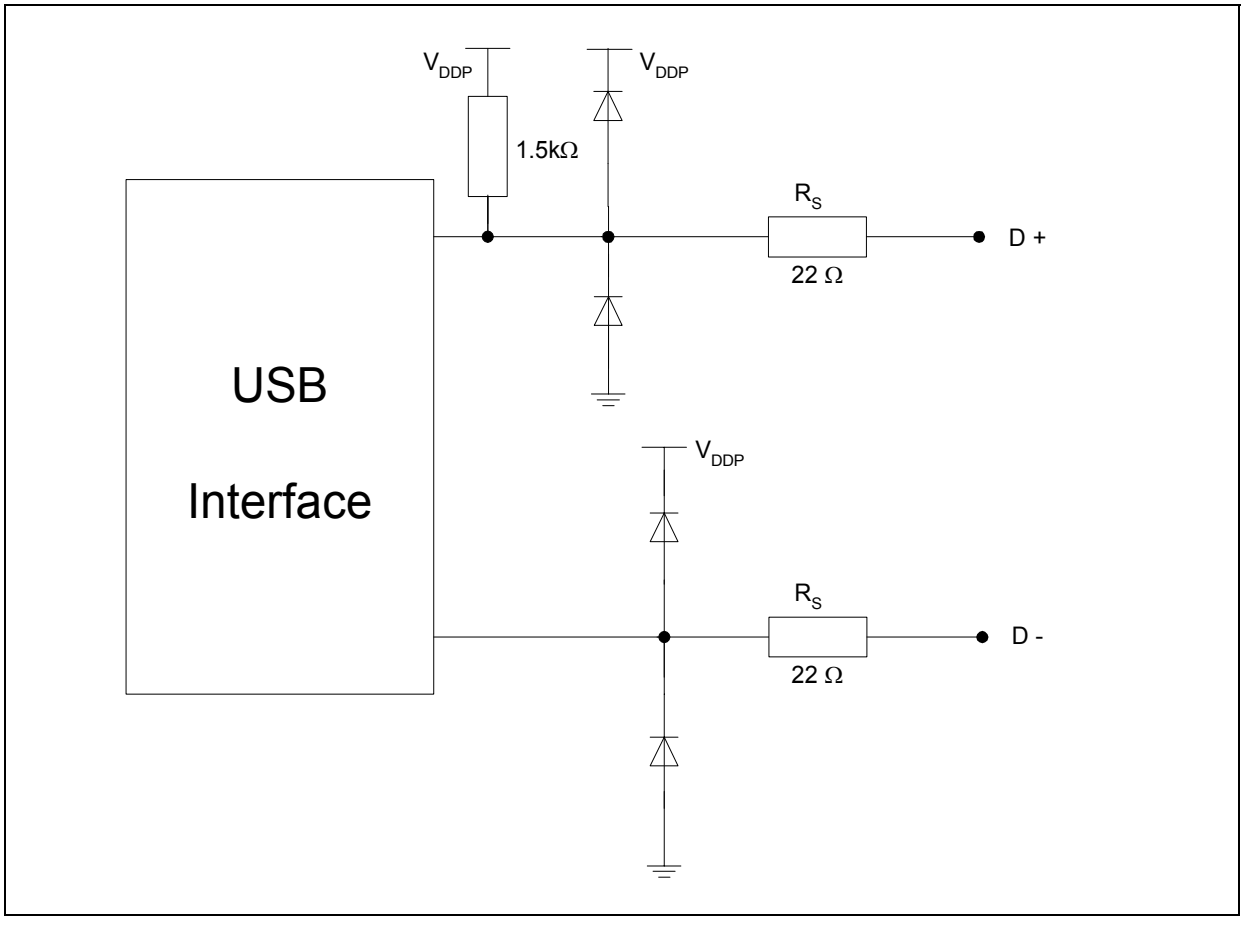


Figure 4-1 USB Interface

4.3.6 Timing for JTAG Signals

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
TCK clock period	t_{TCK}	SR	50	–	ns
TCK high time	t_1	SR	10	–	ns
TCK low time	t_2	SR	29	–	ns
TCK clock rise time	t_3	SR	–	0.4	ns
TCK clock fall time	t_4	SR	–	0.4	ns

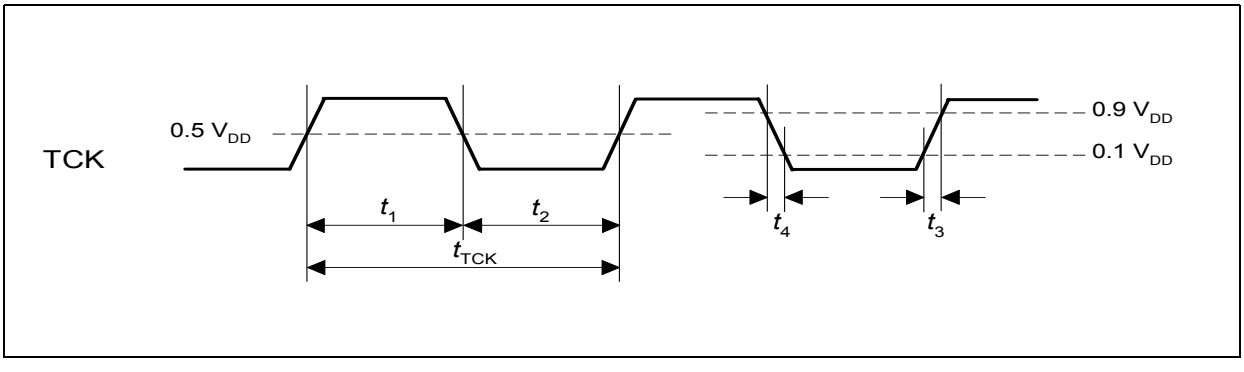


Figure 4-7 TCK Clock Timing

Parameter	Symbol		Limits		Unit
			min	max	
TMS setup to TCK ↑	t_1	SR	7.85	–	ns
TMS hold to TCK ↑	t_2	SR	3.0	–	ns
TDI setup to TCK ↑	t_1	SR	10.9	–	ns
TDI hold to TCK ↑	t_2	SR	3.0	–	ns
TDO valid output from TCK ↓	t_3	CC	–	10.7	ns
TDO high impedance to valid output from TCK ↓	t_4	CC	–	23.0	ns
TDO valid output to high impedance from TCK ↓	t_5	CC	–	26.0	ns

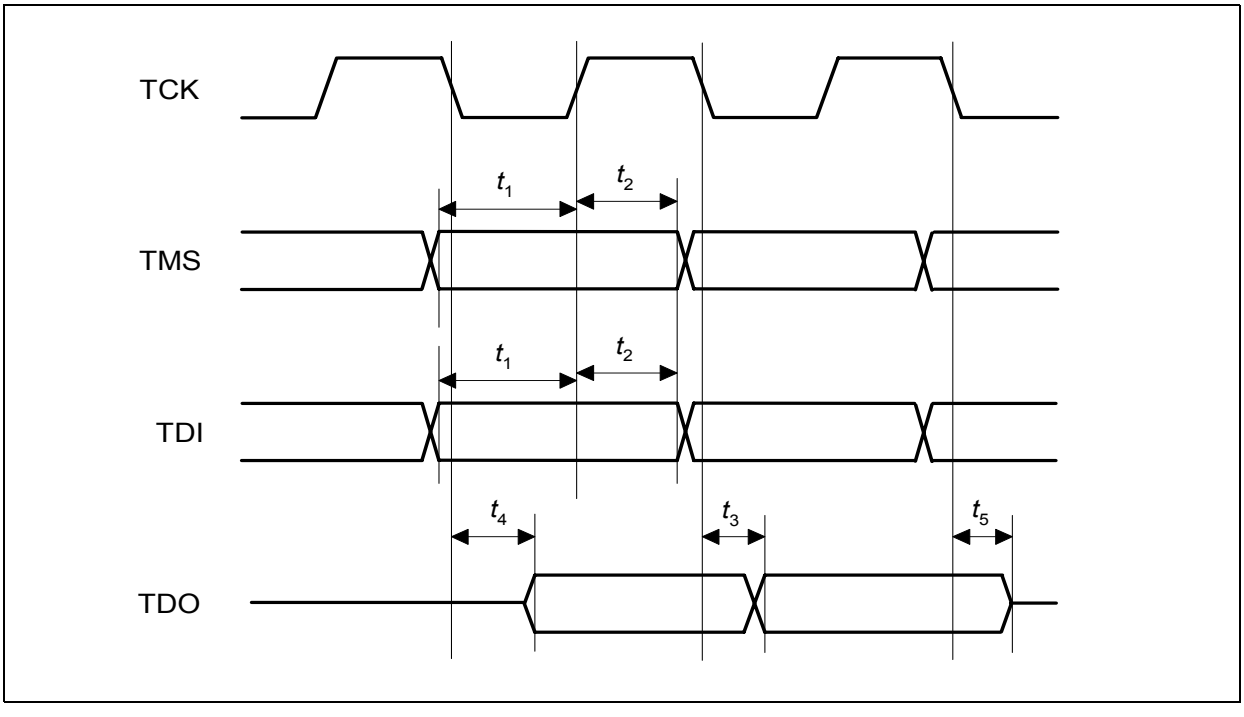
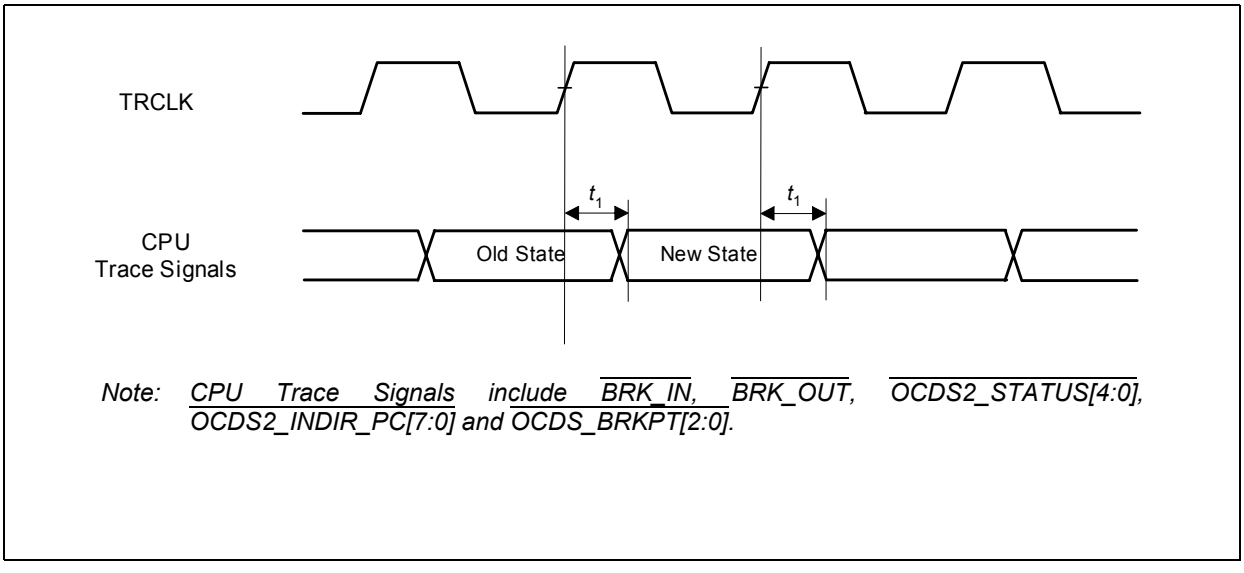


Figure 4-8 JTAG Timing

4.3.7 Timing for OCDS Trace and Breakpoint Signals

(Operating Conditions apply; C_L(TRCLK) = 25 pF, C_L = 50 pF)

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{\text{BRK\_OUT}}$ valid from TRCLK ↓	t_1	CC	–	5.2	ns
$\overline{\text{OCDS2\_STATUS[4:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns
$\overline{\text{OCDS2\_BRKPT[2:0]}}$ valid from TRCLK ↓	t_1	CC	0	5	ns



Note: CPU Trace Signals include $\overline{\text{BRK\_IN}}$, $\overline{\text{BRK\_OUT}}$, $\overline{\text{OCDS2\_STATUS[4:0]}}$, $\overline{\text{OCDS2\_INDIR\_PC[7:0]}}$ and $\overline{\text{OCDS\_BRKPT[2:0]}}$.

Figure 4-9 OCDS Trace Signals Timing

4.3.8.5 Timing for Demultiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF) [1)]

Parameter	Symbol		Limits		Unit
			min	max	
$\overline{CSx}$, RD/$\overline{WR}$, $\overline{RD}$, MR/$\overline{W}$, $\overline{BC(3:0)}$ output valid time from output clock	t_1	CC	–	9	ns
$\overline{CSx}$, RD/$\overline{WR}$, $\overline{RD}$, MR/$\overline{W}$, $\overline{BC(3:0)}$ output hold time from output clock	t_2	CC	0.0	–	ns
Address output valid time from output clock	t_3	CC	–	9	ns
Address output hold time from output clock	t_4	CC	0.0	–	ns
$\overline{WAIT}$ input setup time to output clock	t_7	SR	12	–	ns
$\overline{WAIT}$ input hold time from output clock	t_8	SR	3	–	ns
AD(31:0) output valid time from output clock	t_9	CC	–	9	ns
AD(31:0) output hold time from output clock	t_{10}	CC	0.0	–	ns
AD(31:0) input setup time to output clock	t_{11}	SR	1.3	–	ns
AD(31:0) input hold time from output clock	t_{12}	SR	3	–	ns
$\overline{RMW}$ output valid time from output clock	t_{13}	CC	–	8	ns
$\overline{RMW}$ output hold time from output clock	t_{14}	CC	1.3	–	ns
AD(31:0) output hold time from RD/$\overline{WR}$	t_{16}	CC	0	–	ns

1) The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU specification.

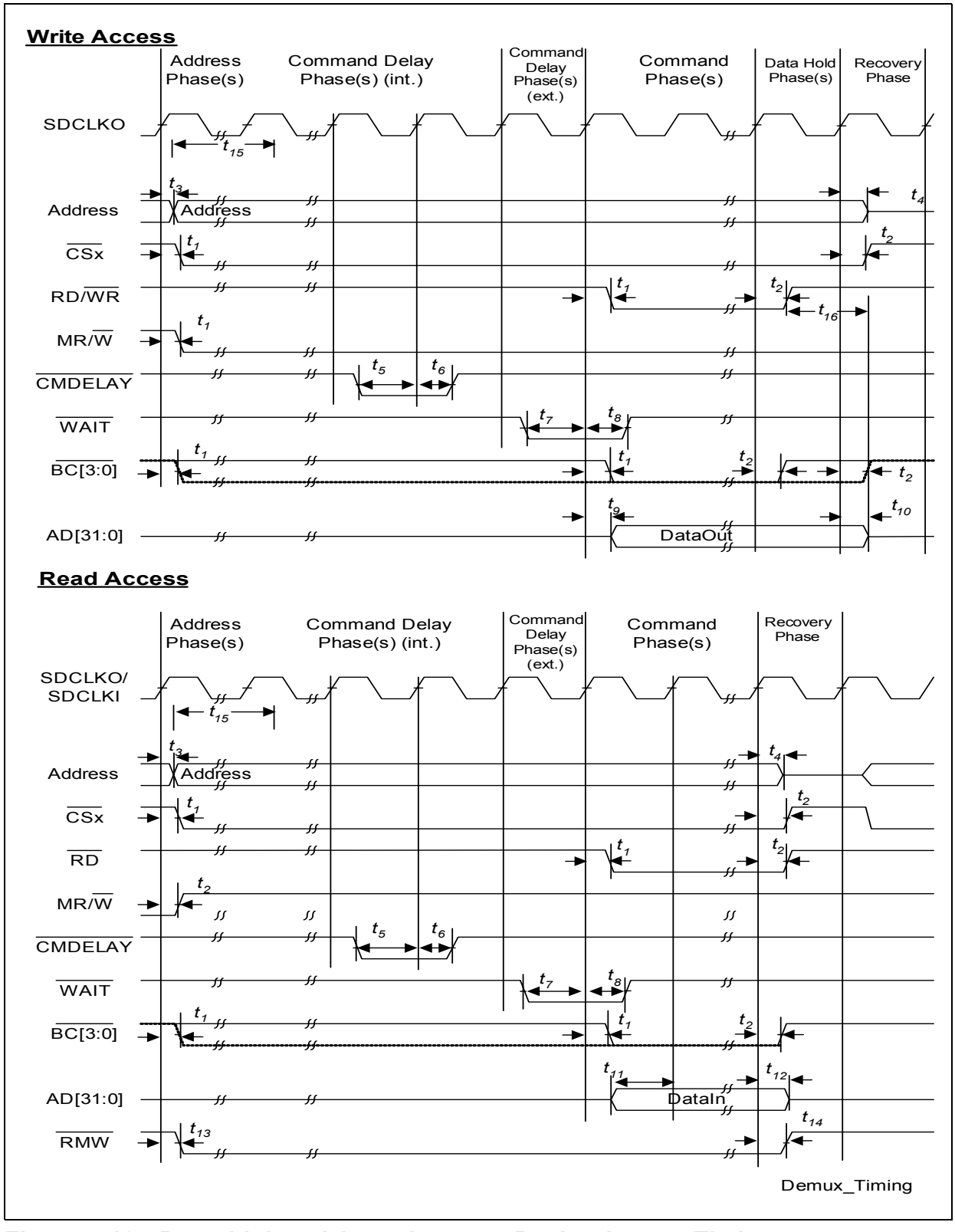


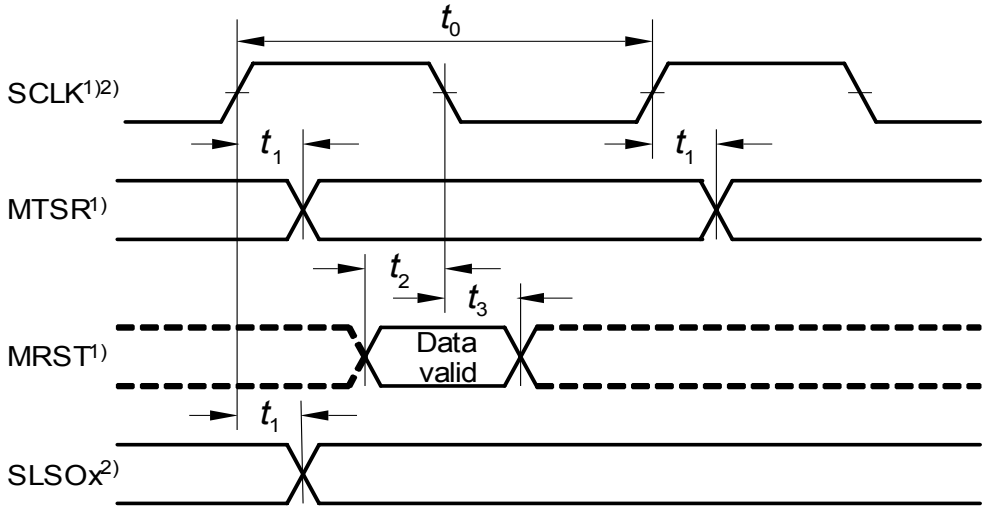
Figure 4-13 Demultiplexed Asynchronous Device Access Timing

4.3.9.2 SSC Master Mode Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock period	t_0	CC	2*T_{SSC} 1)	–	ns
MTSR/SLSOx delay from SCLK ↓	t_1	CC	0	8	ns
MRST setup to SCLK ↓	t_2	SR	10	–	ns
MRST hold from SCLK ↓	t_3	SR	5	–	ns

1) T_{SSCmin} = T_{SYS} = 1/f_{SYS}. When f_{SYS} = 120MHz, t_0 = 16.7ns



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOx is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_Tmg1

Figure 4-16 SSC Master Mode Timing