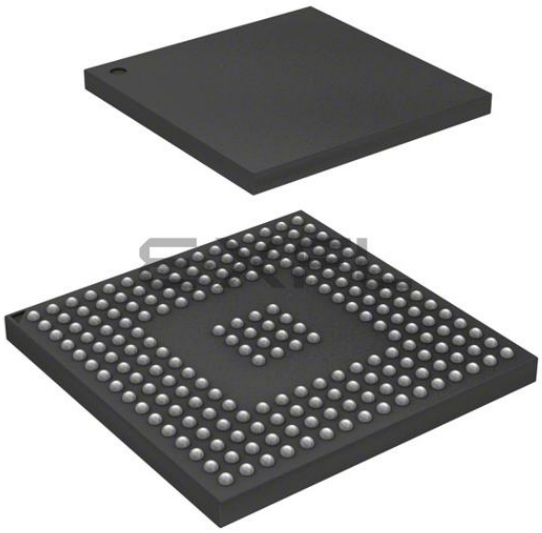
Infineon Technologies - TC1130L100EBGBBFXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1130l100ebgbbfxuma1

Edition 2005-02

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

2.3 Pin Configuration

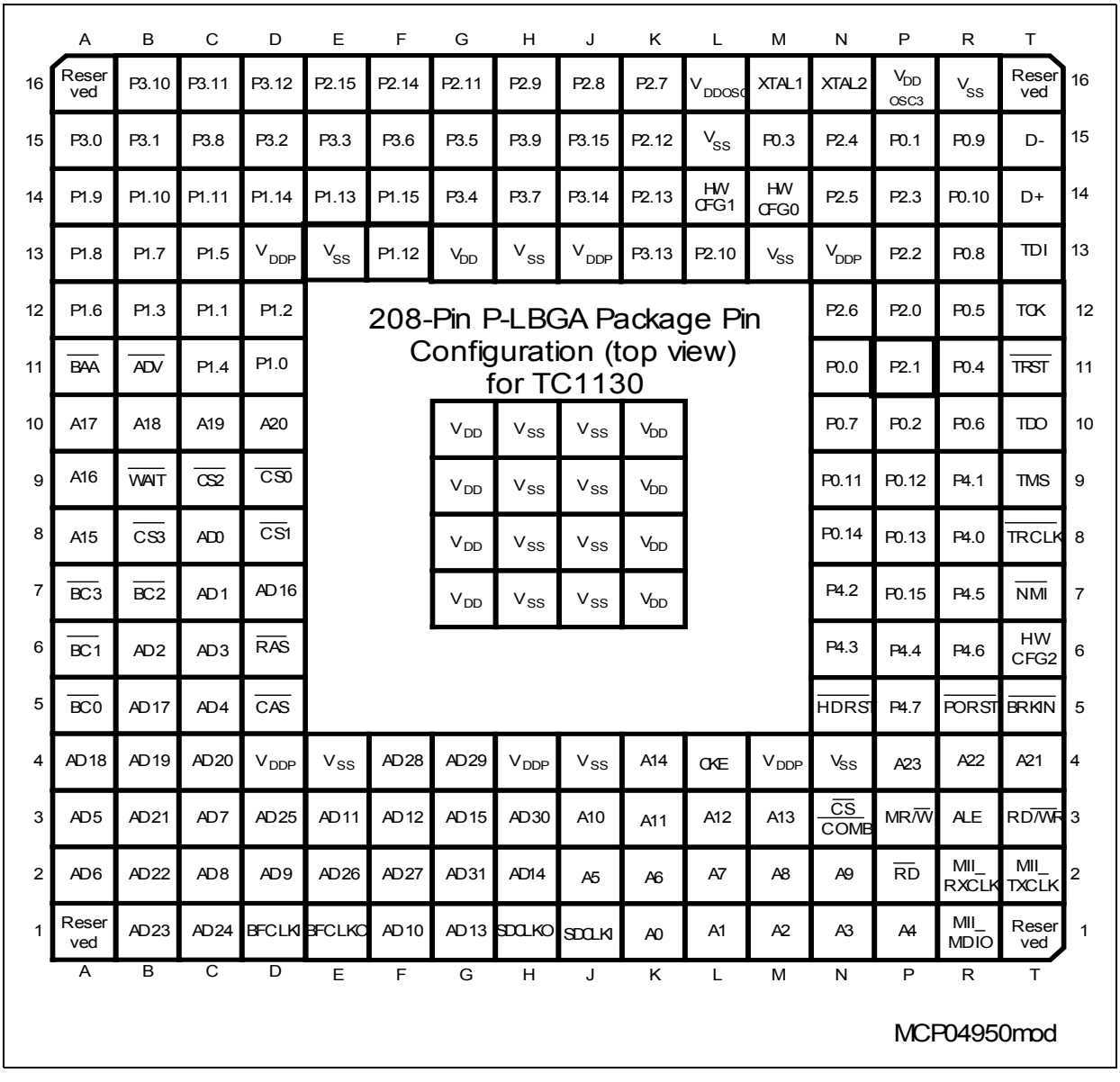


Figure 2-3 TC1130 Pins: P-BGA-208 Package (top view)

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P0.12	P9	I	PUC	RXDCAN2	CAN node 2 receiver input
		I		RCLK0A	MLI0 receive channel clock input A
		I		REQ4	External Trigger Input 4
P0.13	P8	O	PUC	TXDCAN2	CAN node 2 transmitter output
		I		REQ5	External Trigger Input 5
		O		RREADY0A	MLI0 receive channel ready output A
P0.14	N8	I	PUC	RXDCAN3	CAN node 3 receiver input
		I		REQ6	External Trigger Input 6
		I		RVALID0A	MLI0 receive channel valid input A
P0.15	P7	O	PUC	TXDCAN3	CAN node 3 transmitter output
		I		REQ7	External Trigger Input 7
		I		RDATA0A	MLI0 receive channel data input A

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P1.7	B13	I	PUC	MII_RXDV	Ethernet Controller receive data valid input line
		I		SWCFG7	Software configuration 7
		O		OCDSA_7	OCDS L2 Debug Line A7
P1.8	A13	I	PUC	MII_CRS	Ethernet Controller carrier input line
		I		SWCFG8	Software configuration 8
		O		OCDSA_8	OCDS L2 Debug Line A8
P1.9	A14	I	PUC	MII_COL	Ethernet Controller collision input line
		I		SWCFG9	Software configuration 9
		O		OCDSA_9	OCDS L2 Debug Line A9
P1.10	B14	I	PUC	MII_RXD0	Ethernet Controller receive data input line 0
		I		SWCFG10	Software configuration 10
		O		OCDSA_10	OCDS L2 Debug Line A10
P1.11	C14	I	PUC	MII_RXD1	Ethernet Controller receive data input line 1
		I		SWCFG11	Software configuration 11
		O		OCDSA_11	OCDS L2 Debug Line A1
		O		SLSO0_1	SSC0 Slave Select output 1
P1.12	F13	I	PUC	MII_RXD2	Ethernet Controller receive data input line 2
		I		SWCFG12	Software configuration 12
		O		OCDSA_12	OCDS L2 Debug Line A12
		O		SLSO1_1	SSC1 Slave Select output 1
P1.13	E14	I	PUC	MII_RXD3	Ethernet Controller receive data input line 3
		I		SWCFG13	Software configuration 13
		O		OCDSA_13	OCDS L2 Debug Line A13
		O		SLSO0_2	SSC0 Slave Select output 2
P1.14	D14	I	PUC	MII_RXER	Ethernet Controller receive error input line
		O		SLSO1_2	SSC1 Slave Select output 2
		I		SWCFG14	Software configuration 14
		O		OCDSA_14	OCDS L2 Debug Line A14
P1.15	F14	I	PUC	SLSI0	SSC0 Slave Select Input
		O		RMW	EBU Read Modify Write
		I		SWCFG15	Software configuration 15
		O		OCDSA_15	OCDS L2 Debug Line A15

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P3		I/O		**Port 3** Port 3 is a 16-bit bi-directional general purpose I/O port which can be alternatively used for MLI1, CCU61, SSC0/1 and OCDS Level 2 debug lines.	
P3.0	A15	O	PUC	OCDSB_0	OCDS L2 Debug Line B0
		O		COUT61_3	CCU61 compare channel 3 output
P3.1	B15	O	PUC	OCDSB_1	OCDS L2 Debug Line B1
		I/O		CC61_0	CCU61 input/output of capture/ compare channel 0
P3.2	D15	O	PUC	OCDSB_2	OCDS L2 Debug Line B2
		O		COUT61_0	CCU61 output of capture/compare channel 0
P3.3	E15	O	PUC	OCDSB_3	OCDS L2 Debug Line B3
		I/O		CC61_1	CCU61 input/output of capture/ compare channel 1
P3.4	G14	O	PUC	OCDSB_4	OCDS L2 Debug Line B4
		O		COUT61_1	CCU61 output of capture/compare channel 1
P3.5	G15	O	PUC	OCDSB_5	OCDS L2 Debug Line B5
		I/O		CC61_2	CCU61 input/output of capture/ compare channel 2
P3.6	F15	O	PUC	OCDSB_6	OCDS L2 Debug Line B6
		O		COUT61_2	CCU61 output of capture/compare channel 2
P3.7	H14	O	PUC	OCDSB_7	OCDS L2 Debug Line B7
		I		CTRAP1	CCU61 trap input
		O		SLSO0_5	SSC0 Slave Select output 5
P3.8	C15	O	PUC	OCDSB_8	OCDS L2 Debug Line B8
		I		CCPOS1_0	CCU61 Hall input signal 0
		O		TCLK1	MLI1 transmit channel clock output
		O		SLSO1_5	SSC1 Slave Select output 5
P3.9	H15	O	PUC	OCDSB_9	OCDS L2 Debug Line B9
		I		CCPOS1_1	CCU61 Hall input signal 1
		I		TREADY1	MLI1 transmit channel ready input
		O		SLSO0_6	SSC0 Slave Select output 6
P3.10	B16	O	PUC	OCDSB_10	OCDS L2 Debug Line B10
		I		CCPOS1_2	CCU61 Hall input signal 2
		O		TVALID1	MLI1 transmit channel valid output
		O		SLSO1_6	SSC1 Slave Select output 6

Features:

The FPI Bus is designed with the requirements of high-performance systems in mind. The features are:

- Core independent
- Multimaster capability (up to 16 masters)
- Demultiplexed operation
- Clock synchronous
- Peak transfer rate of up to 800 Mbytes/sec (@ 100 MHz bus clock)
- Address and data bus scalable (address bus up to 32 bits, data bus up to 64 bits)
- 8-/16-/32- and 64-bit data transfers
- Broad range of transfer types from single to multiple data transfers
- Split transaction support for agents with long response time
- Burst transfer capability
- EMI and power consumption minimized

3.4.3 LFI

The LMB-to-FPI Interface (LFI) block provides the circuitry to interface (bridge) the FPI bus and the Local Memory Bus (LMB).

LFI Features:

- Full support for bus transactions found within current TriCore™ 1.3 based systems:
  - Single 8/16/32-bit Write/Read transfers from FPI to LMB
  - Single 8/16/32/64-bit Write/Read transfers from LMB to FPI
  - Read-Modify-Write transfers of 8/16/32-bit in both directions
  - Burst transactions of 2, 4 or 8 data beats from the FPI to the LMB
  - Burst transactions of 2 or 4 data beats from the LMB to the FPI
- Address decoding and translation as required by TriCore™ 1.3 implementation
- FPI master interface supports full pipelining on FPI bus
- LMB master interface supports pipelining on LMB within the scope of the LMB specification
- FPI master interface can act as default master on FPI bus
- Programmable support for split LMB to FPI read transactions
- Retry generation on both FPI and LMB buses
- Full support for abort, retry, error and FPI timeout conditions
- Flexible LMB/FPI clock ratio support including dynamic clock switching support
- LFI core clock may be shut down when no transactions are being issued to LFI from either bus and the LFI has no transactions in progress, thus saving power.

3.5 LMB External Bus Unit

The LMB External Bus Control Unit (EBU) of the TC1130 is the interface between external resources, like memories and peripheral units, and the internal resources connected to on-chip buses if enabled. The basic structure and external interconnections of the EBU are shown in **Figure 3-1**.

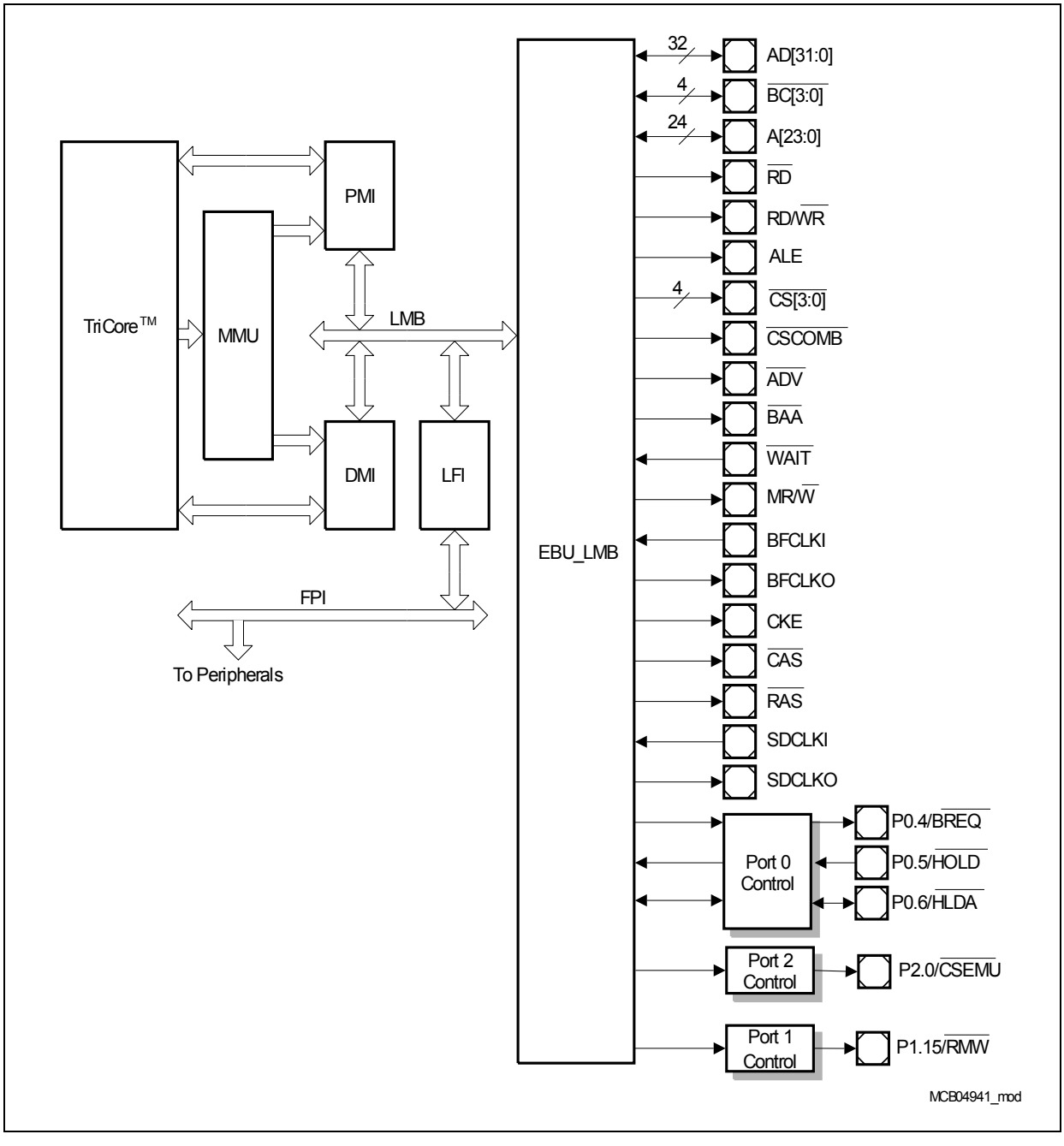


Figure 3-1 EBU Structure and Interface

3.7 Interrupt System

An interrupt request can be serviced by the CPU, which is called “Service Provider”. Interrupt requests are referred to as “Service Requests” in this document.

Each peripheral in the TC1130 can generate service requests. Additionally, the Bus Control Unit, the Debug Unit, the DMA Controller and even the CPU itself can generate service requests to the Service Provider. As shown in **Figure 3-3**, each unit that can generate service requests is connected to one or multiple Service Request Nodes (SRN). Each SRN contains a Service Request Control Register mod_SRC, where “mod” is the identifier of the unit requesting service. The SRNs are connected to the Interrupt Control Unit (ICU) via the CPU Interrupt Arbitration Bus. The ICU arbitrates service requests for the CPU and administers the Interrupt Arbitration Bus.

Units that can generate service requests are:

- Asynchronous/Synchronous Serial Interfaces (ASC0, ASC1 and ASC2) with 4 SRNs each
- High-Speed Synchronous Serial Interfaces (SSC0 and SSC1) with 3 SRNs each
- Inter IC Interface (IIC) with 3 SRNs
- Universal Serial Bus (USB) with 8 SRNs
- Micro Link Interface MLI0 with 4 SRNs and MLI1 with 2 SRNs
- General Purpose Timer Unit (GPTU) with 8 SRNs
- Capture/Compare Unit (CCU60 and CCU61) with 4 SRNs each
- MultiCAN (CAN) with 16 SRNs
- Ethernet Controller with 9 SRNs
- External Interrupts with 4 SRNs
- Direct Memory Access Controller (DMA) with 4 SRNs
- DMA Bus with 1 SRN
- System Timer (STM) with 2 SRNs
- Bus Control Units (SBCU and LBCU) with 1 SRN each
- Central Processing Unit (CPU) with 4 SRNs
- Floating Point Unit (FPU) with 1 SRN
- Debug Unit (OCDS) with 1 SRN

The CPU can make service requests directly to itself (via the ICU). The CPU Service Request Nodes are activated through software.

3.8 Parallel Ports

The TC1130 has 72 digital input/output port lines, which are organized into four parallel 16-bit ports and one parallel 8-bit port, Port P0 to Port P4 with 3.3 V nominal voltage.

The digital parallel ports can be used as general purpose I/O lines or they can perform input/output functions for the on-chip peripheral units. An overview on the port-to-peripheral unit assignment is shown in **Figure 3-4**.

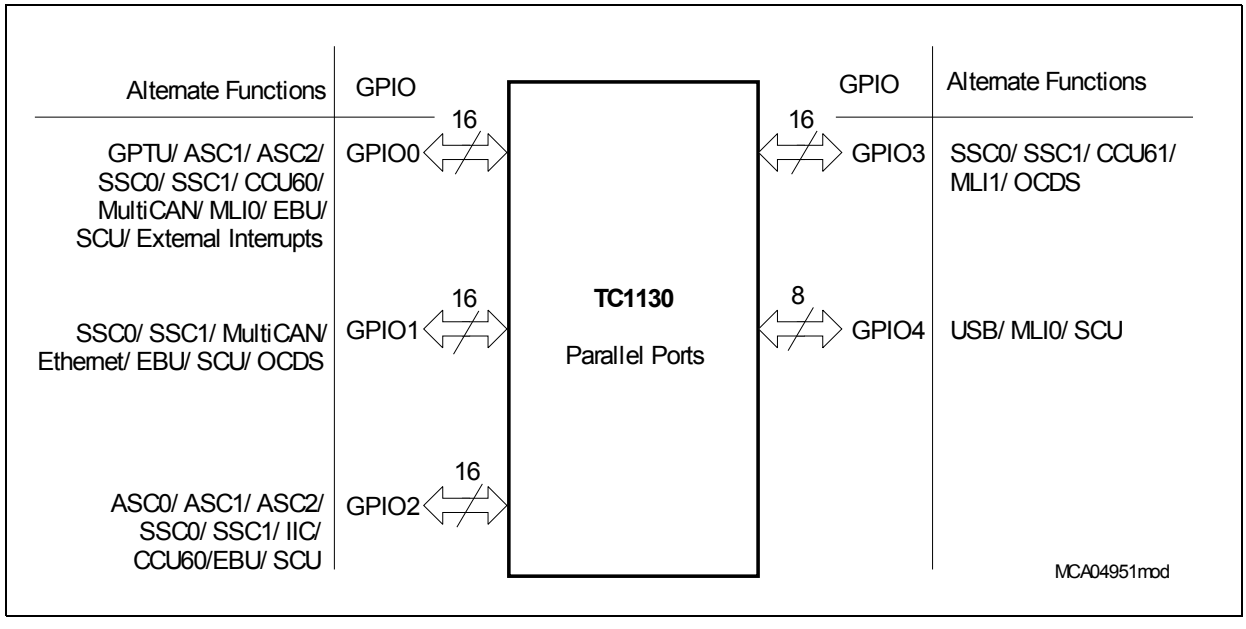


Figure 3-4 Parallel Ports of the TC1130

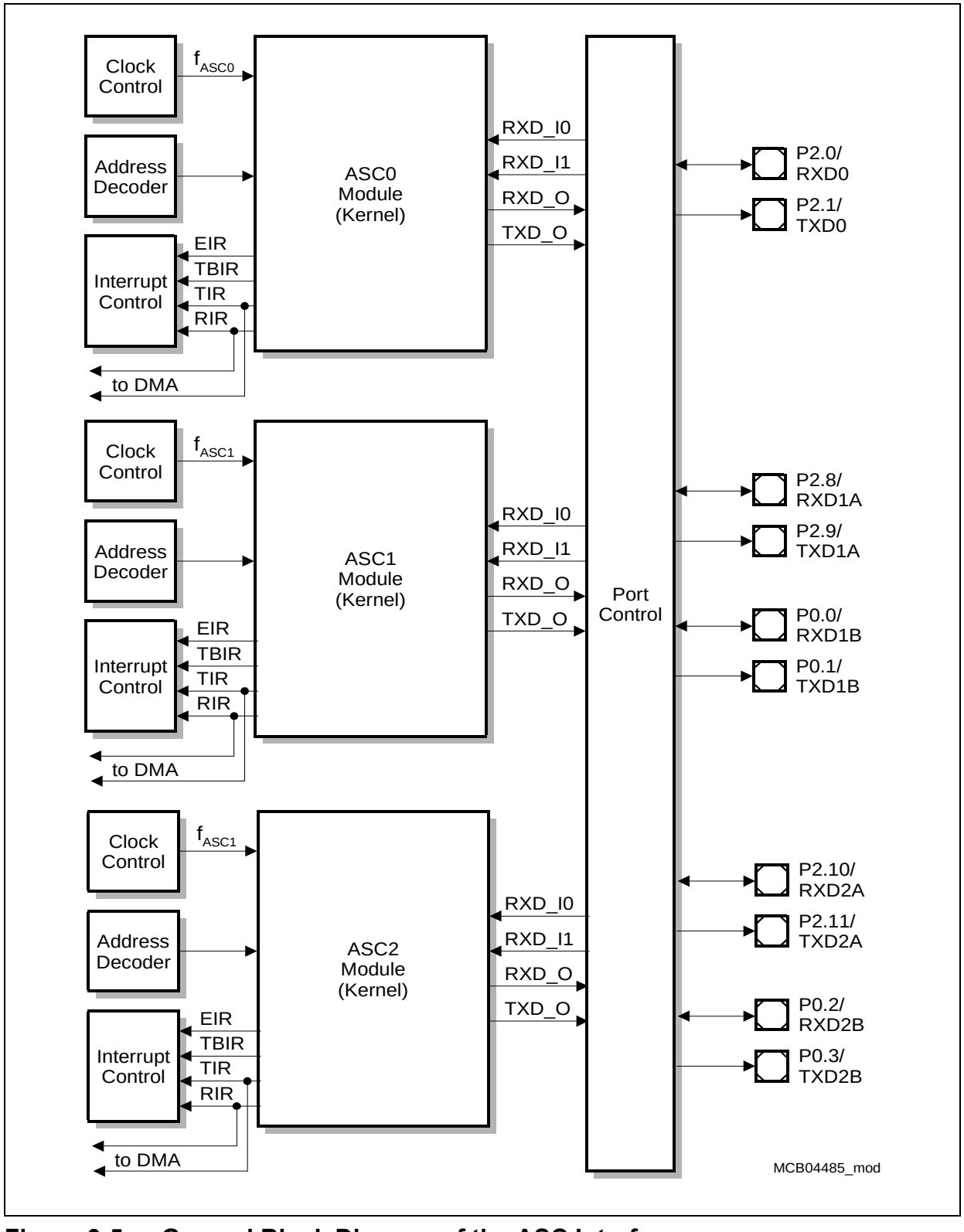


Figure 3-5 General Block Diagram of the ASC Interfaces

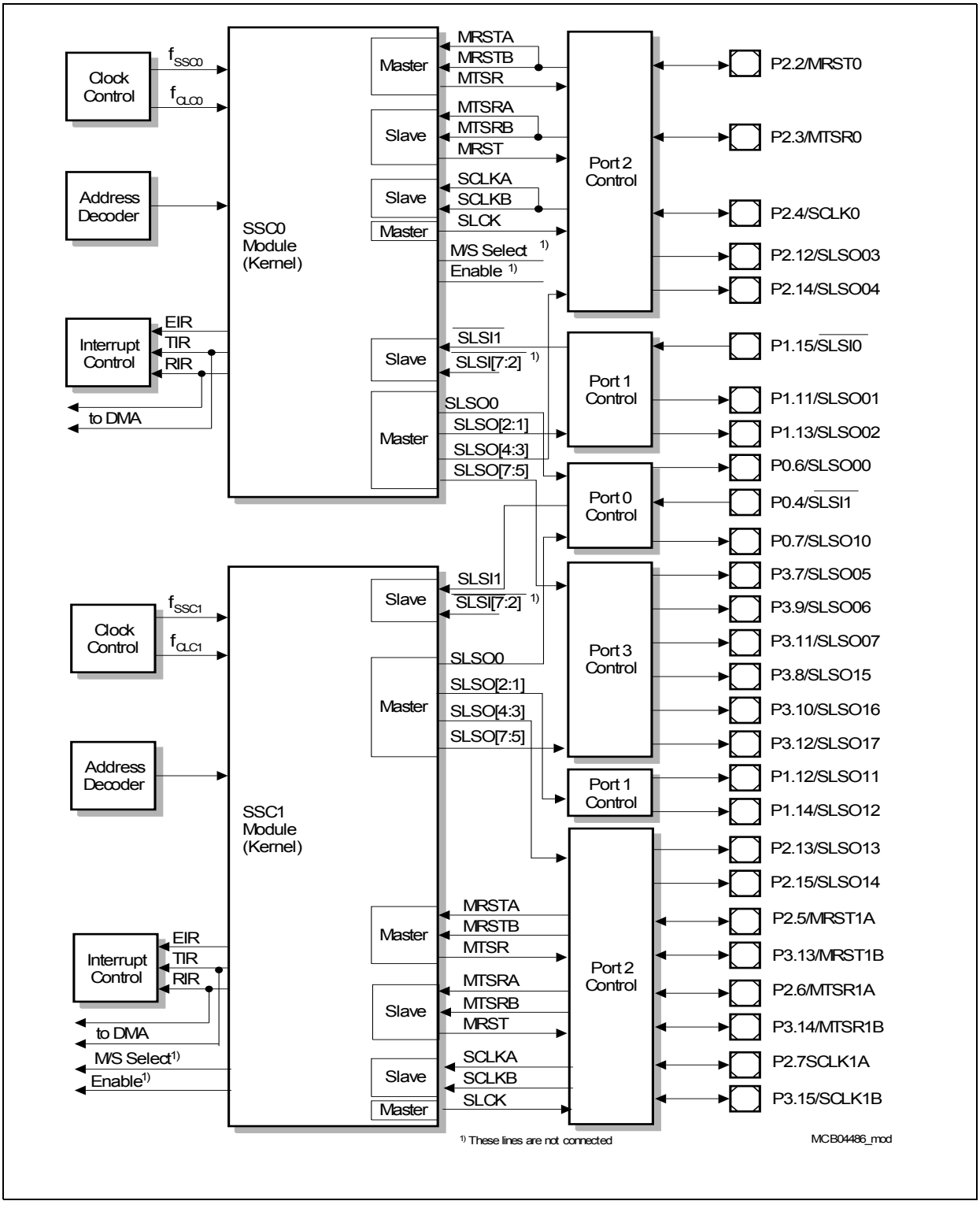


Figure 3-6 General Block Diagram of the SSC Interfaces

The bit timings for the CAN nodes are derived from the peripheral clock (f_{CAN}) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

Features:

- Compliant to ISO 11898
- CAN functionality according to CAN specification V2.0 B (active)
- Dedicated control registers are provided for each CAN node
- A data transfer rate up to 1 MBaud is supported
- Flexible and powerful message transfer control and error handling capabilities are implemented
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter
- Full-CAN functionality: A set of 128 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between two different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed at any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.

The Micro Link Serial Bus Interface is dedicated to the serial communication between the other Infineon 32-bit controllers with MLI. The communication is intended to be fast due to an address translation system, and it is not necessary to have any special program in the second controller.

Features:

- Serial communication from the MLI transmitter to MLI receiver of another controller
- Module supports connection of each MLI with up to four MLI from other controllers
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target controller available
- Special protocol to transfer data, address offset, or address offset and data
- Error control using a parity bit
- 32-bit, 16-bit, and 8-bit data transfers
- Address offset width: from 1- to 16-bit
- Baud rate: f_{MLI} / 2 (symmetric shift clock approach),
  baud rate definition by the corresponding fractional divider

RB and TB provide on-chip data buffering whereas DMUR and DMUT perform data transfer from/to the shared memory.

Two interfaces are provided by the Ethernet Controller module:

- MII interface for connection of Ethernet PHYs via 18 Input/Output lines
- Master/slave FPI bus interface for connection to the on-chip system bus for data transfer as well as configuration

Features:

- Media Independent Interface (MII) according to IEEE 802.3
- Supports 10 or 100 Mbit/sec MII-based Physical devices
- Supports Full Duplex Ethernet
- Supports data transfer between Ethernet Controller and COM-DRAM
- Supports data transfer between Ethernet Controller and SDRAM via EBU
- 256 x 32 bit Receive buffer and Transmit buffer each
- Supports burst transfers up to 8 x 32 Bytes

Media Access Controller (MAC)

- 100/10 Mbit/sec operations
- Full IEEE 802.3 compliance
- Station management signaling
- Large on-chip CAM (Content Addressable Memory)
- Full duplex mode
- 80-byte transmit FIFO
- 16-byte receive FIFO
- PAUSE Operation
- Flexible MAC Control Support
- Supports Long Packet mode and Short Packet mode
- PAD generation

Media Independent Interface (MII)

- Media independence
- Multi-vendor point of interoperability
- Supports connection of MAC layer and Physical (PHY) layer devices
- Capable of supporting both 100 Mbit/sec and 10 Mbit/sec data rates
- Data and delimiters are synchronous to clock references
- Provides independent four bits wide transmit and receive data paths
- Supports connection of PHY layer and Station Management (STA) devices
- Provides a simple management interface
- Capable of driving a limited length of shielded cable

Table 3-5 Load Capacitors Select (cont'd)

Fundamental Mode Crystal Frequency (approx., MHz)	Load Capacitors C1, C2 (pF)
20	10
24	10

A block capacitor between V_{DDOSC3} and V_{SSOSC}, V_{DDOSC} and V_{SSOSC} is recommended, too.

4.2 DC Parameters

4.2.1 Input/Output Characteristics

V_{SS} = 0 V; T_A = -40 °C to +125 °C

Parameter	Symbol		Limit Values		Unit	Test Condition
			min.	max.		
GPIO pins, Dedicated pins and EBU pins						
Input low voltage	V_{IL}	SR	-0.3	0.8	V	LvTTL
Input high voltage	V_{IH}	SR	2.0	V_{DDP} + 0.3	V	LvTTL
Output low voltage	V_{OL}	CC	–	0.4	V	I_{OL} = 2mA
Output high voltage	V_{OH}	CC	2.4	–	V	I_{OH} = -2mA
Pull-up current [1]	$\|I_{PUA}\|$	CC			µA	V_{IN} = 0V
	$\|I_{PUC}\|$	CC			µA	V_{IN} = 0V
Pull-down current [2]	$\|I_{PDA}\|$	CC	–	156	µA	V_{IN} = V_{DDP}
	$\|I_{PDC}\|$	CC	–	15.7	µA	V_{IN} = V_{DDP}
Input leakage current [3]	I_{OZ1}	CC	–	±350	nA	0 < V_{IN} < V_{DDP}
Pin Capacitance [4]	C_{IO}	CC	–	10	pF	f = 1 MHz T_A = 25 °C

1) The current is applicable to the pins, for which a pull-up has been specified. Refer to **Table 2-1**. I_{PUx} refers to the pull-up current for type x in absolute values.

2) The current is applicable to the pins, for which a pull-down has been specified. Refer to **Table 2-1**. I_{PDx} refers to the pull-down current for type x in absolute values.

3) Excluded following pins: $\overline{\text{NMI}}$, $\overline{\text{TRST}}$, TCK, TDI, TMS, MII_TXCLK, MII_RXCLK, MII_MDIO, ALE, P2.1,HWCFG0, HWCFG1, HWCFG2, BRKIN, PORST, HDRST.

4) Not subject to production test, verified by design/characterization.