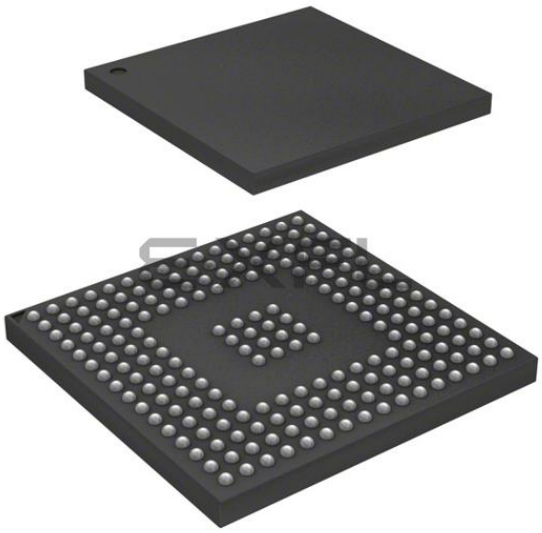
Infineon Technologies - TC1130L150EBGBBFXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IrDA, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	72
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	144K x 8
Voltage - Supply (Vcc/Vdd)	1.43V ~ 1.58V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LBGA
Supplier Device Package	P-LBGA-208-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1130l150ebgbbfxuma1

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2 General Device Information

2.1 Block Diagram

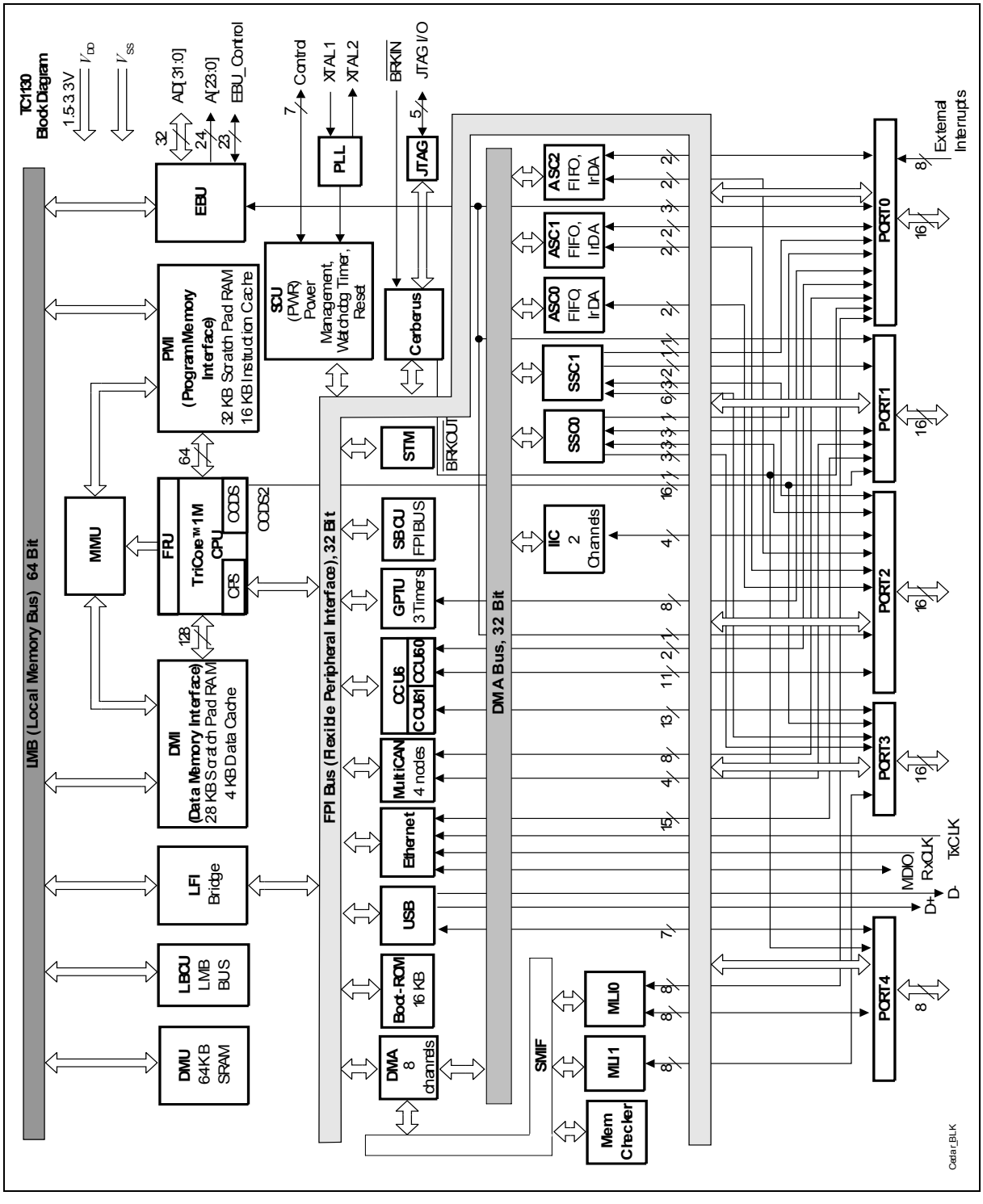

Figure 2-1 TC1130 Block Diagram

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
P1		I/O		**Port 1** Port 1 serves as 16-bit bi-directional general purpose I/O port which can be used for input/output for Ethernet controller, MultiCAN, CAN, OCDS L2, SSC0/1, EBU and SCU.
P1.0	D11	O	PUC	MII_TXD0 Ethernet controller transmit data output line 0
		I		RXDCAN0_B CAN node 0 receiver input B
		I		SWCFG0 Software configuration 0
		O		OCDSA_0 OCDS L2 Debug Line A0
P1.1	C12	O	PUC	MII_TXD1 Ethernet controller transmit data output line 1
		I		SWCFG1 Software configuration 1
		O		TXDCAN0_B CAN node 0 transmitter output B
		O		OCDSA_1 OCDS L2 Debug Line A1
P1.2	D12	O	PUC	MII_TXD2 Ethernet controller transmit data output line 2
		I		RXDCAN1_B CAN node 1 receiver input B
		I		SWCFG2 Software configuration 2
		O		OCDSA_2 OCDS L2 Debug Line A2
P1.3	B12	O	PUC	MII_TXD3 Ethernet controller transmit data output line 3
		O		TXDCAN1_B CAN node 1 transmitter output B
		I		SWCFG3 Software configuration 3
		O		OCDSA_3 OCDS L2 Debug Line A3
P1.4	C11	O	PUC	MII_TXER Ethernet controller transmit error output line
		I		SWCFG4 Software configuration 4
		O		OCDSA_4 OCDS L2 Debug Line A4
P1.5	C13	O	PUC	MII_TXEN Ethernet controller transmit enable output line
		I		SWCFG5 Software configuration 5
		O		OCDSA_5 OCDS L2 Debug Line A5
P1.6	A12	O	PUC	MII_MDC Ethernet controller management data clock output line
		I		SWCFG6 Software configuration 6
		O		OCDSA_6 OCDS L2 Debug Line A6

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions	
P3.11	C16	O	PUC	OCDSB_11	OCDS L2 Debug Line B11
		O		TDATA1	MLI1 transmit channel data output
		O		SLSO0_7	SSC0 Slave Select output 7
		I		CC61_T12HR	CCU61 Timer 12 hardware run
P3.12	D16	O	PUC	OCDSB_12	OCDS L2 Debug Line B12
		I		RCLK1	MLI1 receive channel clock input
		O		SLSO1_7	SSC1 Slave Select output 7
		I		CC61_T13HR	CCU61 Timer 13 hardware run
P3.13	K13	O	PUC	OCDSB_13	OCDS L2 Debug Line B13
		O		RREADY1	MLI1 receive channel ready output
		I/O		MRST1B	SSC1 master receive/slave transmit input/output B
P3.14	J14	O	PUC	OCDSB_14	OCDS L2 Debug Line B14
		I		RVALID1	MLI1 receive channel valid input
		I/O		MTSR1B	SSC1 master transmit/slave receive input/output B
P3.15	J15	O	PUC	OCDSB_15	OCDS L2 Debug Line B15
		I		RDATA1	MLI1 receive channel data input
		I/O		SCLK1B	SSC1 clock input/output line B

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
D-	T15	I/O	—	**USB D- Data Line**
$\overline{\text{CS0}}$ **$\overline{\text{CS1}}$** **$\overline{\text{CS2}}$** **$\overline{\text{CS3}}$**	D9 D8 C9 B8	O O O O	PUC PUC PUC PUC	**EBU Chip Select Output Line 0** **EBU Chip Select Output Line 1** **EBU Chip Select Output Line 2** **EBU Chip Select Output Line 3** Each corresponds to a programmable region. Only one can be active at one time.
$\overline{\text{CSCOMB}}$	N3	O	PUC	**EBU Chip Select Output for combination function (Overlay Memory and Global)**
SDCLKI	J1	I	—	**SDRAM Clock Input (Clock Feedback)**
SDCLKO	H1	O	—	**SDRAM Clock Output** Accesses to SDRAM devices are synchronized to this clock.
$\overline{\text{RAS}}$	D6	O	PUC	**EBU SDRAM Row Address Strobe Output**
$\overline{\text{CAS}}$	D5	O	PUC	**EBU SDRAM Column Address Strobe Output**
CKE	L4	O	PUC	**EBU SDRAM Clock Enable Output**
BFCLKI	D1	I	—	**Burst Flash Clock Input (Clock Feedback)**
BFCLKO	E1	O	—	**Burst Flash Clock Output** Accesses to Burst Flash devices are synchronized to this clock.
$\overline{\text{RD}}$	P2	O	PUC	**EBU Read Control Line** Output in master mode Input in slave mode
RD/$\overline{\text{WR}}$	T3	O	PUC	**EBU Write Control Line** Output in master mode Input in slave mode
$\overline{\text{WAIT}}$	B9	I	PUC	**EBU Wait Control Line**
ALE	R3	O	PDC	**EBU Address Latch Enable Output**
MR/$\overline{\text{W}}$	P3	O	PUC	**EBU Motorola-style Read/Write Output**
$\overline{\text{BAA}}$	A11	O	PUC	**EBU Burst Address Advance Output** For advancing address in a Burst Flash access
$\overline{\text{ADV}}$	B11	O	PUC	**EBU Burst Flash Address Valid Output**

Table 2-1 Pin Definitions and Functions (cont'd)

Symbol	Pin	In Out	PU/ PD[1)]	Functions
				EBU Address Bus Input/Output Lines
A0	K1	O	PUC	EBU Address Bus Line 0
A1	L1	O	PUC	EBU Address Bus Line 1
A2	M1	O	PUC	EBU Address Bus Line 2
A3	N1	O	PUC	EBU Address Bus Line 3
A4	P1	O	PUC	EBU Address Bus Line 4
A5	J2	O	PUC	EBU Address Bus Line 5
A6	K2	O	PUC	EBU Address Bus Line 6
A7	L2	O	PUC	EBU Address Bus Line 7
A8	M2	O	PUC	EBU Address Bus Line 8
A9	N2	O	PUC	EBU Address Bus Line 9
A10	J3	O	PUC	EBU Address Bus Line 10
A11	K3	O	PUC	EBU Address Bus Line 11
A12	L3	O	PUC	EBU Address Bus Line 12
A13	M3	O	PUC	EBU Address Bus Line 13
A14	K4	O	PUC	EBU Address Bus Line 14
A15	A8	O	PUC	EBU Address Bus Line 15
A16	A9	O	PUC	EBU Address Bus Line 16
A17	A10	O	PUC	EBU Address Bus Line 17
A18	B10	O	PUC	EBU Address Bus Line 18
A19	C10	O	PUC	EBU Address Bus Line 19
A20	D10	O	PUC	EBU Address Bus Line 20
A21	T4	O	PUC	EBU Address Bus Line 21
A22	R4	O	PUC	EBU Address Bus Line 22
A23	P4	O	PUC	EBU Address Bus Line 23
XTAL1	M16	I	—	**Oscillator/PLL/Clock Generator Input/Output Pins**
XTAL2	N16	O	—	XTAL1 is the input to the main oscillator amplifier and input to the internal clock generator. XTAL2 is the output of the main oscillator amplifier circuit. For clocking of the device from an external source, XTAL1 is driven with the clock signal while XTAL2 is left unconnected. For crystal oscillator operation, XTAL1 and XTAL2 are connected to the crystal with the appropriate recommended oscillator circuitry.
V_{DDOSC3}	P16	—	—	**Main Oscillator Power Supply (3.3 V)**
V_{SSOSC3}	R16	—	—	**Main Oscillator Ground**
V_{DDOSC}	L16	—	—	**Main Oscillator Power Supply (1.5 V)**

3 Functional Description

3.1 On-Chip Memories

The TC1130 provides the following on-chip memories:

- Program Memory Interface (PMI) with
  - 32-Kbyte Scratch-pad Code RAM (SPRAM)
  - 16-Kbyte Instruction Cache Memory (ICACHE)
- Data Memory Interface (DMI) with
  - 28-Kbyte Scratch-pad Data RAM (SPRAM)
  - 4-Kbyte Data Cache Memory (DCACHE)
- Data Memory Unit (DMU) with
  - 64-Kbyte SRAM
- 16-Kbyte Boot ROM (BROM)

Table 3-1 TC1130 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
13	D000 0000$_H$ – D000 6FFF$_H$	28 KB	DMI Local Data RAM (LDRAM)	DMI local	via LMB	non-cached
	D000 7000$_H$ – D3FF FFFF$_H$	~ 64 MB	Reserved			
	D400 0000$_H$ – D400 7FFF$_H$	32 KB	PMI Local Code Scratch Pad RAM (SPRAM)	via LMB	PMI local	
	D400 8000$_H$ – D7FF FFFF$_H$	~64 MB	Reserved			
	D800 0000$_H$ – DDFF FFFF$_H$	96 MB	External Memory Space	via LMB	via LMB	
	DE00 0000$_H$ – DEFF FFFF$_H$	16 MB	Emulator Memory Space			
	DF00 0000$_H$ – DFFF BFFF$_H$	~16 MB	Reserved	–	–	
	DFFF C000$_H$ – DFFF FFFF$_H$	16 KB	Boot ROM Space	via FPI	via FPI	
14	E000 0000$_H$ – E7FF FFFF$_H$	128 MB	External Memory Space	via LMB	via LMB	
	E800 0000$_H$ – E83F FFFF$_H$	4 MB	Reserved for mapped space for lower 4 Mbytes of Local Memory in Segment 12 (Transformed by LFI bridge to C000 0000$_H$ – C03F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E840 0000$_H$ – E84F FFFF$_H$	1 MB	Reserved for mapped space for lower 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D000 0000$_H$ – D00F FFFF$_H$)	access only from FPI bus side of LFI	access only from FPI bus side of LFI	
	E850 0000$_H$ – E85F FFFF$_H$	1 MB	Reserved for mapped space for 1 Mbyte of Local Memory in Segment 13 (Transformed by LFI bridge to D400 0000$_H$ – D40F FFFF$_H$)			

Table 3-1 TC1130 Block Address Map (cont'd)

Seg-ment	Address Range	Size	Description	DMI Acc.	PMI Acc.	
14	E860 0000$_H$ – EFFF FFFF$_H$	122 MB	Reserved	–	–	non-cached
15	F000 0000$_H$ – FFFF FFFF$_H$	256 MB	See **Table 3-2**	via LMB or via FPI	via LMB or via FPI	

Table 3-2 Block Address Map of Segment 15

Symbol	Description	Address Range	Size
System Peripheral Bus (SPB)			
SCU	System Control Unit (incl. WDT)	F000 0000$_H$ - F000 00FF$_H$	256 Bytes
SBCU	FPI Bus Control Unit	F000 0100$_H$ - F000 01FF$_H$	256 Bytes
STM	System Timer	F000 0200$_H$ - F000 02FF$_H$	256 Bytes
OCDS	On-Chip Debug Support (Cerberus)	F000 0300$_H$ - F000 03FF$_H$	256 Bytes
–	Reserved	F000 0400$_H$ - F000 04FF$_H$	256 Bytes
–	Reserved	F000 0500$_H$ - F000 05FF$_H$	256 Bytes
GPTU	General Purpose Timer Unit	F000 0600$_H$ - F000 06FF$_H$	256 Bytes
–	Reserved	F000 0700$_H$ - F000 07FF$_H$	256 Bytes
–	Reserved	F000 0800$_H$ - F000 08FF$_H$	256 Bytes
–	Reserved	F000 0900$_H$ - F000 09FF$_H$	256 Bytes
–	Reserved	F000 0A00$_H$ - F000 0AFF$_H$	256 Bytes
–	Reserved	F000 0B00$_H$ - F000 0BFF$_H$	256 Bytes
P0	Port 0	F000 0C00$_H$ - F000 0CFF$_H$	256 Bytes
P1	Port 1	F000 0D00$_H$ - F000 0DFF$_H$	256 Bytes
P2	Port 2	F000 0E00$_H$ - F000 0EFF$_H$	256 Bytes
P3	Port 3	F000 0F00$_H$ - F000 0FFF$_H$	256 Bytes
P4	Port 4	F000 1000$_H$ - F000 10FF$_H$	256 Bytes
–	Reserved	F000 1100$_H$ - F000 11FF$_H$	256 Bytes

Table 3-2 Block Address Map of Segment 15 (cont'd)

Symbol	Description	Address Range	Size
MLI1_ LP3	MLI1 Large Transfer Window 3	F027 0000$_H$ - F027 FFFF$_H$	64 Kbytes
–	Reserved	F028 0000$_H$ - F200 00FF$_H$	–
ECU	Ethernet Controller Unit	F200 0100$_H$ - F200 05FF$_H$	1280Bytes
–	Reserved	F200 0600$_H$ - F7E0 FEFF$_H$	–
CPU (Part of System Peripheral Bus)			
CPU SFRs	CPU Slave Interface	F7E0 FF00$_H$ - F7E0 FFFF$_H$	256 Bytes
	Reserved	F7E1 0000$_H$ - F7E1 7FFF$_H$	–
	MMU	F7E1 8000$_H$ - F7E1 80FF$_H$	256 Bytes
	Reserved	F7E1 8100$_H$ - F7E1 BFFF$_H$	–
	Memory Protection Registers	F7E1 C000$_H$ -F7E1 EFFF$_H$	12 Kbytes
	Reserved	F7E1 F000$_H$ - F7E1 FCFF$_H$	–
	Core Debug Register (OCDS)	F7E1 FD00$_H$ -F7E1 FDFF$_H$	256 Bytes
	Core Special Function Registers (CSFRs)	F7E1 FE00$_H$ -F7E1 FEFF$_H$	256 Bytes
	General Purpose Register (GPRs)	F7E1 FF00$_H$ - F7E1 FFFF$_H$	256 Bytes
–	Reserved	F7E2 0000$_H$ - F7FF FFFF$_H$	–
Local Memory Buses (LMB)			
EBU	External Bus Interface Unit	F800 0000$_H$ - F800 03FF$_H$	1 Kbyte
DMU	Data Memory Unit	F800 0400$_H$ - F800 04FF$_H$	256 Bytes
–	Reserved	F800 0500$_H$ - F87F FBFF$_H$	–
DMI	Data Memory Interface Unit	F87F FC00$_H$ - F87F FCFF$_H$	256 Bytes
PMI	Program Memory Interface Unit	F87F FD00$_H$ - F87F FDFF$_H$	256 Bytes
LBCU	Local Memory Bus Control Unit	F87F FE00$_H$ - F87F FEFF$_H$	256 Bytes
LFI	LMB to FPI Bus Bridge	F87F FF00$_H$ - F87F FFFF$_H$	256 Bytes
–	Reserved	F880 0000$_H$ - FFFF FFFF$_H$	–

3.3 Memory Protection System

The TC1130 memory protection system specifies the addressable range and read/write permissions of memory segments available to the currently executing task. The memory protection system controls the position and range of addressable segments in memory. It also controls the types of read and write operations allowed within addressable memory segments. Any illegal memory access is detected by the memory protection hardware, which then invokes the appropriate Trap Service Routine (TSR) to handle the error. Thus, the memory protection system protects critical system functions against both software and hardware errors. The memory protection hardware can also generate signals to the Debug Unit to facilitate tracing illegal memory accesses.

In TC1130, TriCore™ supports two address spaces: the virtual address space and the physical address space. Both address spaces are 4 Gbytes in size and are divided into 16 segments with each segment being 256 Mbytes. The upper 4 bits of the 32-bit address are used to identify the segment. Virtual segments are numbered 0 - 15. But a virtual address is always translated into a physical address before accessing memory. The virtual address is translated into a physical address using one of two translation mechanisms: (a) direct translation, and (b) Page Table Entry (PTE) based translation. If the virtual address belongs to the upper half of the virtual address space then the virtual address is directly used as the physical address (direct translation). If the virtual address belongs to the lower half of the address space, then the virtual address is used directly as the physical address if the processor is operating in physical mode (direct translation) or translated using a Page Table Entry if the processor is operating in Virtual mode (PTE translation). These are managed by Memory Management Unit (MMU).

Memory protection is enforced using separate mechanisms for the two translation paths.

3.3.1 Protection for Direct translation

Memory protection for addresses that undergo direct translation is enforced using the range based protection that has been used in the previous generation of the TriCore™ architecture. The range based protection mechanism provides support for protecting memory ranges from unauthorized read, write, or instruction fetch accesses. The TriCore™ architecture provides up to four protection register sets with the PSW.PRS field controlling the selection of the protection register set. Because the TC1130 uses a Harvard-style memory architecture, each Memory Protection Register Set is broken down into a Data Protection Register Set and a Code Protection Register Set. Each Data Protection Register Set can specify up to four address ranges to receive particular protection modes. Each Code Protection Register Set can specify up to two address ranges to receive particular protection modes.

Each of the Data Protection Register Sets and Code Protection Register Sets determines the range and protection modes for a separate memory area. Each contains register pairs which determine the address range (the Data Segment Protection Registers and Code Segment Protection Registers) and one register (Data Protection

The EBU is used primarily for any Local Memory Bus (LMB) master accessing external memories. The EBU controls all transactions required for this operation and in particular handles the arbitration between the internal EBU master and the external EBU master.

The types of external devices/bus modes controlled by the EBU are:

- Intel-style peripherals (separate $\overline{RD}$ and $\overline{WR}$ signals)
- ROMs, EPROMs
- Static RAMs
- PC100 and PC133 SDRAMs (Burst Read/Write Capacity/Multi-Bank/Page support)
- Specific types of Burst Mode Flash devices
- Special support for external emulator/debug hardware

Features:

- Supports 64-bit Local Memory Bus (LMB)
- Supports external bus frequency: internal LMB frequency = 1:1 or 1:2
- Provides highly programmable access parameters
- Supports Intel-style peripherals/devices
- Supports PC100 and PC133 (runs in maximum 120 MHz) SDRAM (burst access, multibanking, precharge, refresh)
- Supports 16- and 32-bit SDRAM data bus and 64-,128-, and 256-Mbit devices
- Supports Burst Flash devices
- Supports Multiplexed access (address and data on the same bus) when PC100 and PC133 SDRAM are not presented on the external bus
- Supports data buffering: Code Prefetch Buffer, Read/Write Buffer
- External master arbitration compatible to C166 and other TriCore™ devices
- Provides 4 programmable address regions (1 dedicated for emulator)
- Provides a CSGLB signal, bit programmable to combine one or more $\overline{CS}$ lines for buffer control
- Provides $\overline{RMW}$ signal reflecting read-modify-write action
- Supports Little Endian byte ordering
- Provides signal for controlling data flow of slow-memory buffer

Features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity bit generation/checking
  - One or two stop bits
  - Baud rate from 4.6875 MBaud to 1.1 Baud (@ 75 MHz clock)
- Multiprocessor mode for automatic address/data byte detection
- Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 9.375 MBaud to 762.9 Baud (@ 75 MHz clock)
- Support for IrDA data transmission up to 115.2 kBaud maximum
- Double buffered transmitter/receiver
- Interrupt generation
  - On a transmitter buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receiver buffer full condition
  - On an error condition (frame, parity, overrun error)
- FIFO
  - 8-byte receive FIFO (RXFIFO)
  - 8-byte transmit FIFO (TXFIFO)
  - Independent control of RXFIFO and TXFIFO
  - 9-bit FIFO data width
  - Programmable Receive/Transmit Interrupt Trigger Level
  - Receive and Transmit FIFO filling level indication
  - Overrun error generation
  - Underflow error generation

3.14 Micro Link Serial Bus Interface (MLI)

Figure 3-10 shows a global view of the functional blocks of two Micro Link Serial Bus interfaces (MLI0 and MLI1).

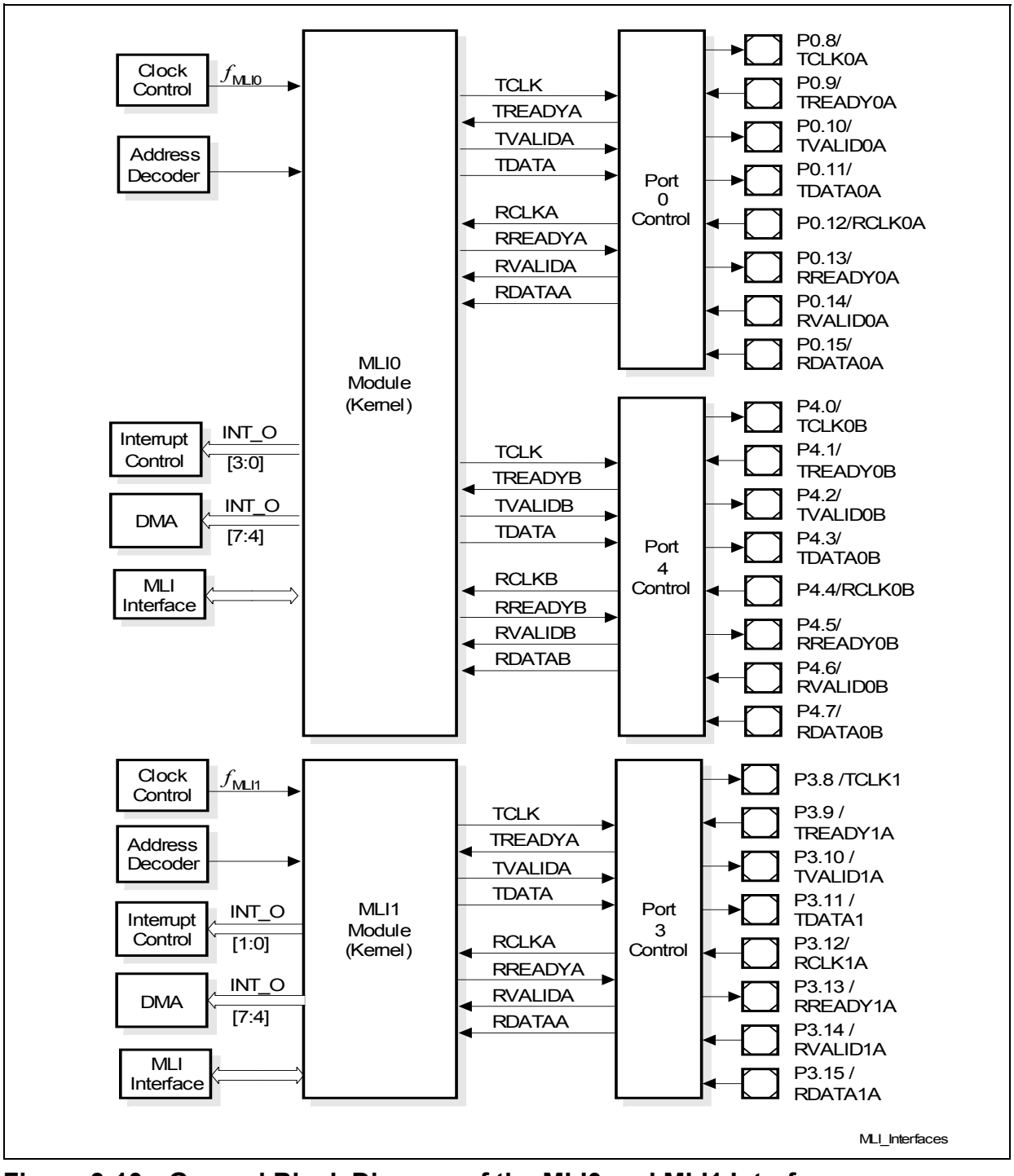

Figure 3-10 General Block Diagram of the MLI0 and MLI1 Interfaces

3.16 Capture/Compare Unit 6 (CCU6)

Figure 3-12 shows a global view of the functional blocks of two Capture/Compare Units (CCU60 and CCU61).

Both of the CCU6 modules are further supplied with clock control, interrupt control, address decoding, and port control logic. One DMA request can be generated by each CCU6 module.

Each CCU6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

Timer 12 Features:

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Features:

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported

Additional Features:

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

3.21 Boot Options

The TC1130 booting schemes provides a number of different boot options for the start of code execution. **Table 3-3** shows the boot options available in the TC1130.

Table 3-3 Boot Selections

$\overline{\text{BRKIN}}$[1]	$\overline{\text{TM}}$[1]	HWCFG [2:0]	Type of Boot	PC Start Value (User Entry)
1	1	000	**Bootstrap Loader** Serial boot from ASC to PMI scratch pad, run loaded program	DFFF FFFC$_H$[2] (D400 0000$_H$)
		001	**Bootstrap Loader** Serial boot from CAN to PMI scratch pad, run loaded program	
		010	**Bootstrap Loader** Serial boot from SSC to PMI scratch pad, run loaded program	
		011	External memory, EBU as master	DFFF FFFC$_H$[2] (A000 0000$_H$)
		100	External memory, EBU as slave	DFFF FFFC$_H$[2] (A000 0000$_H$)
		101	Reserved (STOP)	----
		110	PMI scratch pad	D400 0000$_H$
		111	Reserved (STOP)	DFFF FFFC$_H$[2]
1	0	000-111	Reserved (STOP)	DFFF FFFC$_H$[2]
0	1	000	Tristate chip	----
		001	Go to external emulator space	DFFF FFFC$_H$[2] (DE00 0000$_H$)
		010	Reserved (STOP)	----
		011	OSC and PLL Bypass	----
		100-111	Reserved (STOP)	DFFFFFFC$_H$[2]
0	0	000-111	Reserved (STOP)	DFFFFFFC$_H$[2]

1) This input signal is active low.

2) This is the BootROM entry address; the start address of user program in parentheses.

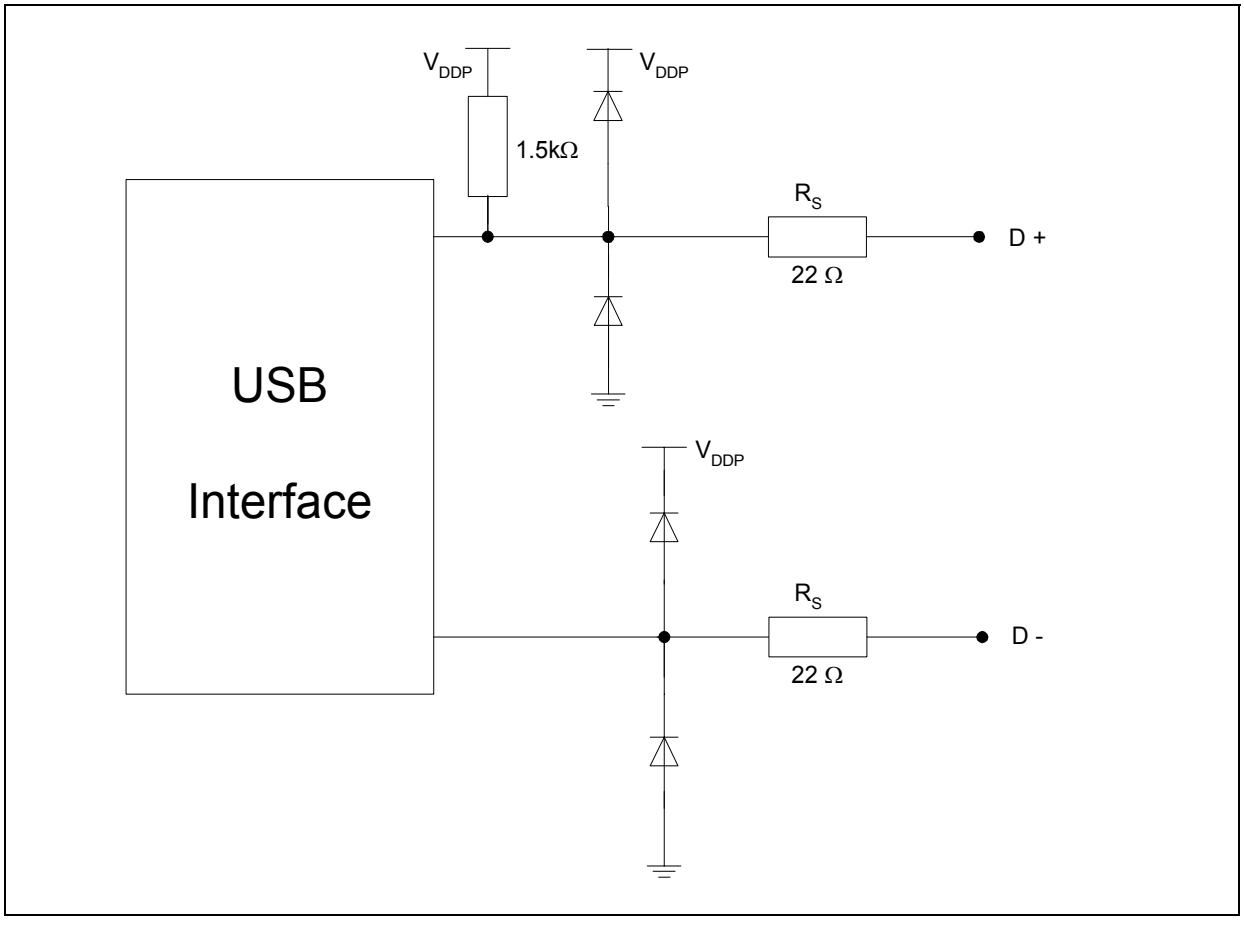

Figure 4-1 USB Interface

4.3.5 Port Timing

(Operating Conditions apply; C_L = 50 pF)

Parameter	Symbol	Limits		Unit
		min	max	
Port data valid from TRCLK [1] up to 120 MHz[2]	t_1 CC	–	13	ns

[1] Port data is output with respect to the FPI clock. The TRCLK is used as a reference here since the FPI clock is not available as an external pin and TRCLK is same frequency as CPU clock. Port lines maintain their states for at least 2 CPU clocks.

[2] 120 MHz is verified by design/characterization.

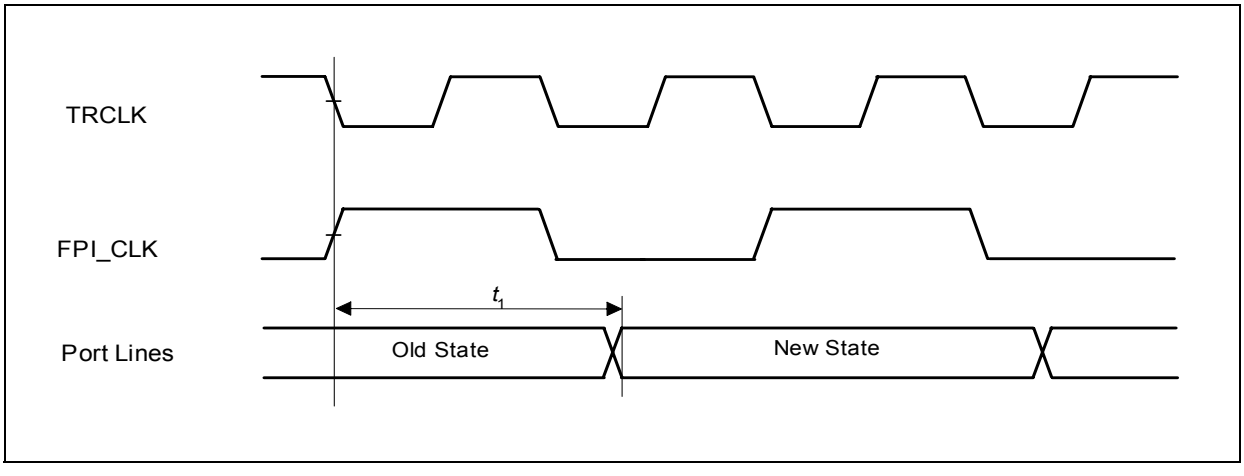

Figure 4-6 Port Timing

4.3.8.6 Timing for Multiplexed Access Signals

(Operating Conditions apply; C_L = 50 pF)[1)]

Parameter	Symbol		Limits		Unit
			min	max	
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output valid time from output clock ↑	t_1	CC	–	9	ns
ALE, $\overline{\text{CSx}}$, RD/$\overline{\text{WR}}$, $\overline{\text{RD}}$, MR/$\overline{\text{W}}$, $\overline{\text{BC(3:0)}}$ output hold time from output clock ↑	t_2	CC	0.0	–	ns
AD(31:0) output valid time from output clock ↑	t_3	CC	–	9	ns
AD(31:0) output hold time from output clock ↑	t_4	CC	0.0	–	ns
AD(31:0) input setup time to output clock ↑	t_5	SR	1.4	–	ns
AD(31:0) input hold time from output clock ↑	t_6	SR	3	–	ns
$\overline{\text{WAIT}}$ input setup time to output clock ↑	t_9	SR	12	–	ns
$\overline{\text{WAIT}}$ input hold time from output clock ↑	t_{10}	SR	3	–	ns
$\overline{\text{RMW}}$ output valid time from output clock ↑	t_{11}	CC	–	8	ns
$\overline{\text{RMW}}$ output hold time from output clock ↑	t_{12}	CC	1.3	–	ns
ALE width	t_{13}	CC	8.5	–	ns
AD(31:0) output hold time from RD/$\overline{\text{WR}}$ ↑	t_{14}	CC	0	–	ns

1) The purpose for characterization of Asynchronous access is to provide the performance of all of the signals to user. User can decide whether an extra cycle is needed or not based on above parameters to generate signals with correct timing sequence. It is user's responsibility to program the correct phase length according to the memory/peripheral device specification and EBU Specification.

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