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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

## Details

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Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg12b500f1024gl125-b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 2. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	DC-DC Con- verter	GPIO	Package	Temp Range
EFM32JG12B500F1024GL125-B	1024	256	Yes	65	BGA125	-40 to +85
EFM32JG12B500F1024IL125-B	1024	256	Yes	65	BGA125	-40 to +125
EFM32JG12B500F1024GM48-B	1024	256	Yes	33	QFN48	-40 to +85
EFM32JG12B500F1024IM48-B	1024	256	Yes	33	QFN48	-40 to +125





Figure 2.1. OPN Decoder

#### 3.6.5 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface LESENSE<sup>TM</sup> is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators, ADC, and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable finite state machine which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

#### 3.7 Security Features

#### 3.7.1 GPCRC (General Purpose Cyclic Redundancy Check)

The GPCRC module implements a Cyclic Redundancy Check (CRC) function. It supports both 32-bit and 16-bit polynomials. The supported 32-bit polynomial is 0x04C11DB7 (IEEE 802.3), while the 16-bit polynomial can be programmed to any value, depending on the needs of the application.

#### 3.7.2 Crypto Accelerator (CRYPTO)

The Crypto Accelerator is a fast and energy-efficient autonomous hardware encryption and decryption accelerator. EFM32JG12 devices support AES encryption and decryption with 128- or 256-bit keys, ECC over both GF(P) and GF(2<sup>m</sup>), and SHA-1 and SHA-2 (SHA-224 and SHA-256).

Supported block cipher modes of operation for AES include: ECB, CTR, CBC, PCBC, CFB, OFB, GCM, CBC-MAC, GMAC and CCM.

Supported ECC NIST recommended curves include P-192, P-224, P-256, K-163, K-233, B-163 and B-233.

The CRYPTO module allows fast processing of GCM (AES), ECC and SHA with little CPU intervention. CRYPTO also provides trigger signals for DMA read and write operations.

#### 3.7.3 True Random Number Generator (TRNG)

The TRNG module is a non-deterministic random number generator based on a full hardware solution. The TRNG is validated with NIST800-22 and AIS-31 test suites as well as being suitable for FIPS 140-2 certification (for the purposes of cryptographic key generation).

#### 3.7.4 Security Management Unit (SMU)

The Security Management Unit (SMU) allows software to set up fine-grained security for peripheral access, which is not possible in the Memory Protection Unit (MPU). Peripherals may be secured by hardware on an individual basis, such that only priveleged accesses to the peripheral's register interface will be allowed. When an access fault occurs, the SMU reports the specific peripheral involved and can optionally generate an interrupt.

#### 3.8 Analog

### 3.8.1 Analog Port (APORT)

The Analog Port (APORT) is an analog interconnect matrix allowing access to many analog modules on a flexible selection of pins. Each APORT bus consists of analog switches connected to a common wire. Since many clients can operate differentially, buses are grouped by X/Y pairs.

#### 3.8.2 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

#### 3.8.3 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to 1 Msps. The output sample resolution is configurable and additional resolution is possible using integrated hardware for averaging over multiple samples. The ADC includes integrated voltage references and an integrated temperature sensor. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

#### 3.8.4 Capacitive Sense (CSEN)

The CSEN module is a dedicated Capacitive Sensing block for implementing touch-sensitive user interface elements such a switches and sliders. The module can be configured to take measurements on a single port pin or scan through multiple pins and store results to memory through DMA. Several channels can also be shorted together to measure the combined capacitance or implement wake-on-touch from very low energy modes. Hardware includes a digital accumulator and an averaging filter, as well as digital threshold comparators to reduce software overhead.

#### 3.8.5 Digital to Analog Current Converter (IDAC)

The Digital to Analog Current Converter can source or sink a configurable constant current. This current can be driven on an output pin or routed to the selected ADC input pin for capacitive sensing. The full-scale current is programmable between 0.05 µA and 64 µA with several ranges consisting of various step sizes.

#### 3.8.6 Digital to Analog Converter (VDAC)

The Digital to Analog Converter (VDAC) can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The opamps are used in conjunction with the VDAC, to provide output buffering. One opamp is used per singleended channel, or two opamps are used to provide differential outputs. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

#### 3.8.7 Operational Amplifiers

The three opamps are low power amplifiers with a high degree of flexibility targeting a wide variety of standard opamp application areas. With flexible built-in programming for gain and interconnection they can be configured to support multiple common opamp functions. All pins are also available externally for filter configurations. Each opamp has a rail to rail input and a rail to rail output. They can be used in conjunction with the VDAC module or in stand-alone configurations. The opamps save energy, PCB space, and cost as compared with standalone opamps because they are integrated on-chip.

#### 3.9 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFM32JG12. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

### 3.10 Core and Memory

#### 3.10.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M3 RISC processor achieving 1.25 Dhrystone MIPS/MHz
- Memory Protection Unit (MPU) supporting up to 8 memory segments
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 1024 kB flash program memory
  - · Dual-bank memory with read-while-write support
- Up to 256 kB RAM data memory
- · Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

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0x400e2000     CLMA       0x400e2000     FPUEH       0x400e1000     FPUEH       0x400e1000     MSC       0x400e1000     MSC       0x400e1000     MSC       0x400e1000     MSC       0x400e1000     MSC       0x400e1200     SMU       0x4001400     CSEN       0x4001400     CSEN       0x4001400     CSEN       0x4001400     CRYPTO0 (bit clear)       0x430e8000     MX48988800       0x4001400     CRYPTO0 (bit.clear)       0x43888800     0x448988800       0x4001400     CRYPTO0 (bit.band)       0x4001400     GPCRC       0x4001400     WTIMER1       0x4001400     WTIMER1       0x4001400     WTIMER1       0x4001400     WTIMER1       0x4001400     USART3       0x4001400     USART3       0x4001400     USART3       0x40000400     USART3       0x40000400     USART3       0x40000400     USART3       0x40000400 <td< td=""><td>0x400e3000</td><td></td><td>\ \</td><td></td><td>0x460†0000</td></td<>	0x400e3000		\ \		0x460†0000
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Ox4001e400 0x4001e000 0x4001e000     CRYOTIMER     Ox4311111       0x4001e000 0x4001d000     TRNG0     6x43e0000 0x43e0000       0x4001e000     GPCRC     6x43e0000       0x4001a000     GPCRC     6x43e0000       0x4001a000     GPCRC     6x43e0000       0x4001a000     GPCRC     6x43e0000       0x4001a000     WTIMER1     6x43e0000       0x4001a000     WTIMER0     6x40e0000       0x4001a000     TIMER1     6x40e0000       0x4001a000     TIMER0     6x40e0000       0x4001a000     WTIMER0     6x40e0000       0x4001a000     USART3     6x40e00000       0x4001a000     USART2     6x20e0000       0x4000000     USART2     6x20e0000       0x4000000     GPIO     6x20e0000       0x4000000     GPIO     6x20e0000       0x4000000     GPIO     6x20e0000       0x4000000     GPIO     6x20e0000       0x40000000     GPIO     6x20e0000       0x40000000     GPIO     6x20e0000       0x40000000     GPIO <td>0x4001f000</td> <td>CSEN</td> <td></td> <td></td> <td>0x44000000</td>	0x4001f000	CSEN			0x44000000
0x4001e000 0x4001400     CRYOTMER     0x434808000       0x4001e000     TRNG0     0x434808000       0x4001400     CRYPT00 (bit-band)     0x438408000       0x40012400     GPCRC     0x434808000       0x40012400     GPCRC     0x438408000       0x40012400     WTIMER1     0x42080000       0x40012400     WTIMER1     0x42080000       0x40012400     WTIMER0     0x4308764800       0x40012800     TIMER1     0x4308764800       0x40012800     TIMER1     0x4308764800       0x40012800     TIMER0     0x4308764800       0x40012800     TIMER0     0x4308764800       0x40012800     TIMER0     0x4388764800       0x40012800     USART1     0x440867677       0x40012800     USART1     0x28877       0x40000000     USART1     0x289489777       0x40000000     I2C1     0x289489777       0x40000000     GPIO     0x289489777       0x40000000     GPIO     0x289489777       0x40000000     GPIO     0x289489777       0x400000	0x4001e400				0x43111111
Ox4001400 0x4001400 0x4001400     CRYPTO0 (bit-band)     0x430000 0x430000       0x4001400 0x4001400     GPCRC     0x430000       0x4001400     0x4001400     0x430000       0x4001400     0x4001400     0x440000       0x4001400     0x4001400     0x440000       0x4001400     0x40000     0x440000       0x4001400     0x400000     0x4400000       0x4001800     0x4400000     0x4400000       0x4001800     0x4400000     0x4400000       0x40018400     0x4400000     0x44000000       0x4001800     0x4400000     0x4400000       0x4001800     0x5400000     0x5400000       0x4001800     0x5400000     0x5400000       0x4001800     0x5400000     0x5400000       0x4001800     0x5400000     0x5400000       0x4000000     0x5400000     0x2000000       0x4000000     0x200000     0x200000       0x40000000     0x2000000     0x2000000       0x40000000     0x2000000     0x2000000       0x40000000     0x20000000     0x2000000  <	0x4001e000	CRYOTIMER			0x43008000
Ox4001/000     TRNG0     0x43860000       0x4001/000     GPCRC     0x43860000       0x4001/000     0x4001/000     0x42000000       0x4001/000     0x4001/000     0x4001/000       0x4001/000     0x4001/000     0x400/000       0x4001/000     0x5ART3     0x400/000       0x40001/000     0x5ART2     0x2000000       0x40001/000     0x5ART2     0x2000000       0x4000000     0x201/000     0x22000000       0x4000000     0     0x201/000       0x40000000     0     0x201/000       0x40000000     0     0x200000       0x400000000     0     0x2000000	0x4001d400			CRYPTO0 (bit-band)	0x43e0/ttt
Ox40012400     Ox4012400     Ox40312400     Ox40312400       0x40012400     GPCRC     0x4011600     0x4011600       0x40012400     WTIMER1     0x4001800     0x4011600       0x40012400     WTIMERD     0x4001800     0x4001800       0x4001800     TIMER0     0x4001800     0x4001800       0x4001800     TIMER0     0x4001800     0x4001800       0x4001800     TIMER0     0x4001800     0x4001800       0x4001800     USART3     0x4001800     0x23006060       0x4001800     USART1     0x23006060     0x23006060       0x4001800     USART1     0x23006060     0x23006060       0x40001800     USART0     0x23006060     0x23006060       0x40008000     USART0     0x2006060     0x2006060       0x40005000     GPIO     0x2001800     0x2001600       0x40005000     USART0     0x2006060     0x2006060       0x40005000     Code     0x2006060     0x2006060       0x40005000     UDAC0     0x2006060     0x2006060       0x40005000	0x4001d000	TRNG0			0x43e00000
Ortholic Loc     GPCRC     Templet de (oc cond)     0x42000000       0x40012000     0x4001400     0x44001400     0x44001400       0x40014000     0x4001400     0x44001600     0x44001600       0x4001800     0x4001400     0x440016000     0x440016000       0x4001800     0x4001800     0x440016000     0x440016000       0x4001800     0x4001800     0x440016000     0x440016000       0x4001800     0x40011000     0x4200171     0x44001600       0x4001000     USART3     0x22060600     0x22060600       0x40001000     USART1     0x22060600     0x221ffffff       0x4000000     USART2     0x20046000     0x22060600       0x4000000     12C0     0x20046000     0x20046800       0x4000000     GPIO     0x20046800     0x20046800       0x4000000     GPIO     0x20046800     0x20046800       0x4000000     GPIO     0x20046800     0x20046800       0x40000000     GPIO     0x20046800     0x20046800       0x40000000     GPIO     0x20041fff     0x200406800 <td>0x4001c400</td> <td></td> <td></td> <td>Peripherals (hit-band)</td> <td>0x43dfffff</td>	0x4001c400			Peripherals (hit-band)	0x43dfffff
0.44001400     WTIMER1     0x401ffff       0x4001a00     WTIMER0     0x400f60f       0x4001a00     WTIMER1     0x400f60f       0x4001a00     WTIMER1     0x400f60f       0x4001a00     WTIMER1     0x400f60ff       0x4001a00     0x400ffff     0x400fffff       0x4001a00     USART3     0x420fffff       0x4001a00     USART1     0x220ffffff       0x4001a00     USART1     0x220ffffff       0x4000c800     USART0     0x220fffff       0x4000c400     USART0     0x220fffff       0x4000c800     I2C1     0x20040000       0x4000c800     I2C0     0x20040000       0x4000c800     GPIO     0x2001ffff       0x4000c800     I2C0     0x20004000       0x4000c800     O     0x2001ffff       0x4000c800     O     0x2001fffff       0x4000c800     IDAC0     0x1ffffff       0x4000c800     ACMP1     0x20004000       0x4000c800     ACMP1     0x80090000	0x4001c400	GPCRC		r enprierais (sie sana)	0×42000000
Ox4001ab00     WTIMER1     0x400fab00       0x4001a000     WTIMER0     0x400fab00       0x4001a000     WTIMER1     0x400f80f       0x4001a000     TIMER1     0x400f80f       0x4001a000     TIMER1     0x400f80f       0x4001a000     TIMER0     0x400f80f       0x4001a000     TIMER0     0x400f80f       0x4001a000     USART3     0x400f80f       0x40010800     USART1     0x22060060       0x40010000     USART0     0x22060060       0x40001000     USART0     0x22060060       0x4000c000     I2C1     0x2004080f       0x4000c000     I2C1     0x2004080f       0x4000c000     GPIO     0x2004080f       0x4000c000     GPIO     0x200200606       0x40006000     IDACO     0x2002000       0x40006000     IDACO     0x2000606       0x40002000     ADCO     0x2000606       0x40000000     ACMP1     0x80006060       0x40000000     ACMP0     0x80006060	0x40010000				0x41ffffff
UK40014400     WTIMER0       0x4001a000     BX4006000       0x4001a000     BX40070000       0x4001a000     BX40070000       0x4001a000     BX40070000       0x40002000     BX400       0x40002000     BX4000       0x4000200	0x4001a800	WTIMER1			0x400f0400
0x40018000     TIMER1     0x4006000       0x40018000     TIMER0     0x4006000       0x40018000     USART3     0x4006000       0x40018000     USART2     0x3ffffff       0x4001000     USART3     0x23ffffff       0x4001000     USART2     0x2200000       0x4001000     USART0     0x2200000       0x4001000     USART0     0x2200000       0x4000000     USART0     0x2200000       0x4000000     0x2200000     0x2200000       0x40000000     12C1     0x200407ff       0x40000000     0     0x200407ff       0x40000000     0     0x20001ffff       0x40000000     0     0x20001ffff       0x40000000     0     0x20001ffff       0x40000000     0     0x20001ffff       0x40000000     0     0x200000       0x40000000     0     0x2000000       0x40000000     0     0x2000000       0x40000000     0     0x2000000       0x40000000     0     0x20000000       0x4000000	0x4001a400	WTIMER0	N		0x400f03ff
Draditised     TIMER1       0x40018400     TIMER0       0x40018400     TIMER0       0x4001800     0x4001000       0x4001000     USART3       0x4001000     0x3ART2       0x4001000     USART1       0x4001000     0x3ART0       0x4001000     0x210fffff       0x4001000     0x22000000       0x4001000     USART0       0x40002600     0x22000000       0x4000000     12C1       0x4000000     0x2004007ff       0x4000000     0x20040006       0x40000000     GPIO       0x40008000     0x2002000       0x40000000     0x2002000       0x40000000     0x2002000       0x40000000     0x2002000       0x40000000     0x2002000       0x40000000     0x2002000       0x40000000     0x2000200       0x40000000     0x2000200       0x40000000     ADC0       0x40000000     ACMP1       0x40000000     0x40000000	0x4001a000		`	CRYPIOU	0x400f0000
Dx40018400     TIMER0     Peripherals     0x4008000       0x40018000     USART3     0x3fffffff       0x4001000     USART2     0x22060000       0x4001000     USART1     0x22060000       0x4001000     USART0     0x22060000       0x4000000     0x22060000     0x22060000       0x4000000     0x22060000     0x22060000       0x4000000     0x2000000     0x2000000       0x4000000     0x2000000     0x2000000       0x4000000     12C0     0x20040000       0x40000000     0x2000000     0x20001000       0x40000000     GPIO     0x20040000       0x40000000     GPIO     0x20001000       0x40000000     0     0x20001000       0x40000000     0     0x20001000       0x40000000     0     0x20000000       0x40000000     0     0x20000000       0x40000000     0     0x20000000       0x40000000     0     0       0x40000000     0     0       0x400000000     0     0	0x40018800	TIMER1			0x400effff
0x40018000     0x3fffffff       0x4001000     0x3ART3       0x4001000     0x3ART2       0x4001000     0x3ART1       0x4001000     0x3ART0       0x4001000     0x22009000       0x4000000     0x22009000       0x4000000     0x22009000       0x4000000     0x22004007       0x4000000     0x200000       0x40000000     0x2000000       0x40000000     0x2000000       0x40000000     0x2000000       0x40000000     0x2000000       0x40000000     0x2000000       0x40000000     0x2000000       0x400000000     0x20000000  <	0x40018400	TIMER0		Peripherals	0×40000000
0x40011000     USART3     0x24000000       0x4001000     USART2     0x23ffffff       0x4001000     USART1     0x22000000       0x4001000     USART0     0x22000000       0x4000000     USART0     0x2000000       0x4000000     USART0     0x2000000       0x4000000     USART0     0x2000000       0x4000000     I2C1     0x20040800       0x4000000     GPIO     0x20040000       0x4000000     GPIO     0x20020000       0x4000000     Ox4000000     0x20000000       0x4000000     GPIO     0x2000000       0x40000000     Ox4000000     Ox4000000       0x40000000     Ox4000000     Ox4000000       0x40000000     Ox4000000     Ox4000000       0x40000000     ADCO     Ox4000000       0x40000000     ACMP1     Ox0000000       0x40000000     ACMP0     Ox0000000	0x40018000				Ov3fffffff
0x40010000     USART2     0x40010000       0x40010000     USART1     0x230fffff       0x40010000     USART0     0x22000000       0x40010000     0x21ffffff       0x40010000     0x21ffffff       0x4000000     0x21ffffff       0x4000000     0x21ffffff       0x4000000     0x21ffffff       0x4000000     0x200400ff       0x4000000     0x200400ff       0x4000000     0x200400ff       0x4000000     0x200400fff       0x40000000     0x2001fff       0x40000000     0x2001ffff       0x40000000     0x2000       0x40000000     0x2000       0x40000000     0x20000       0x40000000     0x20000       0x40000000     0x2000000       0x40000000     0x20000000       0x40000000     0x20000000	0x40011000	USART3			0x2400000
Ux40010800     USART1     SRAM (bit-band)     0X2200000       0x4001000     USART0     0x21fffff       0x4001000     0x2001000     0x22000000       0x4000000     12C1     0x20040800       0x4000000     12C0     0x2004007ff       0x4000000     0x2000000     0x20020000       0x4000000     0x2002000     0x20020000       0x4000000     0x200000     0x20020000       0x4000000     0x200000     0x20020000       0x4000000     0x200000     0x2000000       0x4000000     0x200000     0x2000000       0x40000000     0x2000000     0x2000000       0x40000000     0x200000     0x2000000       0x40000000     0x200000     0x2000000       0x40000000     0x200000     0x2000000       0x40000000     0x2000000     0x2000000       0x40000000     0x2000000     0x2000000       0x40000000     0x2000000     0x2000000       0x40000000     0x2000000     0x0000000       0x40000000     0x00000000     0x0000000	0x40010c00	USART2			0x22ffffff
0x40010000     USARTO     0x220f0000       0x40010000     0x220f0000     0x220f0000       0x40010000     12C1     0x2004000       0x4000000     12C0     0x2004000       0x4000000     12C0     0x2004000       0x4000000     0     0x20040000       0x4000000     0     0x2004000       0x4000000     0     0x20040000       0x4000000     0     0x20040000       0x4000000     0     0x20020000       0x4000000     0     0x2000000       0x40000000     0     0x2000000       0x40000000     0     0x20000000       0x40000000     0     0x20000000       0x40000000     0     0       0x400000000     0     0       0x400000000     0     0       0x4000000000 <td>0x40010800</td> <td>USART1</td> <td>/</td> <td>SRAM (bit-band)</td> <td>0x23111111</td>	0x40010800	USART1	/	SRAM (bit-band)	0x23111111
0x40010000     0x12C1     0x2004000       0x40002600     12C1     0x2004000       0x40002000     12C0     0x20040000       0x40002000     0x20040000     0x20040000       0x40002000     GPIO     0x20040000       0x40008000     0x2002000     0x2002000       0x40008000     VDACO     0x2002000       0x40002000     IDACO     0x20020000       0x40002000     ADCO     0x1fffff       0x40000000     ADCO     0x1ffffff       0x40000000     ADCO     0x4000000       0x40000000     ADCO     0x4000000       0x40000000     ACMP1     0x0000000	0x40010400	USARTO			0x22000000
0x4000c800     12C1     0x200408989       0x4000c400     12C0     0x200408989       0x4000c000     12C0     0x200408989       0x4000c000     0x2004007ff     0x200408989       0x4000c000     GPIO     0x20040000       0x40008000     GPIO     0x20040000       0x40008000     0x20020000     0x20020000       0x40008000     0x200000     0x2000000       0x40008000     0x2000000     0x2000000       0x40002000     0x200000     0x2000000       0x40002000     ADC0     0x2000000       0x40000000     ACMP1     0x00000000	0x40010000				UX21TTTTTT
0x4000c400     12C0     RAM2     0x200407ff       0x4000c000     0x20004000     0x20040000     0x20040000       0x40000000     GPIO     RAM1     0x20037fff       0x40008000     VDACO     0x20040000     0x20020000       0x40000000     IDACO     0x200000000     0x200000000       0x40008000     IDACO     0x200000000     0x20000000000000000       0x40002000     ADCO     0x200000000000000000000000000000000000	0x4000c800	I2C1			0x20040800
0x4000000     0x200400000     0x200400000       0x4000b000     GPIO     0x20020000       0x4000b000     0x20020000     0x20020000       0x4000b000     0x20020000     0x20020000       0x4000b000     0x20020000     0x200200000       0x40000000     IDACO     0x200200000       0x40000000     ADCO     0x1ffffff       0x40000000     ADCO     0x1ffffff       0x40000000     ADCO     0x4000000       0x40000000     ACMP1     0x00000000       0x40000000     ACMPD     0x00000000	0x4000c400	12C0	/	RAM2	0x200407††
0x4000b000     GPIO     RAM1     0x2003/fff       0x4000a000     0     0x2003/fff     0x2003/fff     0x2003/fff       0x40008000     VDACO     RAM1     0x2003/fff     0x2003/fff       0x40008000     VDACO     RAM1     0x2003/fff     0x2003/fff       0x40008000     IDACO     0x20000/ff     0x200000/ff     0x20000000       0x40002000     ADCO     0x1ffffff     0x1ffffff       0x40000000     ACMP1     0x0000000     0x00000000	0x4000c000			(data space)	0x20040000
0x4000a000     0x40       0x4000a000     VDAC0       0x40008000     VDAC0       0x40008000     RAM0     0x20020000       0x40008000     IDAC0     0x2000000       0x40008000     Code     0x1ffffff       0x4000800     Code     0x20000000       0x4000800     ACMP1     0x0000000       0x40000000     ACMP1     0x00000000	0x4000b000	GPIO		RAM1	0x2003ffff
0x40008400     VDAC0     RAM0     0x2001fff       0x40008000     0x20001fff     0x2000000     0x20000000       0x40002400     IDAC0     0x1ffffff     0x1ffffff       0x40008000     ADC0     0x1ffffff     0x1ffffff       0x4000000     ADC0     Code     0x1fffffff       0x4000000     ACMP1     0x0000000     0x0000000	0x4000a000			(data space)	0x20020000
0x40008000     10x100       0x40008000     (data space)     0x20000000       0x40006000     IDAC0     0x1ffffff       0x40002000     ADC0     Code       0x40000000     ACMP1     0x0000000       0x40000000     ACMP0     0x0000000	0x40008400	VDACO	/	RAMO	0x2001ffff
0x40006400     IDAC0     0x1ffffff       0x40006000     ADC0     0x1fffffff       0x40002000     ADC0     Code       0x40000800     ACMP1     0x0000000       0x40000000     ACMP0     0x00000000	0x40008000	15,66		(data space)	0x20000000
0x40006000     ADC0       0x40002400     ADC0       0x40002000     Code       0x40000800     ACMP1       0x40000000     ACMP0	0x40006400				0x1fffffff
0x40002400     ADC0     Code       0x40000800     ACMP1     0x40000000     0x400000000     0x00000000000000000000000000000000000	0x40006000				
0x40002000 0x40000800 0x40000000 0x40000000 ACMP0 0x0000000 ACMP0	0x40002400	ADC0			
0x40000800 0x40000400 0x40000000 ACMP0 0x0000000	0x40002000	ADCU		Code	
0x40000400 0x40000000 ACMP0	0x40000800	ACMP1			
0x4000000 ACMPU	0x40000400				0,00000000
	0x40000000	ACMPU	V		0,00000000

Figure 3.3. EFM32JG12 Memory Map — Peripherals

## 4.1.4 DC-DC Converter

Test conditions: L\_DCDC=4.7 µH (Murata LQH3NPN4R7MM0L), C\_DCDC=4.7 µF (Samsung CL10B475KQ8NQNC), V\_DCDC\_I=3.3 V, V\_DCDC\_O=1.8 V, I\_DCDC\_LOAD=50 mA, Heavy Drive configuration, F\_DCDC\_LN=7 MHz, unless otherwise indicated.

### Table 4.4. DC-DC Converter

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Input voltage range	V <sub>DCDC_I</sub>	Bypass mode, I <sub>DCDC_LOAD</sub> = 50 mA	1.8	—	V <sub>VREGVDD</sub> MAX	V
		Low noise (LN) mode, 1.8 V out- put, $I_{DCDC\_LOAD}$ = 100 mA, or Low power (LP) mode, 1.8 V out- put, $I_{DCDC\_LOAD}$ = 10 mA	TBD	_	Vvregvdd_ Max	V
		Low noise (LN) mode, 1.8 V out- put, I <sub>DCDC_LOAD</sub> = 200 mA	TBD	_	V <sub>VREGVDD</sub> MAX	V
Output voltage programma- ble range <sup>1</sup>	V <sub>DCDC_O</sub>		1.8	—	V <sub>VREGVDD</sub>	V
Regulation DC accuracy	ACC <sub>DC</sub>	Low Noise (LN) mode, 1.8 V tar- get output	TBD		TBD	V
Regulation window <sup>4</sup>	WIN <sub>REG</sub>	Low Power (LP) mode, LPCMPBIASEMxx <sup>3</sup> = 0, 1.8 V tar- get output, I <sub>DCDC_LOAD</sub> ≤ 75 µA	TBD	_	TBD	V
		Low Power (LP) mode, LPCMPBIASEMxx <sup>3</sup> = 3, 1.8 V tar- get output, I <sub>DCDC_LOAD</sub> ≤ 10 mA	TBD	_	TBD	V
Steady-state output ripple	V <sub>R</sub>		_	3	_	mVpp
Output voltage under/over- shoot	Vov	CCM Mode (LNFORCECCM <sup>3</sup> = 1), Load changes between 0 mA and 100 mA	_	_	TBD	mV
		DCM Mode (LNFORCECCM <sup>3</sup> = 0), Load changes between 0 mA and 10 mA	_	_	TBD	mV
		Overshoot during LP to LN CCM/DCM mode transitions com- pared to DC level in LN mode	_	200	_	mV
		Undershoot during BYP/LP to LN CCM (LNFORCECCM <sup>3</sup> = 1) mode transitions compared to DC level in LN mode		50	_	mV
		Undershoot during BYP/LP to LN DCM (LNFORCECCM <sup>3</sup> = 0) mode transitions compared to DC level in LN mode		125	_	mV
DC line regulation	V <sub>REG</sub>	Input changes between V <sub>VREGVDD_MAX</sub> and 2.4 V	_	0.1	—	%
DC load regulation	I <sub>REG</sub>	Load changes between 0 mA and 100 mA in CCM mode		0.1	_	%

## 4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output.  $T_{OP}$  = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at  $T_{OP}$  = 25 °C.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_DCM	38.4 MHz crystal, CPU running while loop from flash <sup>4</sup>	_	86	_	µA/MHz
DCM mode <sup>2</sup> .		38 MHz HFRCO, CPU running Prime from flash	_	70	_	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	_	70	_	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	85	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	77		µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	636	_	µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_CCM	38.4 MHz crystal, CPU running while loop from flash <sup>4</sup>	_	96	_	µA/MHz
CCM mode <sup>1</sup> .		38 MHz HFRCO, CPU running Prime from flash	_	81	_	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	_	82	_	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	_	95	_	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	_	95	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	1155	_	µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_LPM	38.4 MHz crystal, CPU running while loop from flash <sup>4</sup>	_	80	_	µA/MHz
abled, DCDC in LP mode <sup>3</sup> .		38 MHz HFRCO, CPU running Prime from flash	_	64	_	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	_	64	_	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	_	79	_	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	66	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	_	224		µA/MHz
Current consumption in EM0 mode with all peripherals dis-	IACTIVE_CCM_VS	19 MHz HFRCO, CPU running while loop from flash		101		µA/MHz
abled and voltage scaling enabled, DCDC in Low		1 MHz HFRCO, CPU running while loop from flash		1128	_	µA/MHz

## Table 4.6. Current Consumption 3.3 V using DC-DC Converter

## 4.1.7 Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
DVDD BOD threshold	V <sub>DVDDBOD</sub>	DVDD rising	_	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	_	_	V
		DVDD falling (EM2/EM3)	TBD	—	_	V
DVDD BOD hysteresis	V <sub>DVDDBOD_HYST</sub>		—	18	_	mV
DVDD BOD response time	t <sub>DVDDBOD_DELAY</sub>	Supply drops at 0.1V/µs rate	_	2.4	_	μs
AVDD BOD threshold	V <sub>AVDDBOD</sub>	AVDD rising	_	—	TBD	V
		AVDD falling (EM0/EM1)	TBD	—	_	V
		AVDD falling (EM2/EM3)	TBD	—	_	V
AVDD BOD hysteresis	V <sub>AVDDBOD_HYST</sub>		_	20	_	mV
AVDD BOD response time	tavddbod_delay	Supply drops at 0.1V/µs rate	_	2.4	_	μs
EM4 BOD threshold	V <sub>EM4DBOD</sub>	AVDD rising	_	_	TBD	V
		AVDD falling	TBD	—	_	V
EM4 BOD hysteresis	V <sub>EM4BOD_HYST</sub>		_	25	_	mV
EM4 BOD response time	t <sub>EM4BOD_DELAY</sub>	Supply drops at 0.1V/µs rate	_	300	_	μs

## Table 4.9. Brown Out Detector (BOD)

## 4.1.8.2 High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Тур	Мах	Unit
Crystal frequency	f <sub>HFXO</sub>		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR <sub>HFXO_38M4</sub>	Crystal frequency 38.4 MHz	_	_	60	Ω
Supported range of crystal load capacitance <sup>1</sup>	C <sub>HFXO_CL</sub>		6	_	12	pF
On-chip tuning cap range <sup>2</sup>	C <sub>HFXO_T</sub>	On each of HFXTAL_N and HFXTAL_P pins	TBD	20	TBD	pF
On-chip tuning capacitance step	SS <sub>HFXO</sub>		_	0.04	_	pF
Startup time	t <sub>HFXO</sub>	38.4 MHz, ESR = 50 Ohm, C <sub>L</sub> = 10 pF	_	300	_	μs
Frequency tolerance for the crystal	FT <sub>HFXO</sub>	38.4 MHz, ESR = 50 Ohm, C <sub>L</sub> = 10 pF	-40		40	ppm

## Table 4.11. High-Frequency Crystal Oscillator (HFXO)

## Note:

1. Total load capacitance as seen by the crystal.

2. The effective load capacitance seen by the crystal will be C<sub>HFXO\_T</sub> /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. .

## 4.1.8.3 Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Oscillation frequency	f <sub>LFRCO</sub>	ENVREF <sup>2</sup> = 1	TBD	32.768	TBD	kHz
		ENVREF <sup>2</sup> = 1, T <sub>AMB</sub> > 85 °C	TBD	32.768	TBD	kHz
		ENVREF <sup>2</sup> = 0	TBD	32.768	TBD	kHz
		ENVREF <sup>2</sup> = 0, T <sub>AMB</sub> > 85 °C	TBD	32.768	TBD	kHz
Startup time	t <sub>LFRCO</sub>		_	500	_	μs
Current consumption <sup>1</sup>	I <sub>LFRCO</sub>	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

### Note:

1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU\_PWRCTRL register.

2. in CMU\_LFRCOCTRL register.

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Frequency accuracy	fHFRCO_ACC	At production calibrated frequen- cies, across supply voltage and temperature	TBD	_	TBD	%
Start-up time	t <sub>HFRCO</sub>	f <sub>HFRCO</sub> ≥ 19 MHz	—	300	_	ns
		4 < f <sub>HFRCO</sub> < 19 MHz	—	1	_	μs
		f <sub>HFRCO</sub> ≤ 4 MHz	—	2.5		μs
Maximum DPLL lock time <sup>1</sup>	t <sub>DPLL_LOCK</sub>	f <sub>REF</sub> = 32.768 kHz, f <sub>HFRCO</sub> = 39.98 MHz, N = 1219, M = 0		183	_	μs
Current consumption on all	I <sub>HFRCO</sub>	f <sub>HFRCO</sub> = 38 MHz	—	244	TBD	μA
supplies		f <sub>HFRCO</sub> = 32 MHz	—	204	TBD	μA
		f <sub>HFRCO</sub> = 26 MHz	—	173	TBD	μA
		f <sub>HFRCO</sub> = 19 MHz	—	143	TBD	μA
		f <sub>HFRCO</sub> = 16 MHz	—	123	TBD	μA
		f <sub>HFRCO</sub> = 13 MHz	—	110	TBD	μA
		f <sub>HFRCO</sub> = 7 MHz	—	85	TBD	μA
		f <sub>HFRCO</sub> = 4 MHz	—	32	TBD	μA
		f <sub>HFRCO</sub> = 2 MHz	—	31	TBD	μA
		f <sub>HFRCO</sub> = 1 MHz	—	30	TBD	μA
		f <sub>HFRCO</sub> = 40 MHz, DPLL enabled	—	385	TBD	μA
		f <sub>HFRCO</sub> = 32 MHz, DPLL enabled	—	310		μA
		f <sub>HFRCO</sub> = 16 MHz, DPLL enabled	—	203		μA
		f <sub>HFRCO</sub> = 4 MHz, DPLL enabled	—	95	_	μA
		f <sub>HFRCO</sub> = 1 MHz, DPLL enabled	—	79	_	μA
Coarse trim step size (% of period)	SS <sub>HFRCO_COARS</sub> E		_	0.8	_	%
Fine trim step size (% of pe- riod)	SS <sub>HFRCO_FINE</sub>		_	0.1		%
Period jitter	PJ <sub>HFRCO</sub>		_	0.2	_	% RMS
Note:	·					

Table 4.13. High-Fregency RC Oscillator (HFRCO	able 4.13.	4.13. High-Fregenc	v RC Oscillato	r (HFRCO)
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1. Maximum DPLL lock time ~= 6 x (M+1) x t<sub>REF</sub>, where t<sub>REF</sub> is the reference clock period.

# 4.1.11 Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Supply current (including I_SENSE)	I <sub>VMON</sub>	In EM0 or EM1, 1 supply moni- tored	—	6.3	TBD	μA
		In EM0 or EM1, 4 supplies moni- tored	_	12.5	TBD	μA
		In EM2, EM3 or EM4, 1 supply monitored and above threshol		62	_	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	_	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold		99		nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	_	nA
Loading of monitored supply	I <sub>SENSE</sub>	In EM0 or EM1	—	2	_	μA
		In EM2, EM3 or EM4	—	2	_	nA
Threshold range	V <sub>VMON_RANGE</sub>		1.62	_	3.4	V
Threshold step size	N <sub>VMON_STESP</sub>	Coarse	_	200	_	mV
		Fine	—	20	_	mV
Response time	t <sub>VMON_RES</sub>	Supply drops at 1V/µs rate	_	460	_	ns
Hysteresis	V <sub>VMON_HYST</sub>			26	_	mV

## Table 4.18. Voltage Monitor (VMON)

### **SPI Slave Timing**

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
SCLK period <sup>1 3 2</sup>	t <sub>SCLK</sub>		8 * t <sub>HFPERCLK</sub>	_	—	ns
SCLK high time <sup>1 3 2</sup>	t <sub>SCLK_HI</sub>		3 * t <sub>HFPERCLK</sub>	—	—	ns
SCLK low time <sup>1 3 2</sup>	t <sub>SCLK_LO</sub>		3 * <sup>t</sup> HFPERCLK	—	_	ns
CS active to MISO <sup>1 3</sup>	t <sub>CS_ACT_MI</sub>		4	_	50	ns
CS disable to MISO <sup>1 3</sup>	tcs_dis_mi		4	_	50	ns
MOSI setup time <sup>1 3</sup>	t <sub>SU_MO</sub>		4	_	_	ns
MOSI hold time <sup>1 3 2</sup>	t <sub>H_MO</sub>		3 + 2 * t <sub>HFPERCLK</sub>	—	—	ns
SCLK to MISO <sup>1 3 2</sup>	t <sub>SCLK_MI</sub>		16 + t <sub>HFPERCLK</sub>	_	66 + 2 * t <sub>HFPERCLK</sub>	ns

## Table 4.31. SPI Slave Timing

### Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).

2.  $t_{\text{HFPERCLK}}$  is one period of the selected HFPERCLK.

3. Measurement done with 8 pF output loading at 10% and 90% of  $V_{DD}$  (figure shows 50% of  $V_{DD}$ ).



## Figure 4.2. SPI Slave Timing Diagram

## 4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.



Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

	Pin	Pin Alternate Functionality / Description									
Pin #	Pin Name	Analog	Timers	Communication	Other						
G13	PIO	BUSADC0Y BU- SADC0X		US2_TX #5 US2_RX #4 US2_CLK #3 US2_CS #2 US2_CTS #1 US2_RTS #0	LES_ALTEX4						
H1	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC3 #28 WTIM1_CC3 #28 WTIM1_CC1 #29 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE- TIM0_OUT0 #31 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1						
H2	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC3 #27 WTIM1_CC3 #27 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE- TIM0_OUT0 #30 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30						
H5	VSS	Ground	1	1	1						
H6	VSS	Ground									
H7	VSS	Ground									
H8	VSS	Ground									
H9	VSS	Ground									

	Pin	Pin Alternate Functionality / Description										
Pin #	Pin Name	Analog	Timers	Communication	Other							
J13	PA5	VDAC0_OUT0ALT / OPA0_OUTALT #0 BUSCY BUSDX	TIM0_CC0 #5 TIM0_CC1 #4 TIM0_CC2 #3 TIM0_CDTI0 #2 TIM0_CDTI1 #1 TIM0_CDTI2 #0 TIM1_CC0 #5 TIM1_CC1 #4 TIM1_CC2 #3 TIM1_CC3 #2 WTIM0_CC0 #5 WTIM0_CC0 #5 WTIM0_CC2 #1 LE- TIM0_OUT0 #5 LE- TIM0_OUT1 #4 PCNT0_S0IN #5 PCNT0_S1IN #4	US0_TX #5 US0_RX #4 US0_CLK #3 US0_CS #2 US0_CTS #1 US0_RTS #0 US1_TX #5 US1_RX #4 US1_CLK #3 US1_CS #2 US1_CTS #1 US1_RTS #0 US2_TX #0 US2_RX #31 US2_CLK #30 US2_CS #29 US2_CTS #28 US2_RTS #27 LEU0_TX #5 LEU0_RX #4 I2C0_SDA #5 I2C0_SCL #4	CMU_CLKI0 #4 PRS_CH6 #5 PRS_CH7 #4 PRS_CH8 #3 PRS_CH9 #2 ACMP0_O #5 ACMP1_O #5 LES_CH13 ETM_TCLK #1							
K1	HFXTAL_N	High Frequency Crystal input pin.										
K2	VSS	Ground										
K12	PA4	VDAC0_OUT1ALT / OPA1_OUTALT #2 BUSDY BUSCX OPA0_N	TIM0_CC0 #4 TIM0_CC1 #3 TIM0_CC2 #2 TIM0_CDTI0 #1 TIM0_CDTI1 #0 TIM0_CDTI2 #31 TIM1_CC0 #4 TIM1_CC1 #3 TIM1_CC2 #2 TIM1_CC3 #1 WTIM0_CC0 #4 WTIM0_CC1 #2 WTIM0_CC2 #0 LE- TIM0_OUT0 #4 LE- TIM0_OUT1 #3 PCNT0_S0IN #4 PCNT0_S1IN #3	US0_TX #4 US0_RX #3 US0_CLK #2 US0_CS #1 US0_CTS #0 US0_RTS #31 US1_TX #4 US1_RX #3 US1_CLK #2 US1_CS #1 US1_CTS #0 US1_RTS #31 LEU0_TX #4 LEU0_RX #3 I2C0_SDA #4 I2C0_SCL #3	PRS_CH6 #4 PRS_CH7 #3 PRS_CH8 #2 PRS_CH9 #1 ACMP0_O #4 ACMP1_O #4 LES_CH12							
K13	PA3	BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8							
L1	HFXTAL_P	High Frequency Crystal o	utput pin.									
L2	VSS	Ground										
L10	BODEN	Brown-Out Detector Enab	le. This pin may be left dis	sconnected or tied to AVDE	D.							

	Pin	Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Timers	Communication	Other					
N12	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDT10 #30 WTIM0_CDT12 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC2 #18 WTIM1_CC2 #18 WTIM1_CC3 #16 LE- TIM0_OUT0 #22 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4					
N13	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI0 #31 WTIM0_CDT12 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC2 #19 WTIM1_CC2 #19 WTIM1_CC3 #17 LE- TIM0_OUT0 #23 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2					

	Pin	Pin Alternate Functionality / Description								
Pin #	Pin Name	Analog	Timers	Communication Other						
6	PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDT10 #26 TIM0_CDT11 #25 TIM0_CDT12 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 WTIM1_CC3 #26 WTIM1_CC1 #27 WTIM1_CC1 #27 WTIM1_CC2 #25 WTIM1_CC3 #23 LE- TIM0_OUT0 #29 LE- TIM0_OUT0 #29 LE- TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29					
7	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC3 #27 WTIM1_CC3 #24 UTIM1_CC3 #24 LE- TIM0_OUT0 #30 LE- TIM0_OUT0 #30 LE- TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30					
8	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC3 #28 WTIM1_CC3 #28 WTIM1_CC1 #29 WTIM1_CC1 #29 WTIM1_CC3 #25 LE- TIM0_OUT0 #31 LE- TIM0_OUT0 #31 LE- TIM0_OUT0 #31 LE- TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1					
9	AVDD	Analog power supply .								

	Pin		Pin Alternate Functi	onality / Description	
Pin #	Pin Name	Analog	Timers	Communication	Other
26	PA1	BUSCY BUSDX ADC0_EXTP VDAC0_EXT	TIM0_CC0 #1 TIM0_CC1 #0 TIM0_CC2 #31 TIM0_CDT10 #30 TIM0_CDT11 #29 TIM0_CDT12 #28 TIM1_CC0 #1 TIM1_CC1 #0 TIM1_CC2 #31 TIM1_CC3 #30 WTIM0_CC0 #1 LE- TIM0_OUT0 #1 LE- TIM0_OUT0 #1 LE- TIM0_OUT1 #0 PCNT0_S0IN #1 PCNT0_S1IN #0	US0_TX #1 US0_RX #0 US0_CLK #31 US0_CS #30 US0_CTS #29 US0_RTS #28 US1_TX #1 US1_RX #0 US1_CLK #31 US1_CS #30 US1_CTS #29 US1_RTS #28 LEU0_TX #1 LEU0_RX #0 I2C0_SDA #1 I2C0_SCL #0	CMU_CLK0 #0 PRS_CH6 #1 PRS_CH7 #0 PRS_CH8 #10 PRS_CH9 #9 ACMP0_O #1 ACMP1_O #1 LES_CH9
27	PA2	VDAC0_OUT1ALT / OPA1_OUTALT #1 BUSDY BUSCX OPA0_P	TIM0_CC0 #2     TIM0_CC1 #1     TIM0_CDTI0 #31     TIM0_CDTI0 #31     TIM0_CDTI0 #31     TIM0_CDTI1 #30     TIM0_CDTI1 #30     TIM0_CDTI2 #29     TIM1_CC0 #2     TIM1_CC1 #1     BUSDY BUSCX     OPA0_P     TIM1_CC3 #31     WTIM0_CC1 #0 LE-     TIM0_OUT0 #2 LE-     TIM0_OUT1 #1     PCNT0_S0IN #2     PCNT0_S1IN #1		PRS_CH6 #2 PRS_CH7 #1 PRS_CH8 #0 PRS_CH9 #10 ACMP0_O #2 ACMP1_O #2 LES_CH10
28	PA3	BUSCY BUSDX VDAC0_OUT0 / OPA0_OUT	TIM0_CC0 #3 TIM0_CC1 #2 TIM0_CC2 #1 TIM0_CDTI0 #0 TIM0_CDTI1 #31 TIM0_CDTI2 #30 TIM1_CC0 #3 TIM1_CC1 #2 TIM1_CC2 #1 TIM1_CC3 #0 WTIM0_CC0 #3 WTIM0_CC1 #1 LE- TIM0_OUT0 #3 LE- TIM0_OUT1 #2 PCNT0_S0IN #3 PCNT0_S1IN #2	US0_TX #3 US0_RX #2 US0_CLK #1 US0_CS #0 US0_CTS #31 US0_RTS #30 US1_TX #3 US1_RX #2 US1_CLK #1 US1_CS #0 US1_CTS #31 US1_RTS #30 LEU0_TX #3 LEU0_RX #2 I2C0_SDA #3 I2C0_SCL #2	PRS_CH6 #3 PRS_CH7 #2 PRS_CH8 #1 PRS_CH9 #0 ACMP0_O #3 ACMP1_O #3 LES_CH11 GPIO_EM4WU8

Alternate				LOCA	ATION				
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
US1_RTS	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	USART1 Request To Send hardware flow control output.
US1_RX	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	USART1 Asynchro- nous Receive. USART1 Synchro- nous mode Master Input / Slave Out- put (MISO).
US1_TX	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	USART1 Asynchro- nous Transmit. Al- so used as receive input in half duplex communication. USART1 Synchro- nous mode Master Output / Slave In- put (MOSI).
US2_CLK	0: PA7 1: PA8 2: PA9 3: PI0	4: PI1 5: PI2 6: PI3 7: PB6	8: PB7 9: PB8 10: PB9 11: PB10	12: PF0 13: PF1 14: PF3 15: PF4	16: PF5 17: PF6 18: PF7 19: PF8	20: PF9 21: PF10 22: PF11 23: PF12	24: PF13 25: PF14 26: PF15 27: PK0	28: PK1 29: PK2 30: PA5 31: PA6	USART2 clock in- put / output.
US2_CS	0: PA8 1: PA9 2: PI0 3: PI1	4: Pl2 5: Pl3 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PF0	12: PF1 13: PF3 14: PF4 15: PF5	16: PF6 17: PF7 18: PF8 19: PF9	20: PF10 21: PF11 22: PF12 23: PF13	24: PF14 25: PF15 26: PK0 27: PK1	28: PK2 29: PA5 30: PA6 31: PA7	USART2 chip se- lect input / output.
US2_CTS	0: PA9 1: Pl0 2: Pl1 3: Pl2	4: PI3 5: PB6 6: PB7 7: PB8	8: PB9 9: PB10 10: PF0 11: PF1	12: PF3 13: PF4 14: PF5 15: PF6	16: PF7 17: PF8 18: PF9 19: PF10	20: PF11 21: PF12 22: PF13 23: PF14	24: PF15 25: PK0 26: PK1 27: PK2	28: PA5 29: PA6 30: PA7 31: PA8	USART2 Clear To Send hardware flow control input.
US2_RTS	0: PI0 1: PI1 2: PI2 3: PI3	4: PB6 5: PB7 6: PB8 7: PB9	8: PB10 9: PF0 10: PF1 11: PF3	12: PF4 13: PF5 14: PF6 15: PF7	16: PF8 17: PF9 18: PF10 19: PF11	20: PF12 21: PF13 22: PF14 23: PF15	24: PK0 25: PK1 26: PK2 27: PA5	28: PA6 29: PA7 30: PA8 31: PA9	USART2 Request To Send hardware flow control output.
US2_RX	0: PA6 1: PA7 2: PA8 3: PA9	4: PI0 5: PI1 6: PI2 7: PI3	8: PB6 9: PB7 10: PB8 11: PB9	12: PB10 13: PF0 14: PF1 15: PF3	16: PF4 17: PF5 18: PF6 19: PF7	20: PF8 21: PF9 22: PF10 23: PF11	24: PF12 25: PF13 26: PF14 27: PF15	28: PK0 29: PK1 30: PK2 31: PA5	USART2 Asynchro- nous Receive. USART2 Synchro- nous mode Master Input / Slave Out- put (MISO).
US2_TX	0: PA5 1: PA6 2: PA7 3: PA8	4: PA9 5: PI0 6: PI1 7: PI2	8: PI3 9: PB6 10: PB7 11: PB8	12: PB9 13: PB10 14: PF0 15: PF1	16: PF3 17: PF4 18: PF5 19: PF6	20: PF7 21: PF8 22: PF9 23: PF10	24: PF11 25: PF12 26: PF13 27: PF14	28: PF15 29: PK0 30: PK1 31: PK2	USART2 Asynchro- nous Transmit. Al- so used as receive input in half duplex communication. USART2 Synchro- nous mode Master Output / Slave In- put (MOSI).

## EFM32JG12 Family Data Sheet Pin Definitions

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	СН9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OP	A1_	N																				_											
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PCO
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PAO		PD14		PD12		PD10		PD8
OP	A1_	P																															
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
OP	A2_	N		1						1			1								1			1			1			1			
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PCO
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PAO		PD14		PD12		PD10		PD8

## 7.2 BGA125 PCB Land Pattern



Figure 7.2. BGA125 PCB Land Pattern Drawing