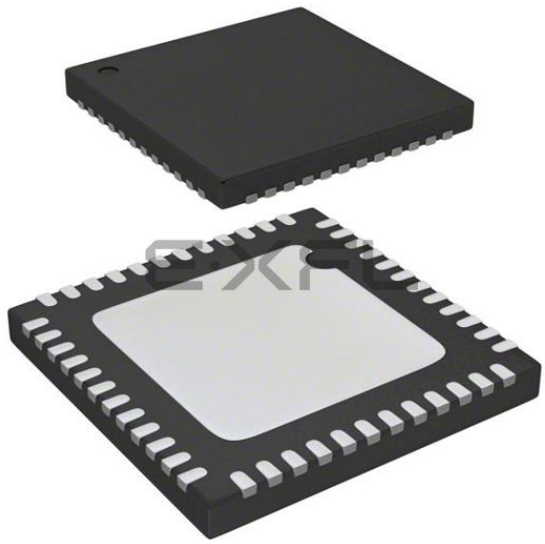
Silicon Labs - EFM32JG12B500F1024GM48-B Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg12b500f1024gm48-b

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Max load current	I_{LOAD_MAX}	Low noise (LN) mode, Heavy Drive[2], T_{amb} ≤ 85 °C	—	—	TBD	mA
		Low noise (LN) mode, Heavy Drive[2], T_{amb} > 85 °C	—	—	TBD	mA
		Low noise (LN) mode, Medium Drive[2]	—	—	TBD	mA
		Low noise (LN) mode, Light Drive[2]	—	—	TBD	mA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 0	—	—	TBD	µA
		Low power (LP) mode, LPCMPBIASEMxx[3] = 3	—	—	TBD	mA
DCDC nominal output capacitor[5]	C_{DCDC}	25% tolerance	1	4.7	4.7	µF
DCDC nominal output inductor	L_{DCDC}	20% tolerance	4.7	4.7	4.7	µH
Resistance in Bypass mode	R_{BYP}		—	1.2	TBD	Ω

Note:

1. Due to internal dropout, the DC-DC output will never be able to reach its input voltage, $V_{VREGVDD}$.
2. Drive levels are defined by configuration of the PFETCNT and NFETCNT registers. Light Drive: PFETCNT=NFETCNT=3; Medium Drive: PFETCNT=NFETCNT=7; Heavy Drive: PFETCNT=NFETCNT=15.
3. In EMU_DCDCMISCCTRL register.
4. LP mode controller is a hysteretic controller that maintains the output voltage withinthe specified limits.
5. Output voltage under/over-shoot and regulation are specified with C_{DCDC} 4.7 µF. Different control loop settings must be used if C_{DCDC} is lower than 4.7 µF.

4.1.5 Current Consumption

4.1.5.1 Current Consumption 3.3 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 3.3 V. T_{OP} = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.5. Current Consumption 3.3 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	126	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	TBD	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	TBD	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	280	TBD	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	88	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	234	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	76	—	µA/MHz
		38 MHz HFRCO	—	50	TBD	µA/MHz
		26 MHz HFRCO	—	52	TBD	µA/MHz
		1 MHz HFRCO	—	230	TBD	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	47	—	µA/MHz
		1 MHz HFRCO	—	193	—	µA/MHz
Current consumption in EM2 mode, with votage scaling enabled.	I_{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.9	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.2	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	2.1	TBD	µA
Current consumption in EM3 mode, with voltage scaling enabled.	I_{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.56	TBD	µA
Current consumption in EM4H mode, with voltage scaling enabled.	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	1.0	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.45	—	µA
		128 byte RAM retention, no RTCC	—	0.43	TBD	µA

4.1.5.3 Current Consumption 1.8 V without DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = DVDD = 1.8 V. T_{OP} = 25 °C. DCDC is off. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.7. Current Consumption 1.8 V without DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	38.4 MHz crystal, CPU running while loop from flash[1]	—	126	—	µA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	99	—	µA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	124	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	102	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	277	—	µA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled	I_{ACTIVE_VS}	19 MHz HFRCO, CPU running while loop from flash	—	87	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	231	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	38.4 MHz crystal[1]	—	76	—	µA/MHz
		38 MHz HFRCO	—	50	—	µA/MHz
		26 MHz HFRCO	—	52	—	µA/MHz
		1 MHz HFRCO	—	227	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled and voltage scaling enabled	I_{EM1_VS}	19 MHz HFRCO	—	47	—	µA/MHz
		1 MHz HFRCO	—	190	—	µA/MHz
Current consumption in EM2 mode, with votage scaling enabled.	I_{EM2_VS}	Full 256 kB RAM retention and RTCC running from LFXO	—	2.8	—	µA
		Full 256 kB RAM retention and RTCC running from LFRCO	—	3.0	—	µA
		16 kB (1 bank) RAM retention and RTCC running from LFRCO[2]	—	1.9	—	µA
Current consumption in EM3 mode, with voltage scaling enabled.	I_{EM3_VS}	Full 256 kB RAM retention and CRYOTIMER running from ULFRCO	—	2.47	—	µA
Current consumption in EM4H mode, with voltage scaling enabled.	I_{EM4H_VS}	128 byte RAM retention, RTCC running from LFXO	—	0.91	—	µA
		128 byte RAM retention, CRYOTIMER running from ULFRCO	—	0.35	—	µA
		128 byte RAM retention, no RTCC	—	0.35	—	µA
Current consumption in EM4S mode	I_{EM4S}	no RAM retention, no RTCC	—	0.04	—	µA

4.1.8.2 High-Frequency Crystal Oscillator (HFXO)

Table 4.11. High-Frequency Crystal Oscillator (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXO}		38	38.4	40	MHz
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	Crystal frequency 38.4 MHz	—	—	60	Ω
Supported range of crystal load capacitance [1]	C_{HFXO_CL}		6	—	12	pF
On-chip tuning cap range [2]	C_{HFXO_T}	On each of HFXTAL_N and HFXTAL_P pins	TBD	20	TBD	pF
On-chip tuning capacitance step	SS_{HFXO}		—	0.04	—	pF
Startup time	t_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	—	300	—	µs
Frequency tolerance for the crystal	FT_{HFXO}	38.4 MHz, ESR = 50 Ohm, C_L = 10 pF	-40	—	40	ppm

Note:
1. Total load capacitance as seen by the crystal.
2. The effective load capacitance seen by the crystal will be C_{HFXO_T} /2. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal. .

4.1.8.3 Low-Frequency RC Oscillator (LFRCO)

Table 4.12. Low-Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{LFRCO}	ENVREF[2] = 1	TBD	32.768	TBD	kHz
		ENVREF[2] = 1, T_{AMB} > 85 °C	TBD	32.768	TBD	kHz
		ENVREF[2] = 0	TBD	32.768	TBD	kHz
		ENVREF[2] = 0, T_{AMB} > 85 °C	TBD	32.768	TBD	kHz
Startup time	t_{LFRCO}		—	500	—	µs
Current consumption [1]	I_{LFRCO}	ENVREF = 1 in CMU_LFRCOCTRL	—	370	—	nA
		ENVREF = 0 in CMU_LFRCOCTRL	—	520	—	nA

Note:
1. Block is supplied by AVDD if ANASW = 0, or DVDD if ANASW=1 in EMU_PWRCTRL register.
2. in CMU_LFRCOCTRL register.

4.1.9 Flash Memory Characteristics[3]

Table 4.16. Flash Memory Characteristics[3]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		10000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB} ≤ 85 °C	10	—	—	years
		T_{AMB} ≤ 125 °C	10	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	24.4	30	µs
Page erase time	t_{PERASE}		20	26.4	35	ms
Mass erase time[1]	t_{MERASE}		20	26.5	35	ms
Device erase time[2]	t_{DERASE}	T_{AMB} ≤ 85 °C	—	69	100	ms
		T_{AMB} ≤ 125 °C	—	69	110	ms
Page erase current[4]	I_{ERASE}		—	—	1.6	mA
Write current[4]	I_{WRITE}		—	—	3.8	mA
Supply voltage during flash erase and write	V_{FLASH}		1.62	—	TBD	V

Note:

1. Mass erase is issued by the CPU and erases all flash.
2. Device erase is issued over the AAP interface and erases all flash, SRAM, the Lock Bit (LB) page, and the User data page Lock Word (ULW).
3. Flash data retention information is published in the Quarterly Quality and Reliability Report.
4. Measured at 25 °C.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	—	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	32	TBD	mV
		HYSTSEL[5] = HYST3	TBD	44	TBD	mV
		HYSTSEL[5] = HYST4	TBD	55	TBD	mV
		HYSTSEL[5] = HYST5	TBD	65	TBD	mV
		HYSTSEL[5] = HYST6	TBD	77	TBD	mV
		HYSTSEL[5] = HYST7	TBD	86	TBD	mV
		HYSTSEL[5] = HYST8	TBD	—	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-32	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-43	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-54	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-64	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-74	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-85	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	inf	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	102	—	kΩ
		CSRESSEL[6] = 6	—	164	—	kΩ
		CSRESSEL[6] = 7	—	239	—	kΩ

4.1.16 Capacitive Sense (CSEN)

Table 4.23. Capacitive Sense (CSEN)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single conversion time (1x accumulation)	t_{CNV}	12-bit SAR Conversions	—	20.2	—	µs
		16-bit SAR Conversions	—	26.4	—	µs
		Delta Modulation Conversion (single comparison)	—	1.55	—	µs
Maximum external capactive load	C_{EXTMAX}	CS0CG=7 (Gain = 1x), including routing parasitics	—	68	—	pF
		CS0CG=0 (Gain = 10x), including routing parasitics	—	680	—	pF
Maximum external series impedance	R_{EXTMAX}		—	1	—	kΩ
Supply current, EM2 scan conversions, WARMUPMODE=NORMAL, WARMUPCNT=0	I_{CSEN_EM2}	12-bit SAR conversions, 20 ms scan rate, 8 samples per scan[1]	—	800	—	nA
		Delta Modulation conversions, 20 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), 8 samples per scan[1]	—	590	—	nA
		12-bit SAR conversions, 200 ms scan rate, 8 samples per scan[1]	—	80	—	nA
		Delta Modulation conversions, 200 ms scan rate, 8 comparisons per sample (DMCR = 1, DMR = 2), 8 samples per scan[1]	—	59	—	nA
Supply current, continuous conversions, WARMUPMODE=KEEPCSENWARM	I_{CSEN_ACTIVE}	SAR or Delta Modulation conversions of 33 pF capacitor, always on	—	90.5	—	µA

Note:

1. Current is specified with a total external capacitance of 33 pF. Average current is dependent on how long the module is actively sampling channels within the scan period, and will scale linearly with the number of samples acquired. Supply current for a specific application can be caclulated by multiplying the current per sample by the total number of samples per period (total_current = single_sample_current * (number_of_channels * accumulation)).

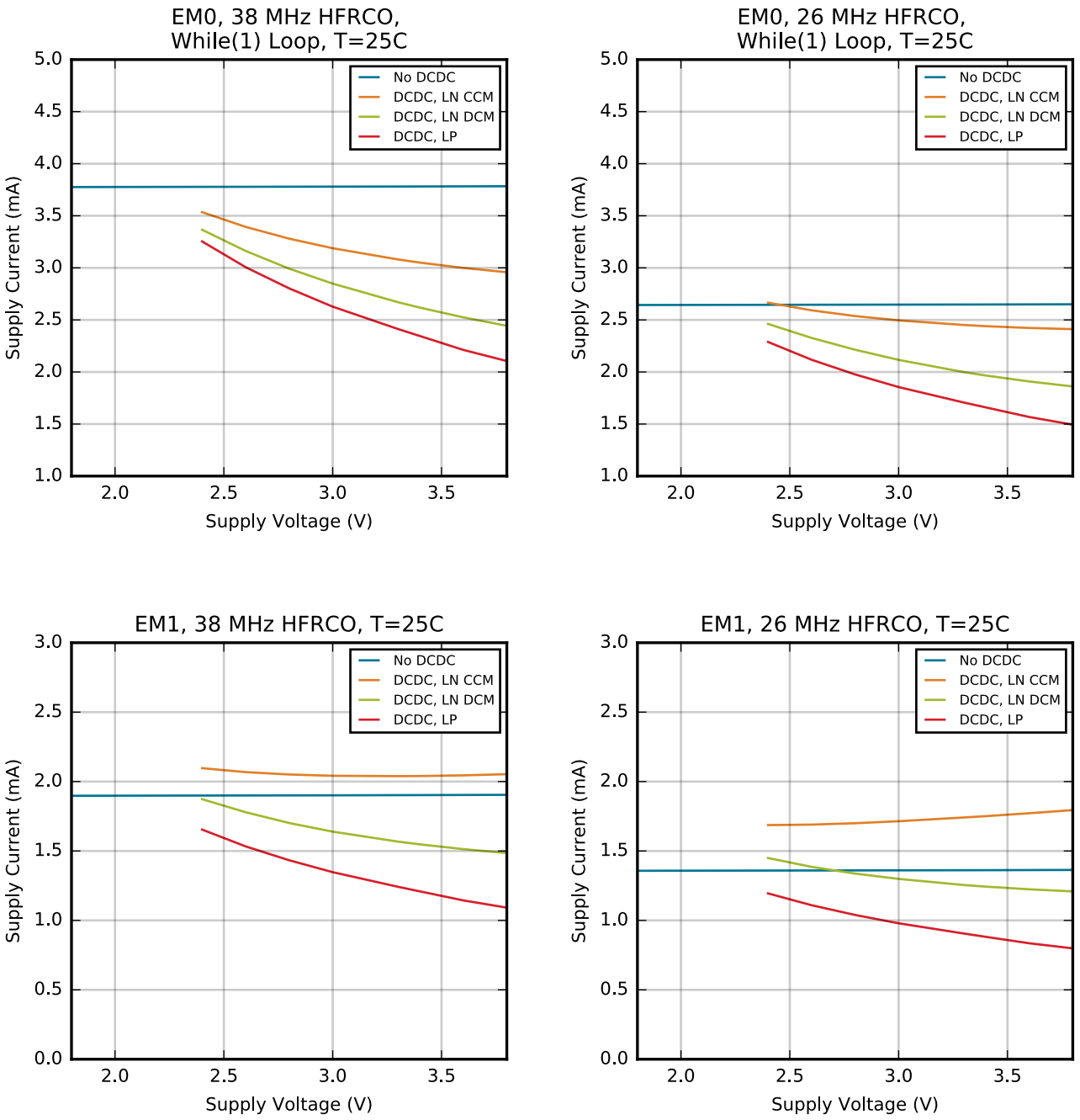

Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
A4	PC3	BUSAY BUSBX	WTIM0_CC0 #23 WTIM0_CC1 #21 WTIM0_CC2 #19 WTIM0_CDTI0 #15 WTIM0_CDTI1 #13 WTIM0_CDTI2 #11 WTIM1_CC0 #7 WTIM1_CC1 #5 WTIM1_CC2 #3 WTIM1_CC3 #1 PCNT1_S0IN #16 PCNT1_S1IN #15 PCNT2_S0IN #16 PCNT2_S1IN #15	US3_TX #21 US3_RX #20 US3_CLK #19 US3_CS #18 US3_CTS #17 US3_RTS #16 I2C1_SDA #16 I2C1_SCL #15	
A5	PC0	BUSBY BUSAX	WTIM0_CC0 #20 WTIM0_CC1 #18 WTIM0_CC2 #16 WTIM0_CDTI0 #12 WTIM0_CDTI1 #10 WTIM0_CDTI2 #8 WTIM1_CC0 #4 WTIM1_CC1 #2 WTIM1_CC2 #0 PCNT1_S0IN #13 PCNT1_S1IN #12 PCNT2_S0IN #13 PCNT2_S1IN #12	US3_TX #18 US3_RX #17 US3_CLK #16 US3_CS #15 US3_CTS #14 US3_RTS #13 I2C1_SDA #13 I2C1_SCL #12	
A6	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE-TIM0_OUT0 #16 LE-TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D2	PF13	BUSAY BUSBX	WTIM1_CC3 #31 PCNT1_S0IN #26 PCNT1_S1IN #25 PCNT2_S0IN #26 PCNT2_S1IN #25	US2_TX #26 US2_RX #25 US2_CLK #24 US2_CS #23 US2_CTS #22 US2_RTS #21 US3_TX #26 US3_RX #25 US3_CLK #24 US3_CS #23 US3_CTS #22 US3_RTS #21 I2C1_SDA #26 I2C1_SCL #25	
D3	PF12	BUSBY BUSAX	WTIM1_CC3 #30 PCNT1_S0IN #25 PCNT1_S1IN #24 PCNT2_S0IN #25 PCNT2_S1IN #24	US2_TX #25 US2_RX #24 US2_CLK #23 US2_CS #22 US2_CTS #21 US2_RTS #20 US3_TX #25 US3_RX #24 US3_CLK #23 US3_CS #22 US3_CTS #21 US3_RTS #20 I2C1_SDA #25 I2C1_SCL #24	ETM_TD3 #0
D11	PB11	BUSCY BUSDX OPA2_P	TIM0_CC0 #6 TIM0_CC1 #5 TIM0_CC2 #4 TIM0_CDTI0 #3 TIM0_CDTI1 #2 TIM0_CDTI2 #1 TIM1_CC0 #6 TIM1_CC1 #5 TIM1_CC2 #4 TIM1_CC3 #3 WTIM0_CC0 #15 WTIM0_CC1 #13 WTIM0_CC2 #11 WTIM0_CDTI0 #7 WTIM0_CDTI1 #5 WTIM0_CDTI2 #3 LE-TIM0_OUT0 #6 LE-TIM0_OUT1 #5 PCNT0_S0IN #6 PCNT0_S1IN #5	US0_TX #6 US0_RX #5 US0_CLK #4 US0_CS #3 US0_CTS #2 US0_RTS #1 US1_TX #6 US1_RX #5 US1_CLK #4 US1_CS #3 US1_CTS #2 US1_RTS #1 US3_TX #15 US3_RX #14 US3_CLK #13 US3_CS #12 US3_CTS #11 US3_RTS #10 LEU0_TX #6 LEU0_RX #5 I2C0_SDA #6 I2C0_SCL #5	PRS_CH6 #6 PRS_CH7 #5 PRS_CH8 #4 PRS_CH9 #3 ACMP0_O #6 ACMP1_O #6
D12	PB10	OPA2_OUTALT #1 BUSDY BUSCX	WTIM0_CC0 #14 WTIM0_CC1 #12 WTIM0_CC2 #10 WTIM0_CDTI0 #6 WTIM0_CDTI1 #4 WTIM0_CDTI2 #2 PCNT1_S0IN #10 PCNT1_S1IN #9 PCNT2_S0IN #10 PCNT2_S1IN #9	US2_TX #13 US2_RX #12 US2_CLK #11 US2_CS #10 US2_CTS #9 US2_RTS #8 US3_TX #14 US3_RX #13 US3_CLK #12 US3_CS #11 US3_CTS #10 US3_RTS #9 I2C1_SDA #10 I2C1_SCL #9	

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
G13	PI0	BUSADC0Y BUSADC0X		US2_TX #5 US2_RX #4 US2_CLK #3 US2_CS #2 US2_CTS #1 US2_RTS #0	LES_ALTEX4
H1	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
H2	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE-TIM0_OUT0 #30 LE-TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
H5	VSS	Ground			
H6	VSS	Ground			
H7	VSS	Ground			
H8	VSS	Ground			
H9	VSS	Ground			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
6	PF5	BUSAY BUSBX	TIM0_CC0 #29 TIM0_CC1 #28 TIM0_CC2 #27 TIM0_CDTI0 #26 TIM0_CDTI1 #25 TIM0_CDTI2 #24 TIM1_CC0 #29 TIM1_CC1 #28 TIM1_CC2 #27 TIM1_CC3 #26 WTIM1_CC0 #29 WTIM1_CC1 #27 WTIM1_CC2 #25 WTIM1_CC3 #23 LE-TIM0_OUT0 #29 LE-TIM0_OUT1 #28 PCNT0_S0IN #29 PCNT0_S1IN #28	US0_TX #29 US0_RX #28 US0_CLK #27 US0_CS #26 US0_CTS #25 US0_RTS #24 US1_TX #29 US1_RX #28 US1_CLK #27 US1_CS #26 US1_CTS #25 US1_RTS #24 US2_TX #18 US2_RX #17 US2_CLK #16 US2_CS #15 US2_CTS #14 US2_RTS #13 LEU0_TX #29 LEU0_RX #28 I2C0_SDA #29 I2C0_SCL #28	PRS_CH0 #5 PRS_CH1 #4 PRS_CH2 #3 PRS_CH3 #2 ACMP0_O #29 ACMP1_O #29
7	PF6	BUSBY BUSAX	TIM0_CC0 #30 TIM0_CC1 #29 TIM0_CC2 #28 TIM0_CDTI0 #27 TIM0_CDTI1 #26 TIM0_CDTI2 #25 TIM1_CC0 #30 TIM1_CC1 #29 TIM1_CC2 #28 TIM1_CC3 #27 WTIM1_CC0 #30 WTIM1_CC1 #28 WTIM1_CC2 #26 WTIM1_CC3 #24 LE-TIM0_OUT0 #30 LE-TIM0_OUT1 #29 PCNT0_S0IN #30 PCNT0_S1IN #29 PCNT1_S0IN #19 PCNT1_S1IN #18	US0_TX #30 US0_RX #29 US0_CLK #28 US0_CS #27 US0_CTS #26 US0_RTS #25 US1_TX #30 US1_RX #29 US1_CLK #28 US1_CS #27 US1_CTS #26 US1_RTS #25 US2_TX #19 US2_RX #18 US2_CLK #17 US2_CS #16 US2_CTS #15 US2_RTS #14 LEU0_TX #30 LEU0_RX #29 I2C0_SDA #30 I2C0_SCL #29	CMU_CLK1 #7 PRS_CH0 #6 PRS_CH1 #5 PRS_CH2 #4 PRS_CH3 #3 ACMP0_O #30 ACMP1_O #30
8	PF7	BUSAY BUSBX	TIM0_CC0 #31 TIM0_CC1 #30 TIM0_CC2 #29 TIM0_CDTI0 #28 TIM0_CDTI1 #27 TIM0_CDTI2 #26 TIM1_CC0 #31 TIM1_CC1 #30 TIM1_CC2 #29 TIM1_CC3 #28 WTIM1_CC0 #31 WTIM1_CC1 #29 WTIM1_CC2 #27 WTIM1_CC3 #25 LE-TIM0_OUT0 #31 LE-TIM0_OUT1 #30 PCNT0_S0IN #31 PCNT0_S1IN #30 PCNT1_S0IN #20 PCNT1_S1IN #19	US0_TX #31 US0_RX #30 US0_CLK #29 US0_CS #28 US0_CTS #27 US0_RTS #26 US1_TX #31 US1_RX #30 US1_CLK #29 US1_CS #28 US1_CTS #27 US1_RTS #26 US2_TX #20 US2_RX #19 US2_CLK #18 US2_CS #17 US2_CTS #16 US2_RTS #15 LEU0_TX #31 LEU0_RX #30 I2C0_SDA #31 I2C0_SCL #30	CMU_CLKI0 #1 CMU_CLK0 #7 PRS_CH0 #7 PRS_CH1 #6 PRS_CH2 #5 PRS_CH3 #4 ACMP0_O #31 ACMP1_O #31 GPIO_EM4WU1
9	AVDD	Analog power supply .			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
23	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE-TIM0_OUT0 #22 LE-TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
24	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE-TIM0_OUT0 #23 LE-TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2
25	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE-TIM0_OUT0 #0 LE-TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
43	PC6	BUSBY BUSAX	TIM0_CC0 #11 TIM0_CC1 #10 TIM0_CC2 #9 TIM0_CDTI0 #8 TIM0_CDTI1 #7 TIM0_CDTI2 #6 TIM1_CC0 #11 TIM1_CC1 #10 TIM1_CC2 #9 TIM1_CC3 #8 WTIM0_CC0 #26 WTIM0_CC1 #24 WTIM0_CC2 #22 WTIM0_CDTI0 #18 WTIM0_CDTI1 #16 WTIM0_CDTI2 #14 WTIM1_CC0 #10 WTIM1_CC1 #8 WTIM1_CC2 #6 WTIM1_CC3 #4 LE-TIM0_OUT0 #11 LE-TIM0_OUT1 #10 PCNT0_S0IN #11 PCNT0_S1IN #10	US0_TX #11 US0_RX #10 US0_CLK #9 US0_CS #8 US0_CTS #7 US0_RTS #6 US1_TX #11 US1_RX #10 US1_CLK #9 US1_CS #8 US1_CTS #7 US1_RTS #6 LEU0_TX #11 LEU0_RX #10 I2C0_SDA #11 I2C0_SCL #10	CMU_CLK0 #2 CMU_CLKI0 #2 PRS_CH0 #8 PRS_CH9 #11 PRS_CH10 #0 PRS_CH11 #5 ACMP0_O #11 ACMP1_O #11 ETM_TCLK #3
44	PC7	BUSAY BUSBX	TIM0_CC0 #12 TIM0_CC1 #11 TIM0_CC2 #10 TIM0_CDTI0 #9 TIM0_CDTI1 #8 TIM0_CDTI2 #7 TIM1_CC0 #12 TIM1_CC1 #11 TIM1_CC2 #10 TIM1_CC3 #9 WTIM0_CC0 #27 WTIM0_CC1 #25 WTIM0_CC2 #23 WTIM0_CDTI0 #19 WTIM0_CDTI1 #17 WTIM0_CDTI2 #15 WTIM1_CC0 #11 WTIM1_CC1 #9 WTIM1_CC2 #7 WTIM1_CC3 #5 LE-TIM0_OUT0 #12 LE-TIM0_OUT1 #11 PCNT0_S0IN #12 PCNT0_S1IN #11	US0_TX #12 US0_RX #11 US0_CLK #10 US0_CS #9 US0_CTS #8 US0_RTS #7 US1_TX #12 US1_RX #11 US1_CLK #10 US1_CS #9 US1_CTS #8 US1_RTS #7 LEU0_TX #12 LEU0_RX #11 I2C0_SDA #12 I2C0_SCL #11	CMU_CLK1 #2 PRS_CH0 #9 PRS_CH9 #12 PRS_CH10 #1 PRS_CH11 #0 ACMP0_O #12 ACMP1_O #12 ETM_TD0

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
47	PC10	BUSBY BUSAX	TIM0_CC0 #15 TIM0_CC1 #14 TIM0_CC2 #13 TIM0_CDTI0 #12 TIM0_CDTI1 #11 TIM0_CDTI2 #10 TIM1_CC0 #15 TIM1_CC1 #14 TIM1_CC2 #13 TIM1_CC3 #12 WTIM0_CC0 #30 WTIM0_CC1 #28 WTIM0_CC2 #26 WTIM0_CDTI0 #22 WTIM0_CDTI1 #20 WTIM0_CDTI2 #18 WTIM1_CC0 #14 WTIM1_CC1 #12 WTIM1_CC2 #10 WTIM1_CC3 #8 LE-TIM0_OUT0 #15 LE-TIM0_OUT1 #14 PCNT0_S0IN #15 PCNT0_S1IN #14 PCNT2_S0IN #19 PCNT2_S1IN #18	US0_TX #15 US0_RX #14 US0_CLK #13 US0_CS #12 US0_CTS #11 US0_RTS #10 US1_TX #15 US1_RX #14 US1_CLK #13 US1_CS #12 US1_CTS #11 US1_RTS #10 LEU0_TX #15 LEU0_RX #14 I2C0_SDA #15 I2C0_SCL #14 I2C1_SDA #19 I2C1_SCL #18	CMU_CLK1 #3 PRS_CH0 #12 PRS_CH9 #15 PRS_CH10 #4 PRS_CH11 #3 ACMP0_O #15 ACMP1_O #15 ETM_TD3 GPIO_EM4WU12
48	PC11	BUSAY BUSBX	TIM0_CC0 #16 TIM0_CC1 #15 TIM0_CC2 #14 TIM0_CDTI0 #13 TIM0_CDTI1 #12 TIM0_CDTI2 #11 TIM1_CC0 #16 TIM1_CC1 #15 TIM1_CC2 #14 TIM1_CC3 #13 WTIM0_CC0 #31 WTIM0_CC1 #29 WTIM0_CC2 #27 WTIM0_CDTI0 #23 WTIM0_CDTI1 #21 WTIM0_CDTI2 #19 WTIM1_CC0 #15 WTIM1_CC1 #13 WTIM1_CC2 #11 WTIM1_CC3 #9 LE-TIM0_OUT0 #16 LE-TIM0_OUT1 #15 PCNT0_S0IN #16 PCNT0_S1IN #15 PCNT2_S0IN #20 PCNT2_S1IN #19	US0_TX #16 US0_RX #15 US0_CLK #14 US0_CS #13 US0_CTS #12 US0_RTS #11 US1_TX #16 US1_RX #15 US1_CLK #14 US1_CS #13 US1_CTS #12 US1_RTS #11 LEU0_TX #16 LEU0_RX #15 I2C0_SDA #16 I2C0_SCL #15 I2C1_SDA #20 I2C1_SCL #19	CMU_CLK0 #3 PRS_CH0 #13 PRS_CH9 #16 PRS_CH10 #5 PRS_CH11 #4 ACMP0_O #16 ACMP1_O #16 DBG_SWO #3

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
DBG_SWCLKTCK	0: PF0								Debug-interface Serial Wire clock input and JTAG Test Clock. Note that this function is enabled to the pin out of reset, and has a built-in pull down.
DBG_SWDIOTMS	0: PF1								Debug-interface Serial Wire data input / output and JTAG Test Mode Select. Note that this function is enabled to the pin out of reset, and has a built-in pull up.
DBG_SWO	0: PF2 1: PB13 2: PD15 3: PC11								Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
DBG_TDI	0: PF3								Debug-interface JTAG Test Data In. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_TDO	0: PF2								Debug-interface JTAG Test Data Out. Note that this function is enabled to pin out of reset.
ETM_TCLK	0: PF8 1: PA5 2: PI2 3: PC6								Embedded Trace Module ETM clock .
ETM_TD0	0: PF9 1: PA6 2: PI3 3: PC7								Embedded Trace Module ETM data 0.
ETM_TD1	0: PF10 1: PA7 2: PB6 3: PC8								Embedded Trace Module ETM data 1.

7. BGA125 Package Specifications

7.1 BGA125 Package Dimensions

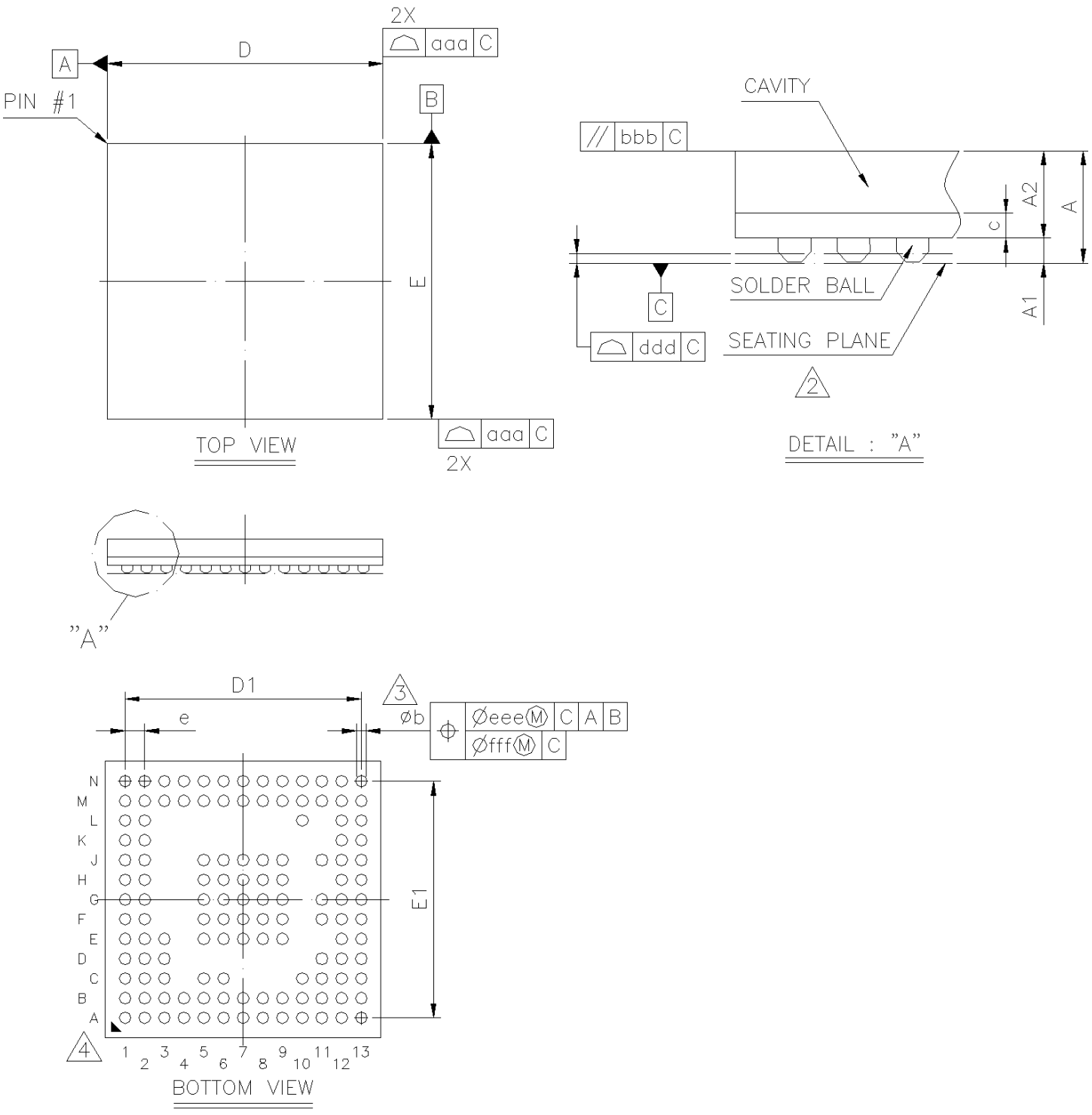

Figure 7.1. BGA125 Package Drawing

7.2 BGA125 PCB Land Pattern

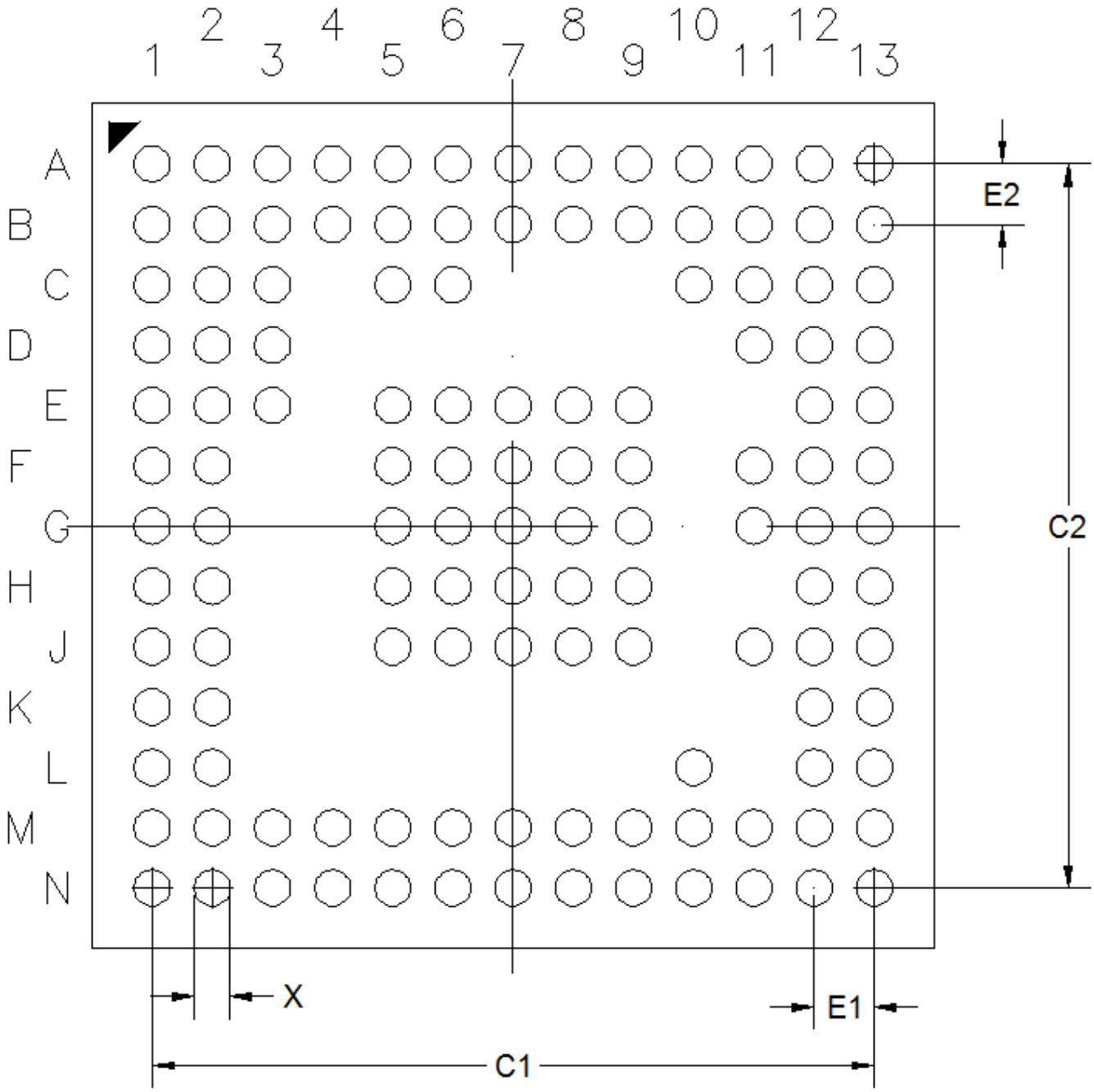

Figure 7.2. BGA125 PCB Land Pattern Drawing

Table 7.2. BGA125 PCB Land Pattern Dimensions

Dimension	Min	Nom	Max
X		0.25	
C1		6.00	
C2		6.00	
E1		0.5	
E2		0.5	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
6. The stencil thickness should be 0.125 mm (5 mils).
7. The ratio of stencil aperture to land pad size should be 1:1.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. QFN48 Package Specifications

8.1 QFN48 Package Dimensions

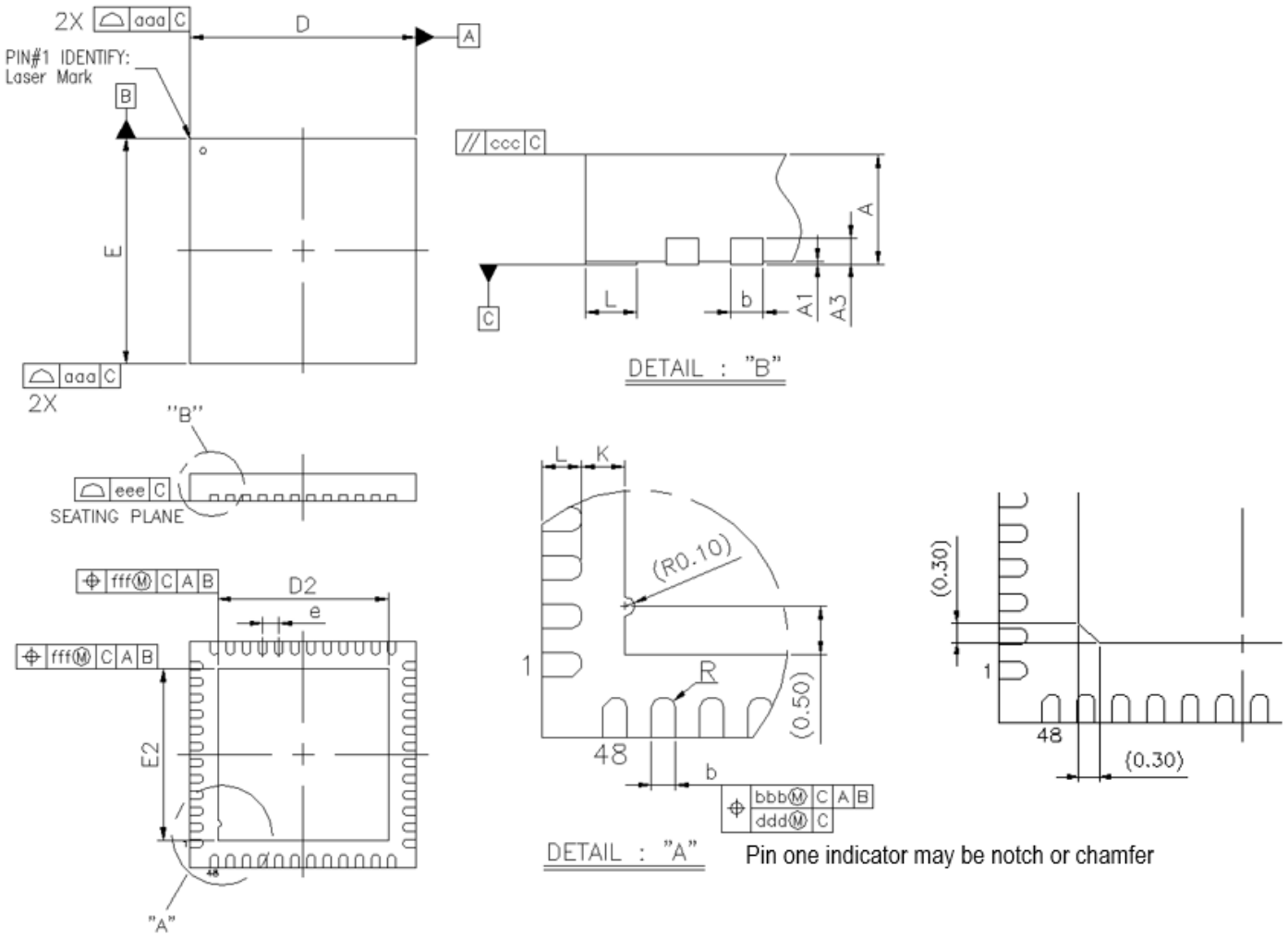

Figure 8.1. QFN48 Package Drawing