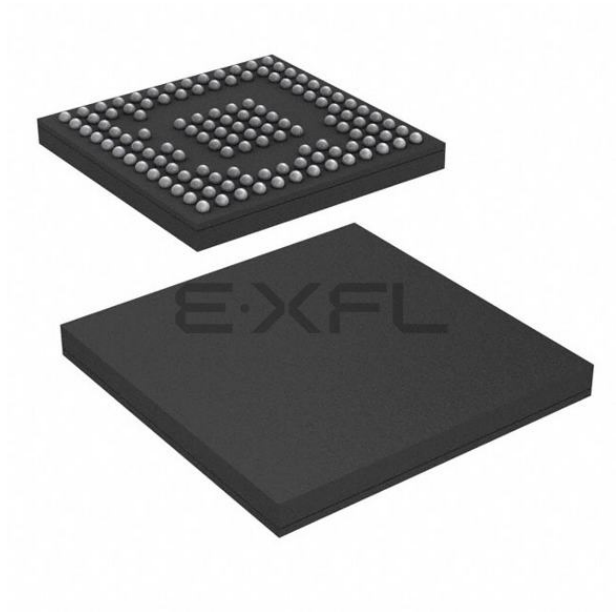
Silicon Labs - EFM32JG12B500F1024IL125-CR Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	65
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	125-VFBGA
Supplier Device Package	125-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg12b500f1024il125-cr

1. Feature List

The EFM32JG12 highlighted features are listed below.

- **ARM Cortex-M3 CPU platform**
  - High performance 32-bit processor @ up to 40 MHz
  - Memory Protection Unit
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 64 µA/MHz in Active Mode (EM0)
  - 2.1 µA EM2 Deep Sleep current (256 kB RAM retention and RTCC running from LFXO)
  - 1.5 µA EM2 Deep Sleep current (16 kB RAM retention and RTCC running from LFRCO)
  - 1.81 µA EM3 Stop current (State and 256 kB RAM retention, CRYOTIMER running from ULFRCO)
  - 0.39 µA EM4H Hibernate Mode (128 byte RAM retention)
- **Up to 1024 kB flash program memory**
  - Dual-bank with read-while-write support
- **Up to 256 kB RAM data memory**
- **Up to 65 General Purpose I/O Pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - Asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **Hardware Cryptography**
  - AES 128/256-bit keys
  - ECC B/K163, B/K233, P192, P224, P256
  - SHA-1 and SHA-2 (SHA-224 and SHA-256)
  - True random number generator (TRNG)
- **Security Management Unit (SMU)**
  - Fine-grained access control for on-chip peripherals
- **Timers/Counters**
  - 2× 16-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 2× 32-bit Timer/Counter
    - 3 + 4 Compare/Capture/PWM channels
  - 1× 32-bit Real Time Counter and Calendar
  - 1× 32-bit Ultra Low Energy CRYOTIMER for periodic wake-up from any Energy Mode
  - 16-bit Low Energy Timer for waveform generation
  - 3× 16-bit Pulse Counter with asynchronous operation
  - 2× Watchdog Timer with dedicated RC oscillator
- **8 Channel DMA Controller**
- **12 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Communication Interfaces**
  - 4× Universal Synchronous/Asynchronous Receiver/ Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S/LIN
    - Triple buffered full/half-duplex operation with flow control
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - 2× I^2C Interface with SMBus support
    - Address recognition in EM3 Stop Mode
- **Ultra Low-Power Precision Analog Peripherals**
  - 12-bit 1 Msps SAR Analog to Digital Converter (ADC)
  - 2× Analog Comparator (ACMP)
  - 2× 12-bit 500 ksps Digital to Analog Converter (VDAC)
  - 3× Operational Amplifier (OPAMP)
  - Digital to Analog Current Converter (IDAC)
  - Multi-channel Capacitive Sense Interface (CSEN)
  - Up to 54 pins connected to analog channels (APORT) shared between analog peripherals
- **Low-Energy Sensor Interface (LESENSE)**
  - Autonomous sensor monitoring in deep sleep mode
  - Wide range of supported sensors, including LC sensors and capacitive touch switches
  - Up to 16 channels
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **Debug Interface**
  - 2-pin Serial Wire Debug interface
  - 1-pin Serial Wire Viewer
  - JTAG (programming only)
  - Embedded Trace Macrocell (ETM)
- **Wide Operating Range**
  - 1.8 V to 3.8 V single power supply
  - Integrated DC-DC, down to 1.8 V output with up to 200 mA load current for system
  - Standard (-40 °C to 85 °C T_{AMB}) and Extended (-40 °C to 125 °C T_J) temperature grades available
- **Packages**
  - 7 mm × 7 mm QFN48
  - 7 mm × 7 mm BGA125
- **Pre-Programmed UART Bootloader**
- **Full Software Support**
  - CMSIS register definitions
  - Low-power Hardware Abstraction Layer (HAL)
  - Portable software components
  - Third-party middleware
  - Free and available example code

3.5.4 Low Energy Timer (LETIMER)

The unique LETIMER is a 16-bit timer that is available in energy mode EM2 Deep Sleep in addition to EM1 Sleep and EM0 Active. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Real Time Counter and Calendar (RTCC), and can be configured to start counting on compare matches from the RTCC.

3.5.5 Ultra Low Power Wake-up Timer (CRYOTIMER)

The CRYOTIMER is a 32-bit counter that is capable of running in all energy modes. It can be clocked by either the 32.768 kHz crystal oscillator (LFXO), the 32.768 kHz RC oscillator (LFRCO), or the 1 kHz RC oscillator (ULFRCO). It can provide periodic Wakeup events and PRS signals which can be used to wake up peripherals from any energy mode. The CRYOTIMER provides a wide range of interrupt periods, facilitating flexible ultra-low energy operation.

3.5.6 Pulse Counter (PCNT)

The Pulse Counter (PCNT) peripheral can be used for counting pulses on a single input or to decode quadrature encoded inputs. The clock for PCNT is selectable from either an external source on pin PCTNn_S0IN or from an internal timing reference, selectable from among any of the internal oscillators, except the AUXHFRCO. The module may operate in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop.

3.5.7 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by PRS.

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™ provides two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud. The LEUART includes all necessary hardware to make asynchronous serial communication possible with a minimum of software intervention and energy consumption.

3.6.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as both a master and a slave and supports multi-master buses. Standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of slave addresses is provided in active and low energy modes.

3.6.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality can be applied by the PRS. The PRS allows peripheral to act autonomously without waking the MCU core, saving power.

4.1.7 Brown Out Detector (BOD)

Table 4.9. Brown Out Detector (BOD)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DVDD BOD threshold	$V_{DVDDBOD}$	DVDD rising	—	—	TBD	V
		DVDD falling (EM0/EM1)	TBD	—	—	V
		DVDD falling (EM2/EM3)	TBD	—	—	V
DVDD BOD hysteresis	$V_{DVDDBOD\_HYST}$		—	18	—	mV
DVDD BOD response time	$t_{DVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
AVDD BOD threshold	$V_{AVDDBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling (EM0/EM1)	TBD	—	—	V
		AVDD falling (EM2/EM3)	TBD	—	—	V
AVDD BOD hysteresis	$V_{AVDDBOD\_HYST}$		—	20	—	mV
AVDD BOD response time	$t_{AVDDBOD\_DELAY}$	Supply drops at 0.1V/µs rate	—	2.4	—	µs
EM4 BOD threshold	$V_{EM4DBOD}$	AVDD rising	—	—	TBD	V
		AVDD falling	TBD	—	—	V
EM4 BOD hysteresis	V_{EM4BOD_HYST}		—	25	—	mV
EM4 BOD response time	t_{EM4BOD_DELAY}	Supply drops at 0.1V/µs rate	—	300	—	µs

4.1.11 Voltage Monitor (VMON)

Table 4.18. Voltage Monitor (VMON)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply current (including I_SENSE)	I_{VMON}	In EM0 or EM1, 1 supply monitored	—	6.3	TBD	µA
		In EM0 or EM1, 4 supplies monitored	—	12.5	TBD	µA
		In EM2, EM3 or EM4, 1 supply monitored and above threshol	—	62	—	nA
		In EM2, EM3 or EM4, 1 supply monitored and below threshold	—	62	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all above threshold	—	99	—	nA
		In EM2, EM3 or EM4, 4 supplies monitored and all below threshold	—	99	—	nA
Loading of monitored supply	I_{SENSE}	In EM0 or EM1	—	2	—	µA
		In EM2, EM3 or EM4	—	2	—	nA
Threshold range	V_{VMON_RANGE}		1.62	—	3.4	V
Threshold step size	N_{VMON_STESP}	Coarse	—	200	—	mV
		Fine	—	20	—	mV
Response time	t_{VMON_RES}	Supply drops at 1V/µs rate	—	460	—	ns
Hysteresis	V_{VMON_HYST}		—	26	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis (V_{CM} = 1.25 V, BIASPROG[4] = 0x10, FULLBIAS[4] = 1)	$V_{ACMPHYST}$	HYSTSEL[5] = HYST0	TBD	—	TBD	mV
		HYSTSEL[5] = HYST1	TBD	18	TBD	mV
		HYSTSEL[5] = HYST2	TBD	32	TBD	mV
		HYSTSEL[5] = HYST3	TBD	44	TBD	mV
		HYSTSEL[5] = HYST4	TBD	55	TBD	mV
		HYSTSEL[5] = HYST5	TBD	65	TBD	mV
		HYSTSEL[5] = HYST6	TBD	77	TBD	mV
		HYSTSEL[5] = HYST7	TBD	86	TBD	mV
		HYSTSEL[5] = HYST8	TBD	—	TBD	mV
		HYSTSEL[5] = HYST9	TBD	-18	TBD	mV
		HYSTSEL[5] = HYST10	TBD	-32	TBD	mV
		HYSTSEL[5] = HYST11	TBD	-43	TBD	mV
		HYSTSEL[5] = HYST12	TBD	-54	TBD	mV
		HYSTSEL[5] = HYST13	TBD	-64	TBD	mV
		HYSTSEL[5] = HYST14	TBD	-74	TBD	mV
		HYSTSEL[5] = HYST15	TBD	-85	TBD	mV
Comparator delay[3]	$t_{ACMPDELAY}$	BIASPROG[4] = 1, FULLBIAS[4] = 0	—	30	—	µs
		BIASPROG[4] = 0x10, FULLBIAS[4] = 0	—	3.7	—	µs
		BIASPROG[4] = 0x02, FULLBIAS[4] = 1	—	360	—	ns
		BIASPROG[4] = 0x20, FULLBIAS[4] = 1	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	BIASPROG[4] =0x10, FULLBIAS[4] = 1	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	CSRESSEL[6] = 0	—	inf	—	kΩ
		CSRESSEL[6] = 1	—	15	—	kΩ
		CSRESSEL[6] = 2	—	27	—	kΩ
		CSRESSEL[6] = 3	—	39	—	kΩ
		CSRESSEL[6] = 4	—	51	—	kΩ
		CSRESSEL[6] = 5	—	102	—	kΩ
		CSRESSEL[6] = 6	—	164	—	kΩ
		CSRESSEL[6] = 7	—	239	—	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	$SNDR_{DAC}$	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave). Noise band limited to 22 kHz.	$SNDR_{DAC\_BAND}$	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity[3]	DNL_{DAC}		TBD	—	TBD	LSB
Intergral non-linearity	INL_{DAC}		TBD	—	TBD	LSB
Offset error[5]	V_{OFFSET}	T_J = 25 °C	TBD	—	TBD	mV
		-40 °C ≤ T_J ≤ 85 °C	TBD	—	TBD	mV
Gain error[5]	V_{GAIN}	T_J = 25 °C	TBD	—	TBD	%
		-40 °C ≤ T_J ≤ 85 °C	TBD	—	TBD	%
External load capactiance, OUTSCALE=0	C_{LOAD}		—	—	75	pF

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HFPERCLK is dependent on HFPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as 20 * $\log_{10}(\Delta VDD / \Delta V_{OUT})$, VDAC output at 90% of full scale

4.1.21 USART SPI

SPI Master Timing

Table 4.30. SPI Master Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period [1] [3] [2]	t_{SCLK}		2 * $t_{HFPERCLK}$	—	—	ns
CS to MOSI [1] [3]	t_{CS_MO}		0	—	13.3	ns
SCLK to MOSI [1] [3]	t_{SCLK_MO}		0	—	8	ns
MISO setup time [1] [3]	t_{SU_MI}	IOVDD = 1.62 V	90	—	—	ns
		IOVDD = 3.0 V	40	—	—	ns
MISO hold time [1] [3]	t_{H_MI}		10	—	—	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. $t_{HFPERCLK}$ is one period of the selected HFPERCLK.
3. Measurement done with 8 pF output loading at 10% and 90% of V_{DD} (figure shows 50% of V_{DD}).

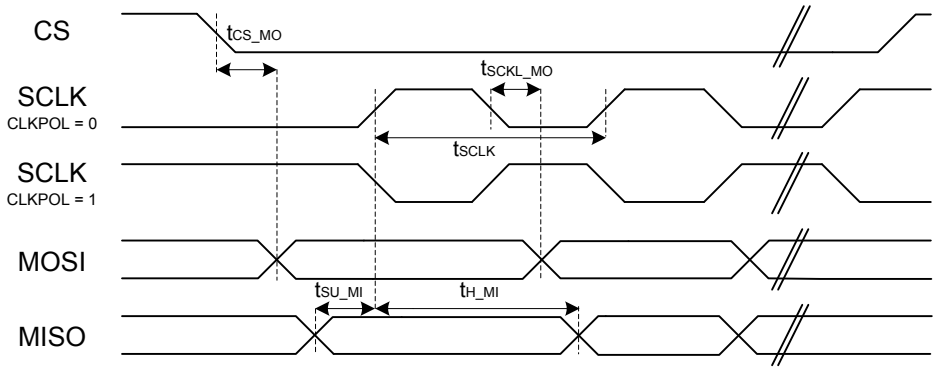


Figure 4.1. SPI Master Timing Diagram

6. Pin Definitions

6.1 EFM32JG12B5xx in BGA125 Device Pinout

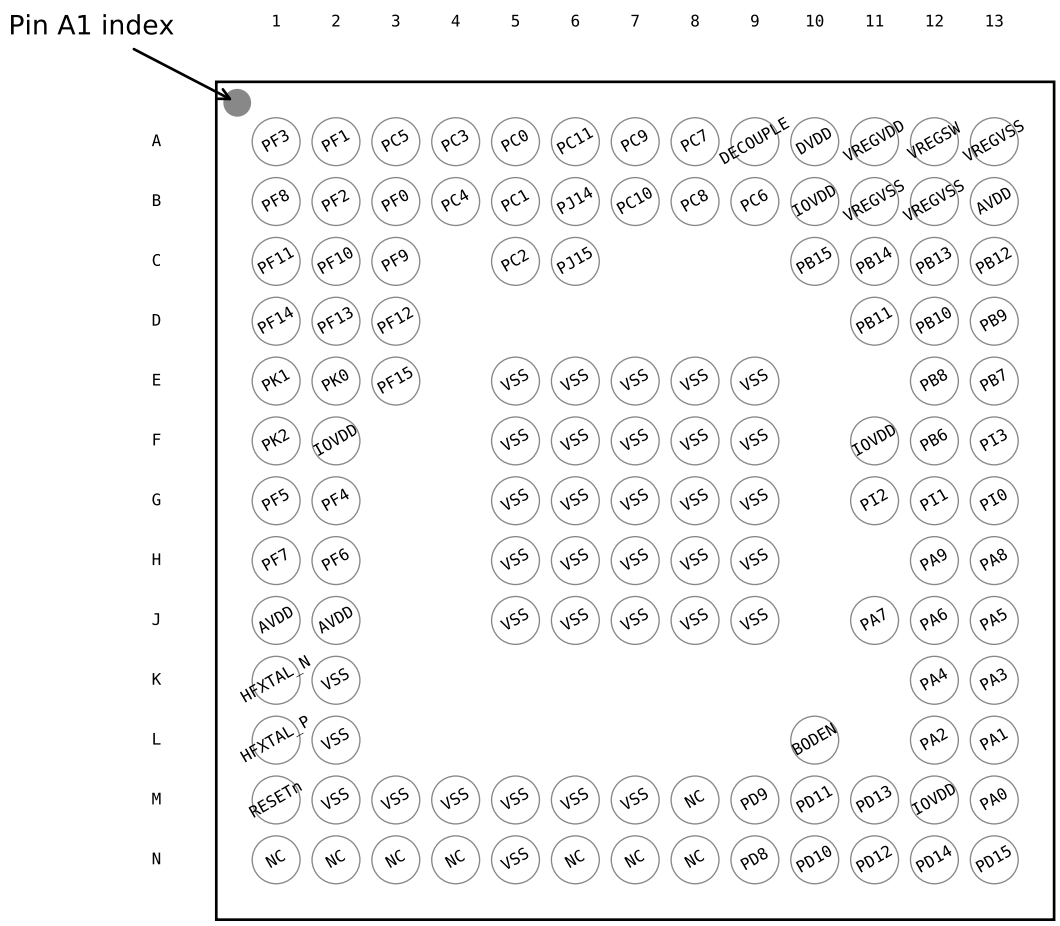


Figure 6.1. EFM32JG12B5xx in BGA125 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
N9	PD8	BUSDY BUSCX	WTIM0_CC1 #30 WTIM0_CC2 #28 WTIM0_CDTI0 #24 WTIM0_CDTI1 #22 WTIM0_CDTI2 #20 WTIM1_CC0 #16 WTIM1_CC1 #14 WTIM1_CC2 #12 WTIM1_CC3 #10	US3_TX #0 US3_RX #31 US3_CLK #30 US3_CS #29 US3_CTS #28 US3_RTS #27	LES_CH0
N10	PD10	BUSDY BUSCX	TIM0_CC0 #18 TIM0_CC1 #17 TIM0_CC2 #16 TIM0_CDTI0 #15 TIM0_CDTI1 #14 TIM0_CDTI2 #13 TIM1_CC0 #18 TIM1_CC1 #17 TIM1_CC2 #16 TIM1_CC3 #15 WTIM0_CC2 #30 WTIM0_CDTI0 #26 WTIM0_CDTI1 #24 WTIM0_CDTI2 #22 WTIM1_CC0 #18 WTIM1_CC1 #16 WTIM1_CC2 #14 WTIM1_CC3 #12 LE-TIM0_OUT0 #18 LE-TIM0_OUT1 #17 PCNT0_S0IN #18 PCNT0_S1IN #17	US0_TX #18 US0_RX #17 US0_CLK #16 US0_CS #15 US0_CTS #14 US0_RTS #13 US1_TX #18 US1_RX #17 US1_CLK #16 US1_CS #15 US1_CTS #14 US1_RTS #13 US3_TX #2 US3_RX #1 US3_CLK #0 US3_CS #31 US3_CTS #30 US3_RTS #29 LEU0_TX #18 LEU0_RX #17 I2C0_SDA #18 I2C0_SCL #17	CMU_CLK1 #4 PRS_CH3 #9 PRS_CH4 #1 PRS_CH5 #0 PRS_CH6 #12 ACMP0_O #18 ACMP1_O #18 LES_CH2
N11	PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LE-TIM0_OUT0 #20 LE-TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
N12	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE-TIM0_OUT0 #22 LE-TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
N13	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE-TIM0_OUT0 #23 LE-TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2

6.2 EFM32JG12B5xx in QFN48 Device Pinout

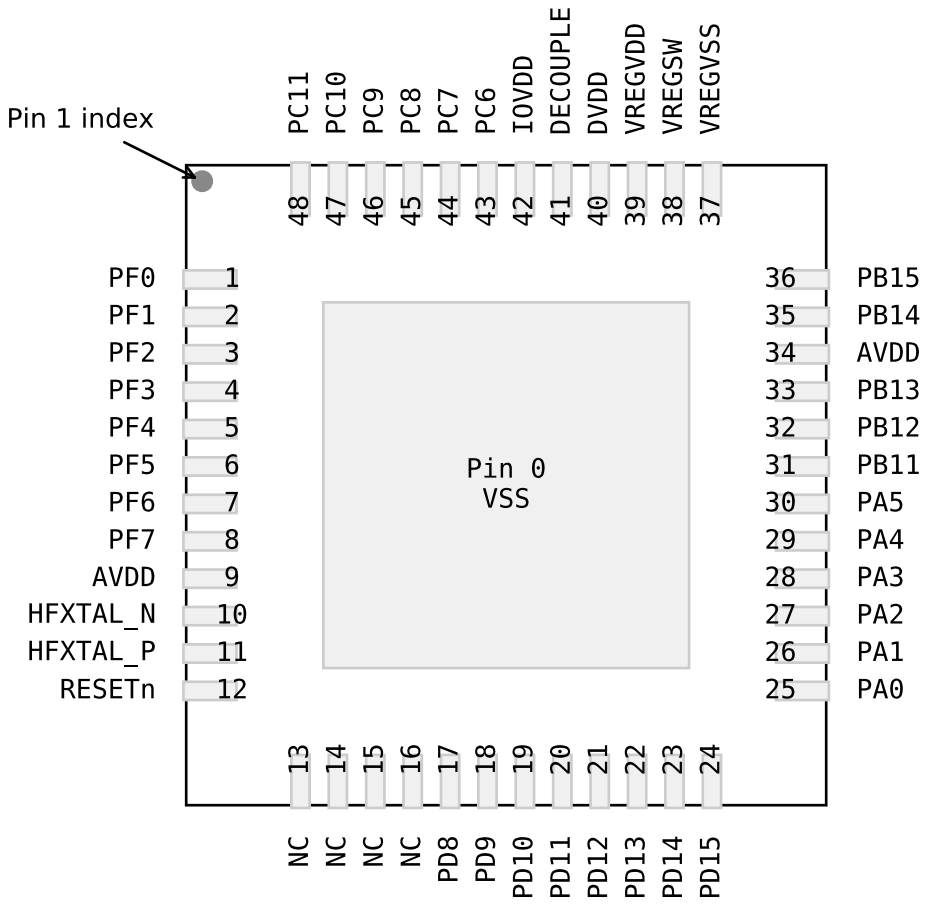


Figure 6.2. EFM32JG12B5xx in QFN48 Device Pinout

Table 6.3. EFM32JG12B5xx in QFN48 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground			
1	PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 WTIM1_CC0 #24 WTIM1_CC1 #22 WTIM1_CC2 #20 WTIM1_CC3 #18 LE-TIM0_OUT0 #24 LE-TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE-TIM0_OUT0 #25 LE-TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
21	PD12	VDAC0_OUT1ALT / OPA1_OUTALT #0 BUSDY BUSCX	TIM0_CC0 #20 TIM0_CC1 #19 TIM0_CC2 #18 TIM0_CDTI0 #17 TIM0_CDTI1 #16 TIM0_CDTI2 #15 TIM1_CC0 #20 TIM1_CC1 #19 TIM1_CC2 #18 TIM1_CC3 #17 WTIM0_CDTI0 #28 WTIM0_CDTI1 #26 WTIM0_CDTI2 #24 WTIM1_CC0 #20 WTIM1_CC1 #18 WTIM1_CC2 #16 WTIM1_CC3 #14 LE-TIM0_OUT0 #20 LE-TIM0_OUT1 #19 PCNT0_S0IN #20 PCNT0_S1IN #19	US0_TX #20 US0_RX #19 US0_CLK #18 US0_CS #17 US0_CTS #16 US0_RTS #15 US1_TX #20 US1_RX #19 US1_CLK #18 US1_CS #17 US1_CTS #16 US1_RTS #15 US3_TX #4 US3_RX #3 US3_CLK #2 US3_CS #1 US3_CTS #0 US3_RTS #31 LEU0_TX #20 LEU0_RX #19 I2C0_SDA #20 I2C0_SCL #19	PRS_CH3 #11 PRS_CH4 #3 PRS_CH5 #2 PRS_CH6 #14 ACMP0_O #20 ACMP1_O #20 LES_CH4
22	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE-TIM0_OUT0 #21 LE-TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5

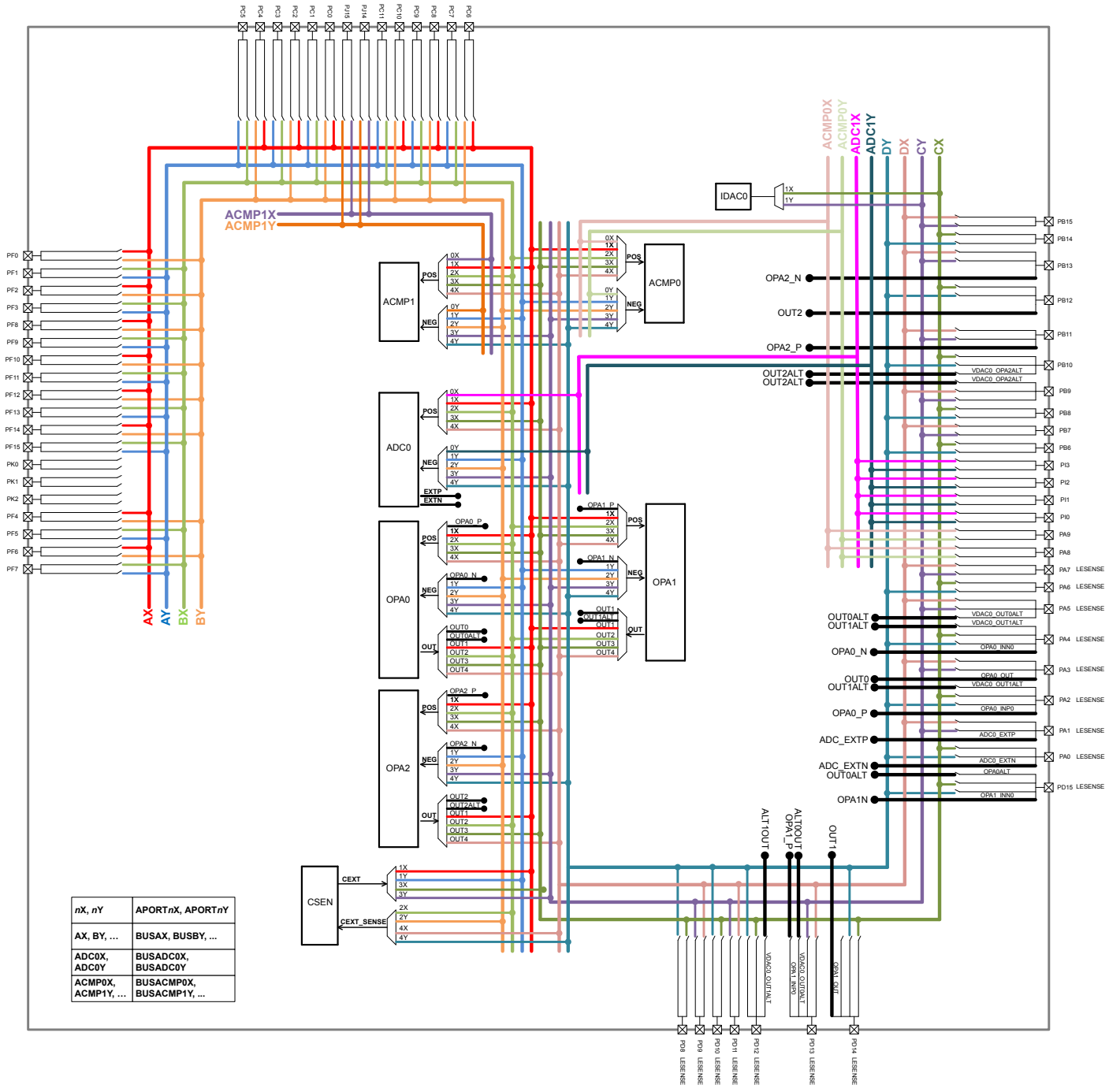
Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
32	PB12	BUSDY BUSCX OPA2_OUT	TIM0_CC0 #7 TIM0_CC1 #6 TIM0_CC2 #5 TIM0_CDTI0 #4 TIM0_CDTI1 #3 TIM0_CDTI2 #2 TIM1_CC0 #7 TIM1_CC1 #6 TIM1_CC2 #5 TIM1_CC3 #4 WTIM0_CC0 #16 WTIM0_CC1 #14 WTIM0_CC2 #12 WTIM0_CDTI0 #8 WTIM0_CDTI1 #6 WTIM0_CDTI2 #4 WTIM1_CC0 #0 LE-TIM0_OUT0 #7 LE-TIM0_OUT1 #6 PCNT0_S0IN #7 PCNT0_S1IN #6	US0_TX #7 US0_RX #6 US0_CLK #5 US0_CS #4 US0_CTS #3 US0_RTS #2 US1_TX #7 US1_RX #6 US1_CLK #5 US1_CS #4 US1_CTS #3 US1_RTS #2 LEU0_TX #7 LEU0_RX #6 I2C0_SDA #7 I2C0_SCL #6	PRS_CH6 #7 PRS_CH7 #6 PRS_CH8 #5 PRS_CH9 #4 ACMP0_O #7 ACMP1_O #7
33	PB13	BUSCY BUSDX OPA2_N	TIM0_CC0 #8 TIM0_CC1 #7 TIM0_CC2 #6 TIM0_CDTI0 #5 TIM0_CDTI1 #4 TIM0_CDTI2 #3 TIM1_CC0 #8 TIM1_CC1 #7 TIM1_CC2 #6 TIM1_CC3 #5 WTIM0_CC0 #17 WTIM0_CC1 #15 WTIM0_CC2 #13 WTIM0_CDTI0 #9 WTIM0_CDTI1 #7 WTIM0_CDTI2 #5 WTIM1_CC0 #1 LE-TIM0_OUT0 #8 LE-TIM0_OUT1 #7 PCNT0_S0IN #8 PCNT0_S1IN #7	US0_TX #8 US0_RX #7 US0_CLK #6 US0_CS #5 US0_CTS #4 US0_RTS #3 US1_TX #8 US1_RX #7 US1_CLK #6 US1_CS #5 US1_CTS #4 US1_RTS #3 LEU0_TX #8 LEU0_RX #7 I2C0_SDA #8 I2C0_SCL #7	CMU_CLKI0 #0 PRS_CH6 #8 PRS_CH7 #7 PRS_CH8 #6 PRS_CH9 #5 ACMP0_O #8 ACMP1_O #8 DBG_SWO #1 GPIO_EM4WU9
34	AVDD	Analog power supply .			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
35	PB14	BUSDY BUSCX LFXTAL_N	TIM0_CC0 #9 TIM0_CC1 #8 TIM0_CC2 #7 TIM0_CDTI0 #6 TIM0_CDTI1 #5 TIM0_CDTI2 #4 TIM1_CC0 #9 TIM1_CC1 #8 TIM1_CC2 #7 TIM1_CC3 #6 WTIM0_CC0 #18 WTIM0_CC1 #16 WTIM0_CC2 #14 WTIM0_CDTI0 #10 WTIM0_CDTI1 #8 WTIM0_CDTI2 #6 WTIM1_CC0 #2 WTIM1_CC1 #0 LE-TIM0_OUT0 #9 LE-TIM0_OUT1 #8 PCNT0_S0IN #9 PCNT0_S1IN #8	US0_TX #9 US0_RX #8 US0_CLK #7 US0_CS #6 US0_CTS #5 US0_RTS #4 US1_TX #9 US1_RX #8 US1_CLK #7 US1_CS #6 US1_CTS #5 US1_RTS #4 LEU0_TX #9 LEU0_RX #8 I2C0_SDA #9 I2C0_SCL #8	CMU_CLK1 #1 PRS_CH6 #9 PRS_CH7 #8 PRS_CH8 #7 PRS_CH9 #6 ACMP0_O #9 ACMP1_O #9
36	PB15	BUSCY BUSDX LFXTAL_P	TIM0_CC0 #10 TIM0_CC1 #9 TIM0_CC2 #8 TIM0_CDTI0 #7 TIM0_CDTI1 #6 TIM0_CDTI2 #5 TIM1_CC0 #10 TIM1_CC1 #9 TIM1_CC2 #8 TIM1_CC3 #7 WTIM0_CC0 #19 WTIM0_CC1 #17 WTIM0_CC2 #15 WTIM0_CDTI0 #11 WTIM0_CDTI1 #9 WTIM0_CDTI2 #7 WTIM1_CC0 #3 WTIM1_CC1 #1 LE-TIM0_OUT0 #10 LE-TIM0_OUT1 #9 PCNT0_S0IN #10 PCNT0_S1IN #9	US0_TX #10 US0_RX #9 US0_CLK #8 US0_CS #7 US0_CTS #6 US0_RTS #5 US1_TX #10 US1_RX #9 US1_CLK #8 US1_CS #7 US1_CTS #6 US1_RTS #5 LEU0_TX #10 LEU0_RX #9 I2C0_SDA #10 I2C0_SCL #9	CMU_CLK0 #1 PRS_CH6 #10 PRS_CH7 #9 PRS_CH8 #8 PRS_CH9 #7 ACMP0_O #10 ACMP1_O #10
37	VREGVSS	Voltage regulator VSS			
38	VREGSW	DCDC regulator switching node			
39	VREGVDD	Voltage regulator VDD input			
40	DVDD	Digital power supply .			
41	DECOUPLE	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.			
42	IOVDD	Digital IO power supply .			

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
WTIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PA6 7: PA7	8: PA8 9: PA9 10: PB6 11: PB7	12: PB8 13: PB9 14: PB10 15: PB11	16: PB12 17: PB13 18: PB14 19: PB15	20: PC0 21: PC1 22: PC2 23: PC3	24: PC4 25: PC5 26: PC6 27: PC7	28: PC8 29: PC9 30: PC10 31: PC11	Wide timer 0 Capture Compare input / output channel 0.
WTIM0_CC1	0: PA2 1: PA3 2: PA4 3: PA5	4: PA6 5: PA7 6: PA8 7: PA9	8: PB6 9: PB7 10: PB8 11: PB9	12: PB10 13: PB11 14: PB12 15: PB13	16: PB14 17: PB15 18: PC0 19: PC1	20: PC2 21: PC3 22: PC4 23: PC5	24: PC6 25: PC7 26: PC8 27: PC9	28: PC10 29: PC11 30: PD8 31: PD9	Wide timer 0 Capture Compare input / output channel 1.
WTIM0_CC2	0: PA4 1: PA5 2: PA6 3: PA7	4: PA8 5: PA9 6: PB6 7: PB7	8: PB8 9: PB9 10: PB10 11: PB11	12: PB12 13: PB13 14: PB14 15: PB15	16: PC0 17: PC1 18: PC2 19: PC3	20: PC4 21: PC5 22: PC6 23: PC7	24: PC8 25: PC9 26: PC10 27: PC11	28: PD8 29: PD9 30: PD10 31: PD11	Wide timer 0 Capture Compare input / output channel 2.
WTIM0_CDTI0	0: PA8 1: PA9 2: PB6 3: PB7	4: PB8 5: PB9 6: PB10 7: PB11	8: PB12 9: PB13 10: PB14 11: PB15	12: PC0 13: PC1 14: PC2 15: PC3	16: PC4 17: PC5 18: PC6 19: PC7	20: PC8 21: PC9 22: PC10 23: PC11	24: PD8 25: PD9 26: PD10 27: PD11	28: PD12 29: PD13 30: PD14 31: PD15	Wide timer 0 Complimentary Dead Time Insertion channel 0.
WTIM0_CDTI1	0: PB6 1: PB7 2: PB8 3: PB9	4: PB10 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC0 11: PC1	12: PC2 13: PC3 14: PC4 15: PC5	16: PC6 17: PC7 18: PC8 19: PC9	20: PC10 21: PC11 22: PD8 23: PD9	24: PD10 25: PD11 26: PD12 27: PD13	28: PD14 29: PD15 30: PF0 31: PF1	Wide timer 0 Complimentary Dead Time Insertion channel 1.
WTIM0_CDTI2	0: PB8 1: PB9 2: PB10 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC0 9: PC1 10: PC2 11: PC3	12: PC4 13: PC5 14: PC6 15: PC7	16: PC8 17: PC9 18: PC10 19: PC11	20: PD8 21: PD9 22: PD10 23: PD11	24: PD12 25: PD13 26: PD14 27: PD15	28: PF0 29: PF1 30: PF2 31: PF3	Wide timer 0 Complimentary Dead Time Insertion channel 2.
WTIM1_CC0	0: PB12 1: PB13 2: PB14 3: PB15	4: PC0 5: PC1 6: PC2 7: PC3	8: PC4 9: PC5 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD8 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Wide timer 1 Capture Compare input / output channel 0.
WTIM1_CC1	0: PB14 1: PB15 2: PC0 3: PC1	4: PC2 5: PC3 6: PC4 7: PC5	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD8 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PF8 31: PF9	Wide timer 1 Capture Compare input / output channel 1.
WTIM1_CC2	0: PC0 1: PC1 2: PC2 3: PC3	4: PC4 5: PC5 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD8 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PF8 29: PF9 30: PF10 31: PF11	Wide timer 1 Capture Compare input / output channel 2.
WTIM1_CC3	0: PC2 1: PC3 2: PC4 3: PC5	4: PC6 5: PC7 6: PC8 7: PC9	8: PC10 9: PC11 10: PD8 11: PD9	12: PD10 13: PD11 14: PD12 15: PD13	16: PD14 17: PD15 18: PF0 19: PF1	20: PF2 21: PF3 22: PF4 23: PF5	24: PF6 25: PF7 26: PF8 27: PF9	28: PF10 29: PF11 30: PF12 31: PF13	Wide timer 1 Capture Compare input / output channel 3.

6.4 Analog Port (APORT) Client Maps

The Analog Port (APORT) is an infrastructure used to connect chip pins with on-chip analog clients such as analog comparators, ADCs, DACs, etc. The APORT consists of a set of shared buses, switches, and control logic needed to configurably implement the signal routing. Figure 6.3 APORT Connection Diagram on page 111 Shows the APORT routing for this device family. A complete description of APORT functionality can be found in the Reference Manual.



nX, *nY*	APORT*nX*, APORT*nY*
AX, BY, ...	BUSAX, BUSBY, ...
ADC0X, ADC0Y	BUSADC0X, BUSADC0Y
ACMP0X, ACMP1Y, ...	BUSACMP0X, BUSACMP1Y, ...

Figure 6.3. APORT Connection Diagram

Client maps for each analog circuit using the APORT are shown in the following tables. The maps are organized by bus, and show the peripheral's port connection, the shared bus, and the connection from specific bus channel numbers to GPIO pins.

In general, enumerations for the pin selection field in an analog peripheral's register can be determined by finding the desired pin connection in the table and then combining the value in the Port column (APORT__), and the channel identifier (CH__). For example, if pin

Table 6.11. VDAC0 / OPA Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
OPA0_N																																	
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT2Y	BUSBY		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10		PC8		PC6		PC4		PC2		PC0
APORT3Y	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	
APORT4Y	BUSDY		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
OPA0_P																																	
APORT1X	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0					PC10		PC8		PC6		PC4		PC2		PC0	
APORT2X	BUSBX	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11		PC9		PC7		PC5		PC3		PC1	
APORT3X	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4		PA2		PA0		PD14		PD12		PD10		PD8
APORT4X	BUSDX	PB15		PB13		PB11		PB9		PB7								PA7		PA5		PA3		PA1		PD15		PD13		PD11		PD9	

7. BGA125 Package Specifications

7.1 BGA125 Package Dimensions

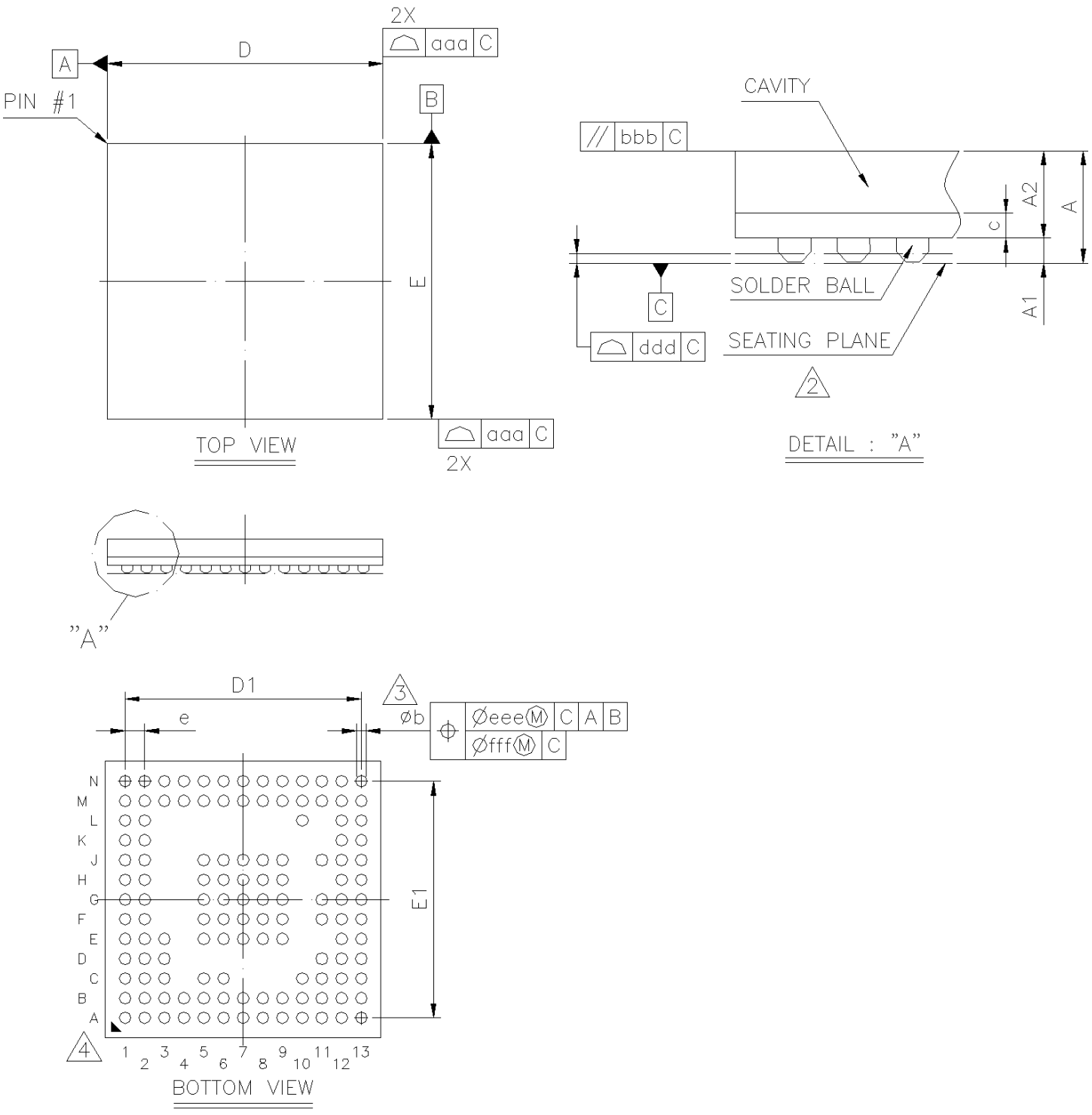


Figure 7.1. BGA125 Package Drawing

7.2 BGA125 PCB Land Pattern

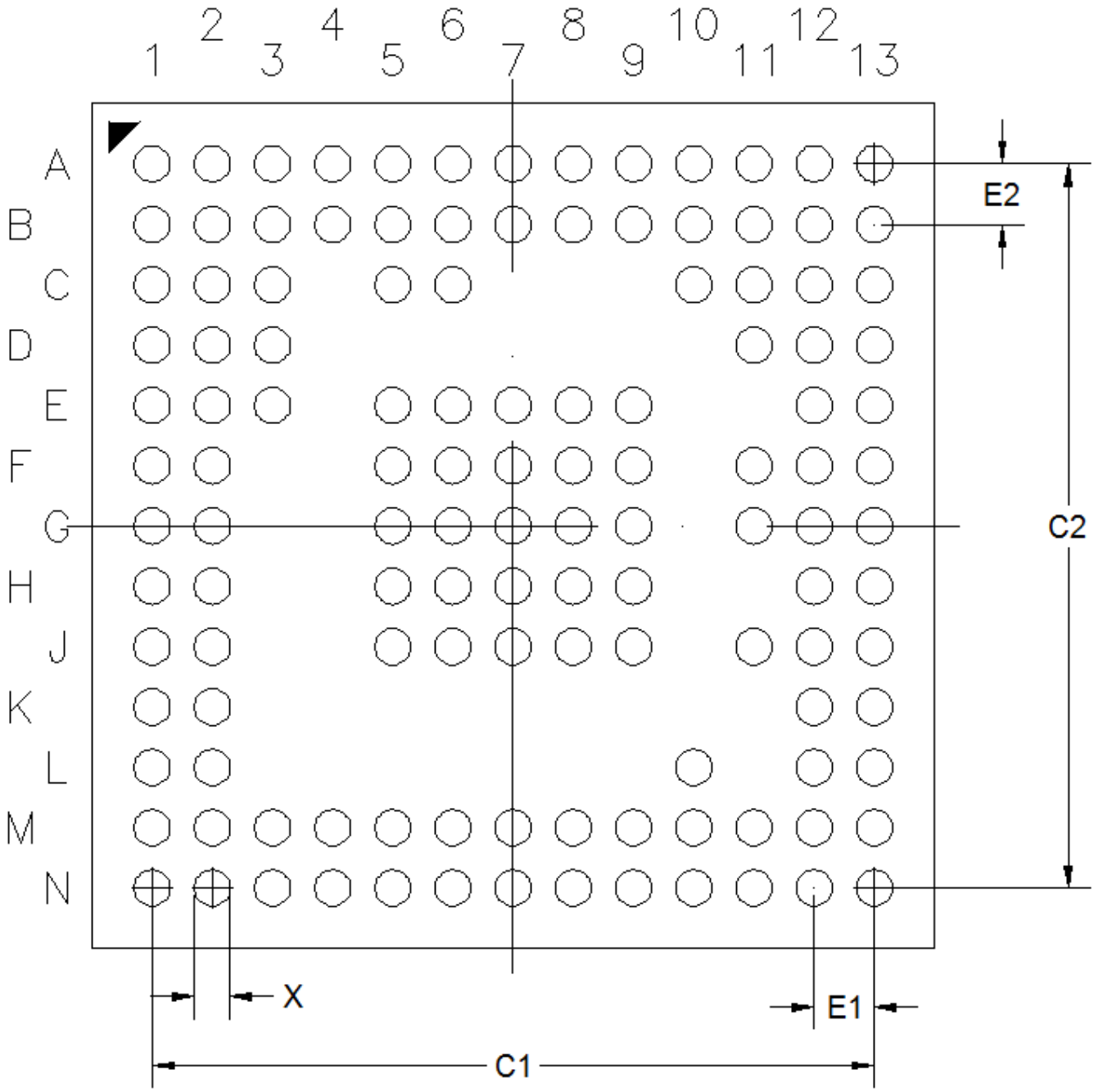


Figure 7.2. BGA125 PCB Land Pattern Drawing