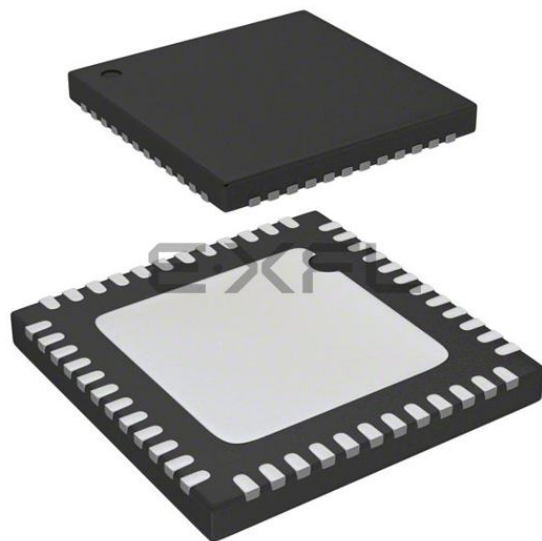




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	40MHz
Connectivity	I ² C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D - 12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32jg12b500f1024im48-br

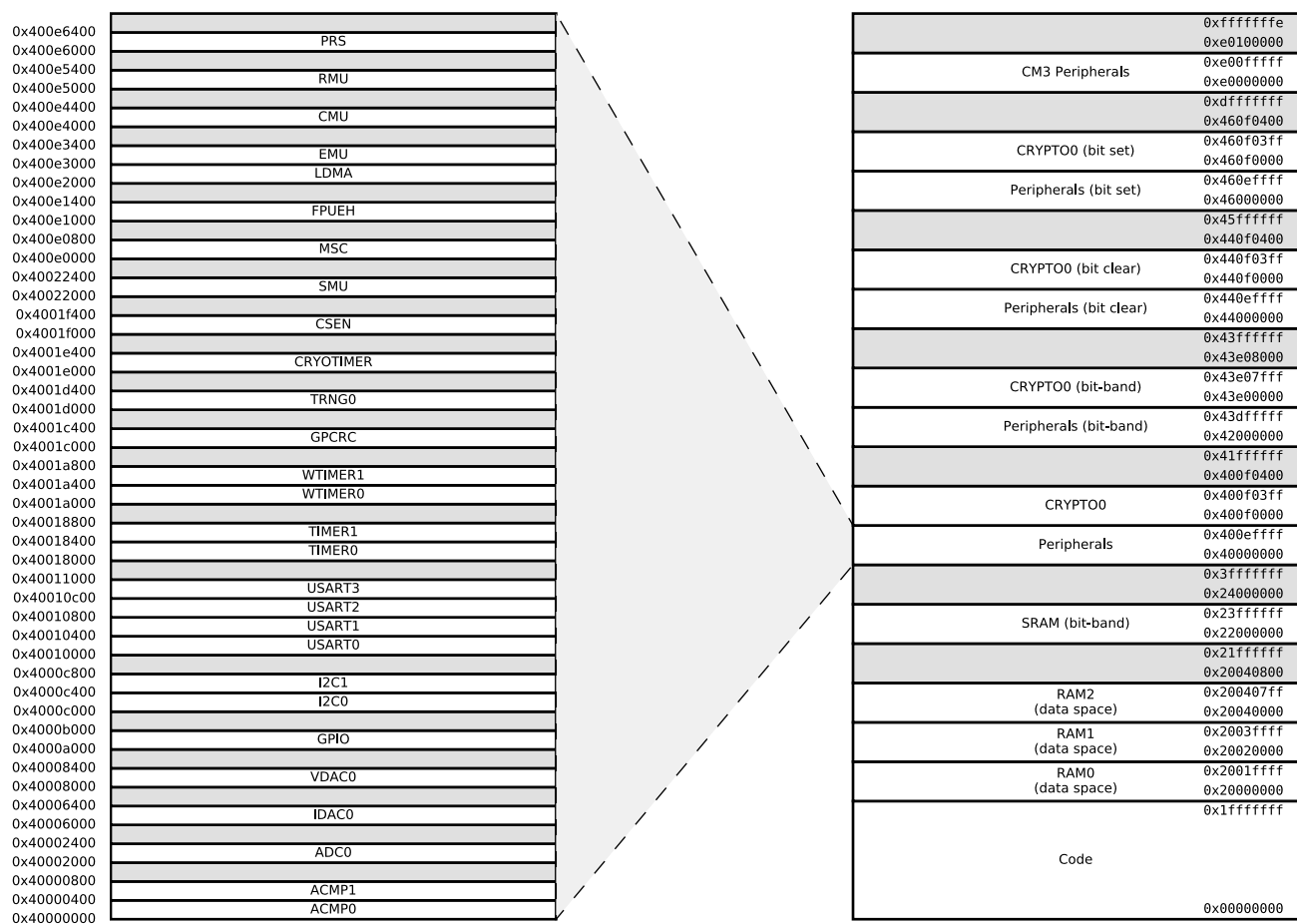


Figure 3.3. EFM32JG12 Memory Map — Peripherals

3.12 Configuration Summary

The features of the EFM32JG12 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.2. Configuration Summary

Module	Configuration	Pin Connections
USART0	IrDA SmartCard	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	IrDA I ² S SmartCard	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	IrDA SmartCard	US2_TX, US2_RX, US2_CLK, US2_CS
USART3	IrDA I ² S SmartCard	US3_TX, US3_RX, US3_CLK, US3_CS
TIMER0	with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	-	TIM1_CC[3:0]
WTIMER0	with DTI	WTIM0_CC[2:0], WTIM0_CDTI[2:0]
WTIMER1	-	WTIM1_CC[3:0]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM4S mode	I_{EM4S}	No RAM retention, no RTCC	—	0.07	TBD	μA
Note: 1. CMU_HFXOCTRL_LOWPOWER=1. 2. CMU_LFRCOCTRL_ENVREF = 1, CMU_LFRCOCTRL_VREFUPDATE = 1						

4.1.5.2 Current Consumption 3.3 V using DC-DC Converter

Unless otherwise indicated, typical conditions are: VREGVDD = AVDD = IOVDD = 3.3 V, DVDD = 1.8 V DC-DC output. T_{OP} = 25 °C. Minimum and maximum values in this table represent the worst conditions across supply voltage and process variation at T_{OP} = 25 °C.

Table 4.6. Current Consumption 3.3 V using DC-DC Converter

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise DCM mode ² .	I _{ACTIVE_DCM}	38.4 MHz crystal, CPU running while loop from flash ⁴	—	86	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	70	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	70	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	85	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	77	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	636	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in Low Noise CCM mode ¹ .	I _{ACTIVE_CCM}	38.4 MHz crystal, CPU running while loop from flash ⁴	—	96	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	81	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	82	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	95	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	95	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1155	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled, DCDC in LP mode ³ .	I _{ACTIVE_LPM}	38.4 MHz crystal, CPU running while loop from flash ⁴	—	80	—	μA/MHz
		38 MHz HFRCO, CPU running Prime from flash	—	64	—	μA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	64	—	μA/MHz
		38 MHz HFRCO, CPU running CoreMark from flash	—	79	—	μA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	66	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	224	—	μA/MHz
Current consumption in EM0 mode with all peripherals disabled and voltage scaling enabled, DCDC in Low Noise CCM mode ¹ .	I _{ACTIVE_CCM_VS}	19 MHz HFRCO, CPU running while loop from flash	—	101	—	μA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	1128	—	μA/MHz

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Hysteresis ($V_{CM} = 1.25\text{ V}$, $BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$)	$V_{ACMPHYST}$	$HYSTSEL^5 = HYST0$	TBD	—	TBD	mV
		$HYSTSEL^5 = HYST1$	TBD	18	TBD	mV
		$HYSTSEL^5 = HYST2$	TBD	32	TBD	mV
		$HYSTSEL^5 = HYST3$	TBD	44	TBD	mV
		$HYSTSEL^5 = HYST4$	TBD	55	TBD	mV
		$HYSTSEL^5 = HYST5$	TBD	65	TBD	mV
		$HYSTSEL^5 = HYST6$	TBD	77	TBD	mV
		$HYSTSEL^5 = HYST7$	TBD	86	TBD	mV
		$HYSTSEL^5 = HYST8$	TBD	—	TBD	mV
		$HYSTSEL^5 = HYST9$	TBD	-18	TBD	mV
		$HYSTSEL^5 = HYST10$	TBD	-32	TBD	mV
		$HYSTSEL^5 = HYST11$	TBD	-43	TBD	mV
		$HYSTSEL^5 = HYST12$	TBD	-54	TBD	mV
		$HYSTSEL^5 = HYST13$	TBD	-64	TBD	mV
		$HYSTSEL^5 = HYST14$	TBD	-74	TBD	mV
		$HYSTSEL^5 = HYST15$	TBD	-85	TBD	mV
Comparator delay ³	$t_{ACMPDELAY}$	$BIASPROG^4 = 1$, $FULLBIAS^4 = 0$	—	30	—	μs
		$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 0$	—	3.7	—	μs
		$BIASPROG^4 = 0x02$, $FULLBIAS^4 = 1$	—	360	—	ns
		$BIASPROG^4 = 0x20$, $FULLBIAS^4 = 1$	—	35	—	ns
Offset voltage	$V_{ACMPOFFSET}$	$BIASPROG^4 = 0x10$, $FULLBIAS^4 = 1$	TBD	—	TBD	mV
Reference voltage	$V_{ACMPREF}$	Internal 1.25 V reference	TBD	1.25	TBD	V
		Internal 2.5 V reference	TBD	2.5	TBD	V
Capacitive sense internal resistance	R_{CSRES}	$CSRESSEL^6 = 0$	—	inf	—	k Ω
		$CSRESSEL^6 = 1$	—	15	—	k Ω
		$CSRESSEL^6 = 2$	—	27	—	k Ω
		$CSRESSEL^6 = 3$	—	39	—	k Ω
		$CSRESSEL^6 = 4$	—	51	—	k Ω
		$CSRESSEL^6 = 5$	—	102	—	k Ω
		$CSRESSEL^6 = 6$	—	164	—	k Ω
		$CSRESSEL^6 = 7$	—	239	—	k Ω

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal to noise and distortion ratio (1 kHz sine wave), Noise band limited to 250 kHz	SNDR _{DAC}	500 ksps, single-ended, internal 1.25V reference	—	60.4	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	61.6	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	64.0	—	dB
		500 ksps, differential, internal 1.25V reference	—	63.3	—	dB
		500 ksps, differential, internal 2.5V reference	—	64.4	—	dB
		500 ksps, differential, 3.3V VDD reference	—	65.8	—	dB
Signal to noise and distortion ratio (1 kHz sine wave). Noise band limited to 22 kHz.	SNDR _{DAC_BAND}	500 ksps, single-ended, internal 1.25V reference	—	65.3	—	dB
		500 ksps, single-ended, internal 2.5V reference	—	66.7	—	dB
		500 ksps, differential, 3.3V VDD reference	—	68.5	—	dB
		500 ksps, differential, internal 1.25V reference	—	67.8	—	dB
		500 ksps, differential, internal 2.5V reference	—	69.0	—	dB
		500 ksps, single-ended, 3.3V VDD reference	—	70.0	—	dB
Total harmonic distortion	THD		—	70.2	—	dB
Differential non-linearity ³	DNL _{DAC}		TBD	—	TBD	LSB
Integral non-linearity	INL _{DAC}		TBD	—	TBD	LSB
Offset error ⁵	V _{OFFSET}	T _J = 25 °C	TBD	—	TBD	mV
		-40 °C ≤ T _J ≤ 85 °C	TBD	—	TBD	mV
Gain error ⁵	V _{GAIN}	T _J = 25 °C	TBD	—	TBD	%
		-40 °C ≤ T _J ≤ 85 °C	TBD	—	TBD	%
External load capacitance, OUTSCALE=0	C _{LOAD}		—	—	75	pF

Note:

1. Supply current specifications are for VDAC circuitry operating with static output only and do not include current required to drive the load.
2. In differential mode, the output is defined as the difference between two single-ended outputs. Absolute voltage on each output is limited to the single-ended range.
3. Entire range is monotonic and has no missing codes.
4. Current from HPERCLK is dependent on HPERCLK frequency. This current contributes to the total supply current used when the clock to the DAC module is enabled in the CMU.
5. Gain is calculated by measuring the slope from 10% to 90% of full scale. Offset is calculated by comparing actual VDAC output at 10% of full scale to ideal VDAC output at 10% of full scale with the measured gain.
6. PSRR calculated as $20 * \log_{10}(\Delta V_{DD} / \Delta V_{OUT})$, VDAC output at 90% of full scale

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Open-loop gain	G _{OL}	DRIVESTRENGTH = 3	—	135	—	dB
		DRIVESTRENGTH = 2	—	137	—	dB
		DRIVESTRENGTH = 1	—	121	—	dB
		DRIVESTRENGTH = 0	—	109	—	dB
Loop unit-gain frequency ⁷	UGF	DRIVESTRENGTH = 3, Buffer connection	—	3.38	—	MHz
		DRIVESTRENGTH = 2, Buffer connection	—	0.9	—	MHz
		DRIVESTRENGTH = 1, Buffer connection	—	132	—	kHz
		DRIVESTRENGTH = 0, Buffer connection	—	34	—	kHz
		DRIVESTRENGTH = 3, 3x Gain connection	—	2.57	—	MHz
		DRIVESTRENGTH = 2, 3x Gain connection	—	0.71	—	MHz
		DRIVESTRENGTH = 1, 3x Gain connection	—	113	—	kHz
		DRIVESTRENGTH = 0, 3x Gain connection	—	28	—	kHz
Phase margin	PM	DRIVESTRENGTH = 3, Buffer connection	—	67	—	°
		DRIVESTRENGTH = 2, Buffer connection	—	69	—	°
		DRIVESTRENGTH = 1, Buffer connection	—	63	—	°
		DRIVESTRENGTH = 0, Buffer connection	—	68	—	°
Output voltage noise	N _{OUT}	DRIVESTRENGTH = 3, Buffer connection, 10 Hz - 10 MHz	—	146	—	μVrms
		DRIVESTRENGTH = 2, Buffer connection, 10 Hz - 10 MHz	—	163	—	μVrms
		DRIVESTRENGTH = 1, Buffer connection, 10 Hz - 1 MHz	—	170	—	μVrms
		DRIVESTRENGTH = 0, Buffer connection, 10 Hz - 1 MHz	—	176	—	μVrms
		DRIVESTRENGTH = 3, 3x Gain connection, 10 Hz - 10 MHz	—	313	—	μVrms
		DRIVESTRENGTH = 2, 3x Gain connection, 10 Hz - 10 MHz	—	271	—	μVrms
		DRIVESTRENGTH = 1, 3x Gain connection, 10 Hz - 1 MHz	—	247	—	μVrms
		DRIVESTRENGTH = 0, 3x Gain connection, 10 Hz - 1 MHz	—	245	—	μVrms

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slew rate ⁵	SR	DRIVESTRENGTH = 3, INCBW=1 ³	—	4.7	—	V/μs
		DRIVESTRENGTH = 3, INCBW=0	—	1.5	—	V/μs
		DRIVESTRENGTH = 2, INCBW=1 ³	—	1.27	—	V/μs
		DRIVESTRENGTH = 2, INCBW=0	—	0.42	—	V/μs
		DRIVESTRENGTH = 1, INCBW=1 ³	—	0.17	—	V/μs
		DRIVESTRENGTH = 1, INCBW=0	—	0.058	—	V/μs
		DRIVESTRENGTH = 0, INCBW=1 ³	—	0.044	—	V/μs
		DRIVESTRENGTH = 0, INCBW=0	—	0.015	—	V/μs
Startup time ⁶	T _{START}	DRIVESTRENGTH = 3	—	—	TBD	μs
		DRIVESTRENGTH = 2	—	—	TBD	μs
		DRIVESTRENGTH = 1	—	—	TBD	μs
		DRIVESTRENGTH = 0	—	—	TBD	μs
Input offset voltage	V _{OSI}	DRIVESTRENGTH = 2 or 3, T _J = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, T _J = 25 °C	TBD	—	TBD	mV
		DRIVESTRENGTH = 2 or 3, across operating temperature range	TBD	—	TBD	mV
		DRIVESTRENGTH = 1 or 0, across operating temperature range	TBD	—	TBD	mV
DC power supply rejection ratio ⁹	PSRR _{DC}	Input referred	—	70	—	dB
DC common-mode rejection ratio ⁹	CMRR _{DC}	Input referred	—	70	—	dB
Total harmonic distortion	THD _{OPA}	DRIVESTRENGTH = 2, 3x Gain connection, 1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB
		DRIVESTRENGTH = 0, 3x Gain connection, 0.1 kHz, V _{OUT} = 0.1 V to V _{OPA} - 0.1 V	—	90	—	dB

4.1.20.3 I2C Fast-mode Plus (Fm+)¹Table 4.29. I2C Fast-mode Plus (Fm+)¹

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL clock frequency ²	f _{SCL}		0	—	1000	kHz
SCL clock low time	t _{LOW}		0.5	—	—	μs
SCL clock high time	t _{HIGH}		0.26	—	—	μs
SDA set-up time	t _{SU_DAT}		50	—	—	ns
SDA hold time	t _{HD_DAT}		100	—	—	ns
Repeated START condition set-up time	t _{SU_STA}		0.26	—	—	μs
(Repeated) START condition hold time	t _{HD_STA}		0.26	—	—	μs
STOP condition set-up time	t _{SU_STO}		0.26	—	—	μs
Bus free time between a STOP and START condition	t _{BUF}		0.5	—	—	μs

Note:

1. For CLHR set to 0 or 1 in the I2Cn_CTRL register.
2. For the minimum HPERCLK frequency required in Fast-mode Plus, refer to the I2C chapter in the reference manual.

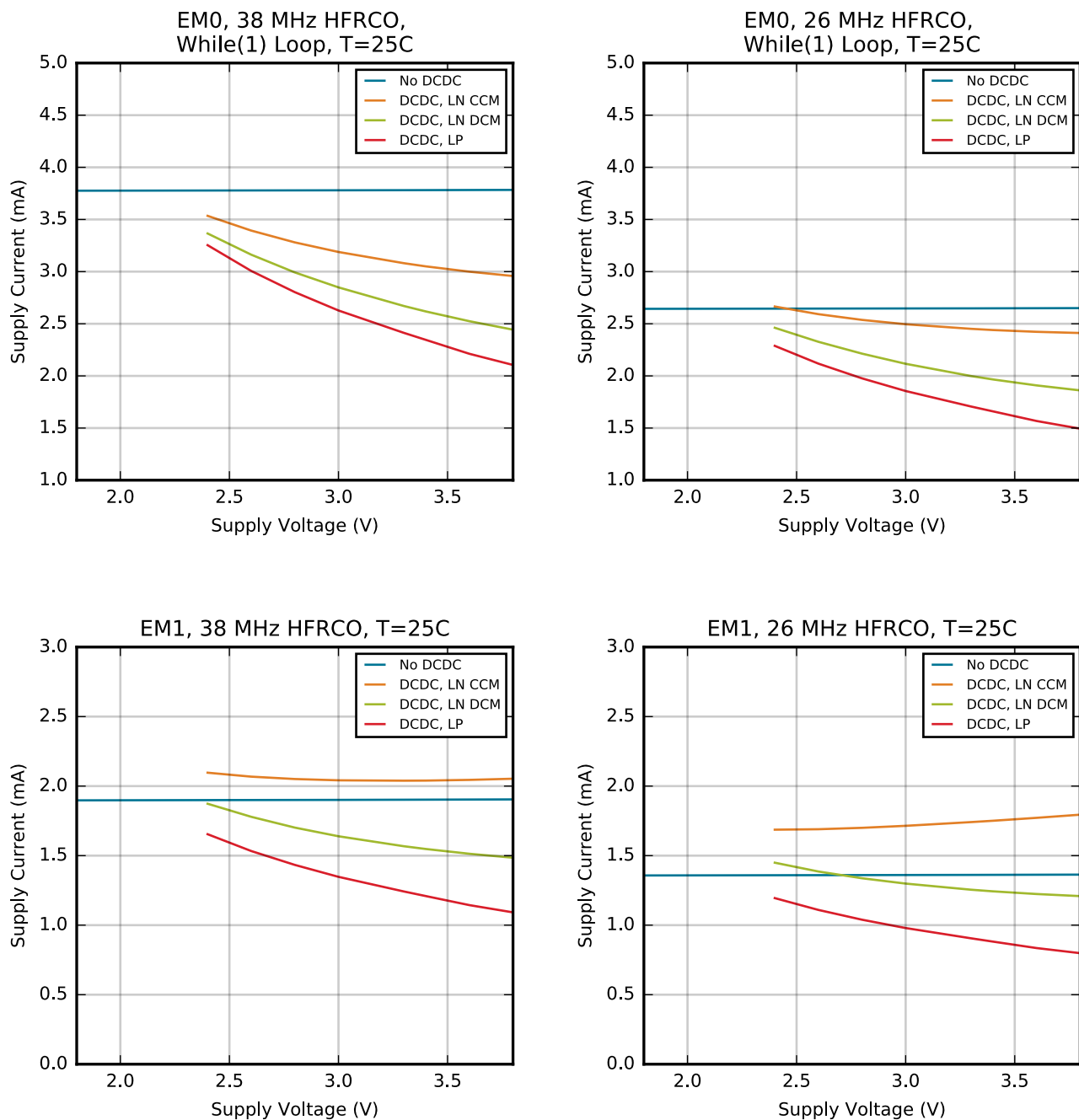


Figure 4.6. EM0 and EM1 Mode Typical Supply Current vs. Supply

Typical supply current for EM2, EM3 and EM4H using standard software libraries from Silicon Laboratories.

4.2.2 DC-DC Converter

Default test conditions: CCM mode, LDCDC = 4.7 μ H, CDCDC = 4.7 μ F, VDCDC_I = 3.3 V, VDCDC_O = 1.8 V, FDCDC_LN = 7 MHz

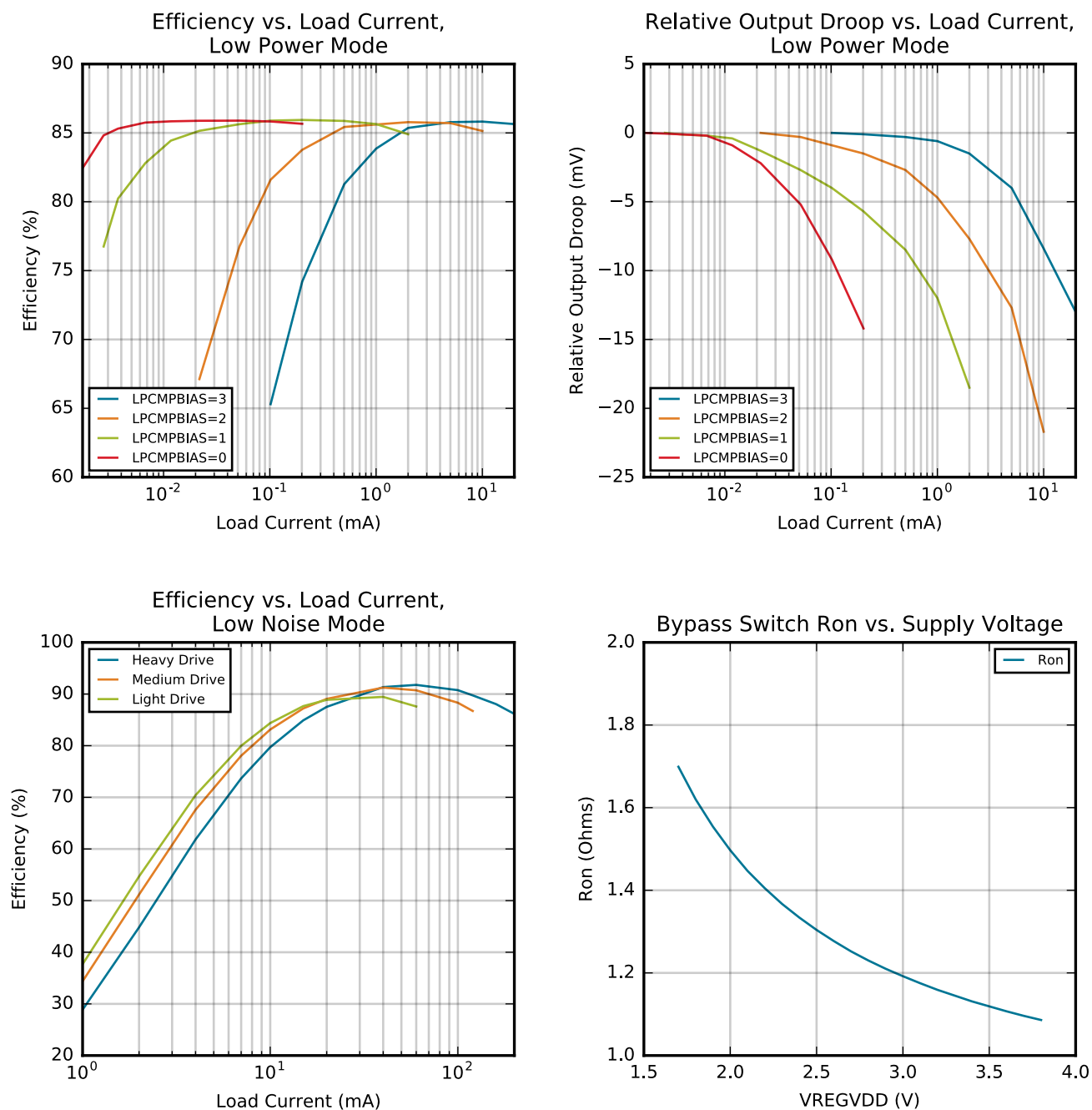


Figure 4.8. DC-DC Converter Typical Performance Characteristics

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
M11	PD13	VDAC0_OUT0ALT / OPA0_OUTALT #1 BUSCY BUSDX OPA1_P	TIM0_CC0 #21 TIM0_CC1 #20 TIM0_CC2 #19 TIM0_CDTI0 #18 TIM0_CDTI1 #17 TIM0_CDTI2 #16 TIM1_CC0 #21 TIM1_CC1 #20 TIM1_CC2 #19 TIM1_CC3 #18 WTIM0_CDTI0 #29 WTIM0_CDTI1 #27 WTIM0_CDTI2 #25 WTIM1_CC0 #21 WTIM1_CC1 #19 WTIM1_CC2 #17 WTIM1_CC3 #15 LE- TIM0_OUT0 #21 LE- TIM0_OUT1 #20 PCNT0_S0IN #21 PCNT0_S1IN #20	US0_TX #21 US0_RX #20 US0_CLK #19 US0_CS #18 US0_CTS #17 US0_RTS #16 US1_TX #21 US1_RX #20 US1_CLK #19 US1_CS #18 US1_CTS #17 US1_RTS #16 US3_TX #5 US3_RX #4 US3_CLK #3 US3_CS #2 US3_CTS #1 US3_RTS #0 LEU0_TX #21 LEU0_RX #20 I2C0_SDA #21 I2C0_SCL #20	PRS_CH3 #12 PRS_CH4 #4 PRS_CH5 #3 PRS_CH6 #15 ACMP0_O #21 ACMP1_O #21 LES_CH5
M12	IOVDD	Digital IO power supply .			
M13	PA0	BUSDY BUSCX ADC0_EXTN	TIM0_CC0 #0 TIM0_CC1 #31 TIM0_CC2 #30 TIM0_CDTI0 #29 TIM0_CDTI1 #28 TIM0_CDTI2 #27 TIM1_CC0 #0 TIM1_CC1 #31 TIM1_CC2 #30 TIM1_CC3 #29 WTIM0_CC0 #0 LE- TIM0_OUT0 #0 LE- TIM0_OUT1 #31 PCNT0_S0IN #0 PCNT0_S1IN #31	US0_TX #0 US0_RX #31 US0_CLK #30 US0_CS #29 US0_CTS #28 US0_RTS #27 US1_TX #0 US1_RX #31 US1_CLK #30 US1_CS #29 US1_CTS #28 US1_RTS #27 LEU0_TX #0 LEU0_RX #31 I2C0_SDA #0 I2C0_SCL #31	CMU_CLK1 #0 PRS_CH6 #0 PRS_CH7 #10 PRS_CH8 #9 PRS_CH9 #8 ACMP0_O #0 ACMP1_O #0 LES_CH8
N1	NC	No Connect.			
N2	NC	No Connect.			
N3	NC	No Connect.			
N4	NC	No Connect.			
N5	VSS	Ground			
N6	NC	No Connect.			
N7	NC	No Connect.			
N8	NC	No Connect.			

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
N12	PD14	BUSDY BUSCX VDAC0_OUT1 / OPA1_OUT	TIM0_CC0 #22 TIM0_CC1 #21 TIM0_CC2 #20 TIM0_CDTI0 #19 TIM0_CDTI1 #18 TIM0_CDTI2 #17 TIM1_CC0 #22 TIM1_CC1 #21 TIM1_CC2 #20 TIM1_CC3 #19 WTIM0_CDTI0 #30 WTIM0_CDTI1 #28 WTIM0_CDTI2 #26 WTIM1_CC0 #22 WTIM1_CC1 #20 WTIM1_CC2 #18 WTIM1_CC3 #16 LE- TIM0_OUT0 #22 LE- TIM0_OUT1 #21 PCNT0_S0IN #22 PCNT0_S1IN #21	US0_TX #22 US0_RX #21 US0_CLK #20 US0_CS #19 US0_CTS #18 US0_RTS #17 US1_TX #22 US1_RX #21 US1_CLK #20 US1_CS #19 US1_CTS #18 US1_RTS #17 US3_TX #6 US3_RX #5 US3_CLK #4 US3_CS #3 US3_CTS #2 US3_RTS #1 LEU0_TX #22 LEU0_RX #21 I2C0_SDA #22 I2C0_SCL #21	CMU_CLK0 #5 PRS_CH3 #13 PRS_CH4 #5 PRS_CH5 #4 PRS_CH6 #16 ACMP0_O #22 ACMP1_O #22 LES_CH6 GPIO_EM4WU4
N13	PD15	VDAC0_OUT0ALT / OPA0_OUTALT #2 BUSCY BUSDX OPA1_N	TIM0_CC0 #23 TIM0_CC1 #22 TIM0_CC2 #21 TIM0_CDTI0 #20 TIM0_CDTI1 #19 TIM0_CDTI2 #18 TIM1_CC0 #23 TIM1_CC1 #22 TIM1_CC2 #21 TIM1_CC3 #20 WTIM0_CDTI0 #31 WTIM0_CDTI1 #29 WTIM0_CDTI2 #27 WTIM1_CC0 #23 WTIM1_CC1 #21 WTIM1_CC2 #19 WTIM1_CC3 #17 LE- TIM0_OUT0 #23 LE- TIM0_OUT1 #22 PCNT0_S0IN #23 PCNT0_S1IN #22	US0_TX #23 US0_RX #22 US0_CLK #21 US0_CS #20 US0_CTS #19 US0_RTS #18 US1_TX #23 US1_RX #22 US1_CLK #21 US1_CS #20 US1_CTS #19 US1_RTS #18 US3_TX #7 US3_RX #6 US3_CLK #5 US3_CS #4 US3_CTS #3 US3_RTS #2 LEU0_TX #23 LEU0_RX #22 I2C0_SDA #23 I2C0_SCL #22	CMU_CLK1 #5 PRS_CH3 #14 PRS_CH4 #6 PRS_CH5 #5 PRS_CH6 #17 ACMP0_O #23 ACMP1_O #23 LES_CH7 DBG_SWO #2

6.2 EFM32JG12B5xx in QFN48 Device Pinout

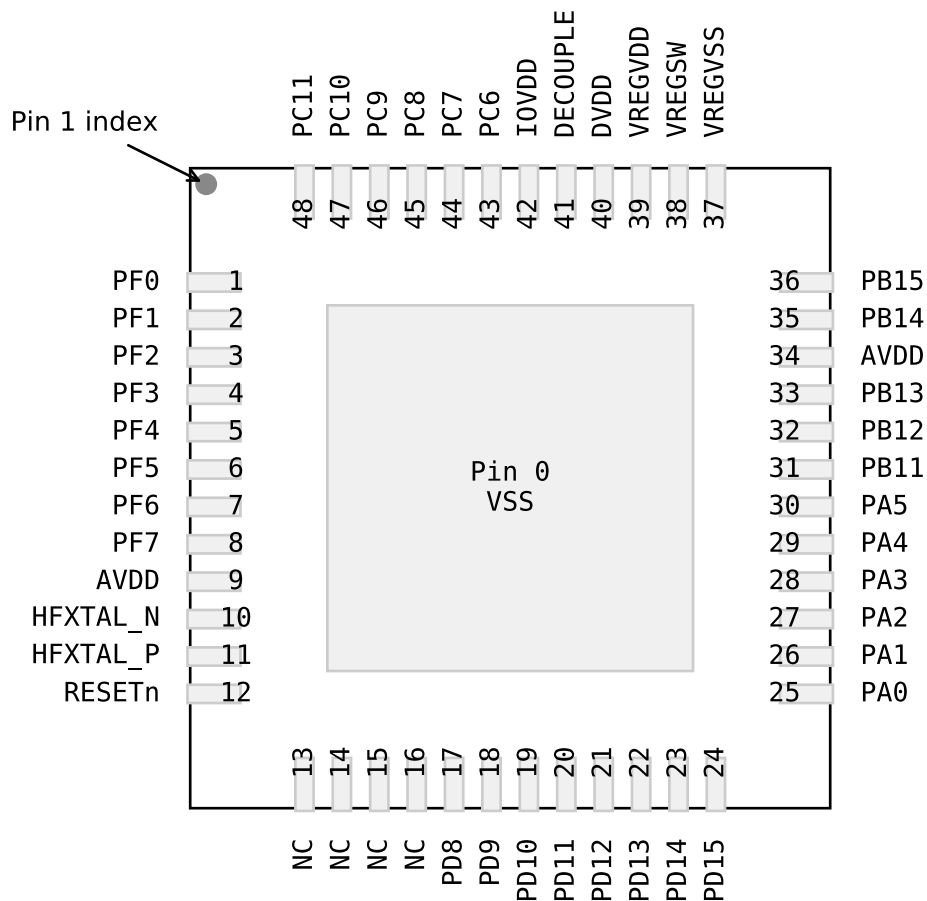


Figure 6.2. EFM32JG12B5xx in QFN48 Device Pinout

Table 6.3. EFM32JG12B5xx in QFN48 Device Pinout

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground			
1	PF0	BUSBY BUSAX	TIM0_CC0 #24 TIM0_CC1 #23 TIM0_CC2 #22 TIM0_CDTI0 #21 TIM0_CDTI1 #20 TIM0_CDTI2 #19 TIM1_CC0 #24 TIM1_CC1 #23 TIM1_CC2 #22 TIM1_CC3 #21 WTIM0_CDTI1 #30 WTIM0_CDTI2 #28 WTIM1_CC0 #24 WTIM1_CC1 #22 WTIM1_CC2 #20 WTIM1_CC3 #18 LE- TIM0_OUT0 #24 LE- TIM0_OUT1 #23 PCNT0_S0IN #24 PCNT0_S1IN #23	US0_TX #24 US0_RX #23 US0_CLK #22 US0_CS #21 US0_CTS #20 US0_RTS #19 US1_TX #24 US1_RX #23 US1_CLK #22 US1_CS #21 US1_CTS #20 US1_RTS #19 US2_TX #14 US2_RX #13 US2_CLK #12 US2_CS #11 US2_CTS #10 US2_RTS #9 LEU0_TX #24 LEU0_RX #23 I2C0_SDA #24 I2C0_SCL #23	PRS_CH0 #0 PRS_CH1 #7 PRS_CH2 #6 PRS_CH3 #5 ACMP0_O #24 ACMP1_O #24 DBG_SWCLKTCK BOOT_TX
2	PF1	BUSAY BUSBX	TIM0_CC0 #25 TIM0_CC1 #24 TIM0_CC2 #23 TIM0_CDTI0 #22 TIM0_CDTI1 #21 TIM0_CDTI2 #20 TIM1_CC0 #25 TIM1_CC1 #24 TIM1_CC2 #23 TIM1_CC3 #22 WTIM0_CDTI1 #31 WTIM0_CDTI2 #29 WTIM1_CC0 #25 WTIM1_CC1 #23 WTIM1_CC2 #21 WTIM1_CC3 #19 LE- TIM0_OUT0 #25 LE- TIM0_OUT1 #24 PCNT0_S0IN #25 PCNT0_S1IN #24	US0_TX #25 US0_RX #24 US0_CLK #23 US0_CS #22 US0_CTS #21 US0_RTS #20 US1_TX #25 US1_RX #24 US1_CLK #23 US1_CS #22 US1_CTS #21 US1_RTS #20 US2_TX #15 US2_RX #14 US2_CLK #13 US2_CS #12 US2_CTS #11 US2_RTS #10 LEU0_TX #25 LEU0_RX #24 I2C0_SDA #25 I2C0_SCL #24	PRS_CH0 #1 PRS_CH1 #0 PRS_CH2 #7 PRS_CH3 #6 ACMP0_O #25 ACMP1_O #25 DBG_SWDIOTMS BOOT_RX

Pin		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PF2	BUSBY BUSAX	TIM0_CC0 #26 TIM0_CC1 #25 TIM0_CC2 #24 TIM0_CDTI0 #23 TIM0_CDTI1 #22 TIM0_CDTI2 #21 TIM1_CC0 #26 TIM1_CC1 #25 TIM1_CC2 #24 TIM1_CC3 #23 WTIM0_CDTI2 #30 WTIM1_CC0 #26 WTIM1_CC1 #24 WTIM1_CC2 #22 WTIM1_CC3 #20 LE- TIM0_OUT0 #26 LE- TIM0_OUT1 #25 PCNT0_S0IN #26 PCNT0_S1IN #25	US0_TX #26 US0_RX #25 US0_CLK #24 US0_CS #23 US0_CTS #22 US0_RTS #21 US1_TX #26 US1_RX #25 US1_CLK #24 US1_CS #23 US1_CTS #22 US1_RTS #21 LEU0_TX #26 LEU0_RX #25 I2C0_SDA #26 I2C0_SCL #25	CMU_CLK0 #6 PRS_CH0 #2 PRS_CH1 #1 PRS_CH2 #0 PRS_CH3 #7 ACMP0_O #26 ACMP1_O #26 DBG_TDO DBG_SWO #0 GPIO_EM4WU0
4	PF3	BUSAY BUSBX	TIM0_CC0 #27 TIM0_CC1 #26 TIM0_CC2 #25 TIM0_CDTI0 #24 TIM0_CDTI1 #23 TIM0_CDTI2 #22 TIM1_CC0 #27 TIM1_CC1 #26 TIM1_CC2 #25 TIM1_CC3 #24 WTIM0_CDTI2 #31 WTIM1_CC0 #27 WTIM1_CC1 #25 WTIM1_CC2 #23 WTIM1_CC3 #21 LE- TIM0_OUT0 #27 LE- TIM0_OUT1 #26 PCNT0_S0IN #27 PCNT0_S1IN #26	US0_TX #27 US0_RX #26 US0_CLK #25 US0_CS #24 US0_CTS #23 US0_RTS #22 US1_TX #27 US1_RX #26 US1_CLK #25 US1_CS #24 US1_CTS #23 US1_RTS #22 US2_TX #16 US2_RX #15 US2_CLK #14 US2_CS #13 US2_CTS #12 US2_RTS #11 LEU0_TX #27 LEU0_RX #26 I2C0_SDA #27 I2C0_SCL #26	CMU_CLK1 #6 PRS_CH0 #3 PRS_CH1 #2 PRS_CH2 #1 PRS_CH3 #0 ACMP0_O #27 ACMP1_O #27 DBG_TDI
5	PF4	BUSBY BUSAX	TIM0_CC0 #28 TIM0_CC1 #27 TIM0_CC2 #26 TIM0_CDTI0 #25 TIM0_CDTI1 #24 TIM0_CDTI2 #23 TIM1_CC0 #28 TIM1_CC1 #27 TIM1_CC2 #26 TIM1_CC3 #25 WTIM1_CC0 #28 WTIM1_CC1 #26 WTIM1_CC2 #24 WTIM1_CC3 #22 LE- TIM0_OUT0 #28 LE- TIM0_OUT1 #27 PCNT0_S0IN #28 PCNT0_S1IN #27	US0_TX #28 US0_RX #27 US0_CLK #26 US0_CS #25 US0_CTS #24 US0_RTS #23 US1_TX #28 US1_RX #27 US1_CLK #26 US1_CS #25 US1_CTS #24 US1_RTS #23 US2_TX #17 US2_RX #16 US2_CLK #15 US2_CS #14 US2_CTS #13 US2_RTS #12 LEU0_TX #28 LEU0_RX #27 I2C0_SDA #28 I2C0_SCL #27	PRS_CH0 #4 PRS_CH1 #3 PRS_CH2 #2 PRS_CH3 #1 ACMP0_O #28 ACMP1_O #28

Alternate	LOCATION								
Functionality	0 - 3	4 - 7	8 - 11	12 - 15	16 - 19	20 - 23	24 - 27	28 - 31	Description
PRS_CH7	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PA0						Peripheral Reflex System PRS, channel 7.
PRS_CH8	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PA0 10: PA1						Peripheral Reflex System PRS, channel 8.
PRS_CH9	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PA0 9: PA1 10: PA2 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11				Peripheral Reflex System PRS, channel 9.
PRS_CH10	0: PC6 1: PC7 2: PC8 3: PC9	4: PC10 5: PC11							Peripheral Reflex System PRS, channel 10.
PRS_CH11	0: PC7 1: PC8 2: PC9 3: PC10	4: PC11 5: PC6							Peripheral Reflex System PRS, channel 11.
TIM0_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	0: PA2 1: PA3 2: PA4 3: PA5	4: PB11 5: PB12 6: PB13 7: PB14	8: PB15 9: PC6 10: PC7 11: PC8	12: PC9 13: PC10 14: PC11 15: PD9	16: PD10 17: PD11 18: PD12 19: PD13	20: PD14 21: PD15 22: PF0 23: PF1	24: PF2 25: PF3 26: PF4 27: PF5	28: PF6 29: PF7 30: PA0 31: PA1	Timer 0 Capture Compare input / output channel 2.
TIM0_CDT10	0: PA3 1: PA4 2: PA5 3: PB11	4: PB12 5: PB13 6: PB14 7: PB15	8: PC6 9: PC7 10: PC8 11: PC9	12: PC10 13: PC11 14: PD9 15: PD10	16: PD11 17: PD12 18: PD13 19: PD14	20: PD15 21: PF0 22: PF1 23: PF2	24: PF3 25: PF4 26: PF5 27: PF6	28: PF7 29: PA0 30: PA1 31: PA2	Timer 0 Complimentary Dead Time Insertion channel 0.
TIM0_CDT11	0: PA4 1: PA5 2: PB11 3: PB12	4: PB13 5: PB14 6: PB15 7: PC6	8: PC7 9: PC8 10: PC9 11: PC10	12: PC11 13: PD9 14: PD10 15: PD11	16: PD12 17: PD13 18: PD14 19: PD15	20: PF0 21: PF1 22: PF2 23: PF3	24: PF4 25: PF5 26: PF6 27: PF7	28: PA0 29: PA1 30: PA2 31: PA3	Timer 0 Complimentary Dead Time Insertion channel 1.
TIM0_CDT12	0: PA5 1: PB11 2: PB12 3: PB13	4: PB14 5: PB15 6: PC6 7: PC7	8: PC8 9: PC9 10: PC10 11: PC11	12: PD9 13: PD10 14: PD11 15: PD12	16: PD13 17: PD14 18: PD15 19: PF0	20: PF1 21: PF2 22: PF3 23: PF4	24: PF5 25: PF6 26: PF7 27: PA0	28: PA1 29: PA2 30: PA3 31: PA4	Timer 0 Complimentary Dead Time Insertion channel 2.
TIM1_CC0	0: PA0 1: PA1 2: PA2 3: PA3	4: PA4 5: PA5 6: PB11 7: PB12	8: PB13 9: PB14 10: PB15 11: PC6	12: PC7 13: PC8 14: PC9 15: PC10	16: PC11 17: PD9 18: PD10 19: PD11	20: PD12 21: PD13 22: PD14 23: PD15	24: PF0 25: PF1 26: PF2 27: PF3	28: PF4 29: PF5 30: PF6 31: PF7	Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	0: PA1 1: PA2 2: PA3 3: PA4	4: PA5 5: PB11 6: PB12 7: PB13	8: PB14 9: PB15 10: PC6 11: PC7	12: PC8 13: PC9 14: PC10 15: PC11	16: PD9 17: PD10 18: PD11 19: PD12	20: PD13 21: PD14 22: PD15 23: PF0	24: PF1 25: PF2 26: PF3 27: PF4	28: PF5 29: PF6 30: PF7 31: PA0	Timer 1 Capture Compare input / output channel 1.

Table 6.7. ACMP1 Bus and Pin Mapping

APORT4Y	APORT4X	APORT3Y	APORT3X	APORT2Y	APORT2X	APORT1Y	APORT1X	APORT0Y	APORT0X	Port
BUSDY	BUSDX	BUSCY	BUSCX	BUSBY	BUSBX	BUSAY	BUSAX	BUSACMP1Y	BUSACMP1X	Bus
PB14	PB15	PB15	PB14	PF14	PF15	PF15	PF14			CH31
	PB13	PB13			PF13	PF13				CH30
PB12			PB12	PF12			PF12			CH29
	PB11	PB11			PF11	PF11				CH28
PB10			PB10	PF10			PF10			CH27
	PB9	PB9			PF9	PF9				CH26
PB8			PB8	PF8			PF8			CH25
	PB7	PB7			PF7	PF7				CH24
PB6			PB6	PF6			PF6			CH23
					PF5	PF5				CH22
				PF4			PF4			CH21
					PF3	PF3				CH20
				PF2			PF2			CH19
					PF1	PF1				CH18
				PF0			PF0			CH17
	PA7	PA7								CH16
PA6			PA6							CH15
	PA5	PA5								CH14
PA4			PA4							CH13
	PA3	PA3			PC11	PC11				CH12
PA2			PA2	PC10			PC10			CH11
	PA1	PA1			PC9	PC9				CH10
PA0			PA0	PC8			PC8			CH9
	PD15	PD15			PC7	PC7		PJ15	PJ15	CH8
PD14			PD14	PC6			PC6	PJ14	PJ14	CH7
	PD13	PD13			PC5	PC5				CH6
PD12			PD12	PC4			PC4			CH5
	PD11	PD11			PC3	PC3				CH4
PD10			PD10	PC2			PC2			CH3
	PD9	PD9			PC1	PC1				CH2
PD8			PD8	PC0			PC0			CH1
										CH0

Table 6.9. CSEN Bus and Pin Mapping

Port	Bus	CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0	
CEXT																																		
APORT1X	BUSCY	PB15		PB13		PB11		PB9		PB7								PA7				PA3		PA1		PD15		PD13		PD11		PD9		
	BUSCX		PB14		PB12		PB10		PB8		PB6								PA6		PA4			PA2		PA0		PD14		PD12		PD10		
APORT1Y	BUSAY	PF15		PF13		PF11		PF9		PF7		PF5		PF3		PF1						PC11			PC9		PC7		PC5		PC3		PC1	
	BUSAX		PF14		PF12		PF10		PF8		PF6		PF4		PF2		PF0						PC10			PC8		PC6		PC4		PC2		
APORT3X																																		
APORT3Y																																		
APORT3X																																		
APORT1Y																																		
APORT1X																																		
APORT3Y																																		
APORT3X																																		
APORT1Y																																		
APORT1X																																		
APORT3Y																																		
APORT3X																																		
APORT1Y																																		
APORT1X																																		
APORT3Y																																		
APORT3X																																		
APORT1Y																																		
APORT1X																																		
																															</			

CEXT Sense

APORT4Y	APORT4X	APORT2Y	APORT2X
BUSDY	BUSDX	BUSBY	BUSBX
PB14	PB15	PF14	PF15
	PB13		PF13
PB12		PF12	
	PB11		PF11
PB10		PF10	
	PB9		PF9
PB8		PF8	
	PB7		PF7
PB6		PF6	
		PF4	PF5
		PF2	PF3
		PF0	PF1
	PA7		
PA6			
	PA5		
PA4			
	PA3		PC11
PA2		PC10	
PA0	PA1	PC8	PC9
	PD15		PC7
PD14		PC6	
	PD13		PC5
PD12		PC4	
	PD11		PC3
PD10		PC2	
	PD9		PC1
PD8		PC0	

Table 6.10. IDAC0 Bus and Pin Mapping

APORT1Y	APORT1X	Port
BUSCY	BUSCX	Bus
PB15		CH31
	PB14	CH30
PB13		CH29
	PB12	CH28
PB11		CH27
	PB10	CH26
PB9		CH25
	PB8	CH24
PB7		CH23
	PB6	CH22
		CH21
		CH20
		CH19
		CH18
		CH17
		CH16
PA7		CH15
	PA6	CH14
PA5		CH13
	PA4	CH12
PA3		CH11
	PA2	CH10
PA1		CH9
	PA0	CH8
PD15		CH7
	PD14	CH6
PD13		CH5
	PD12	CH4
PD11		CH3
	PD10	CH2
PD9		CH1
	PD8	CH0

8.2 QFN48 PCB Land Pattern

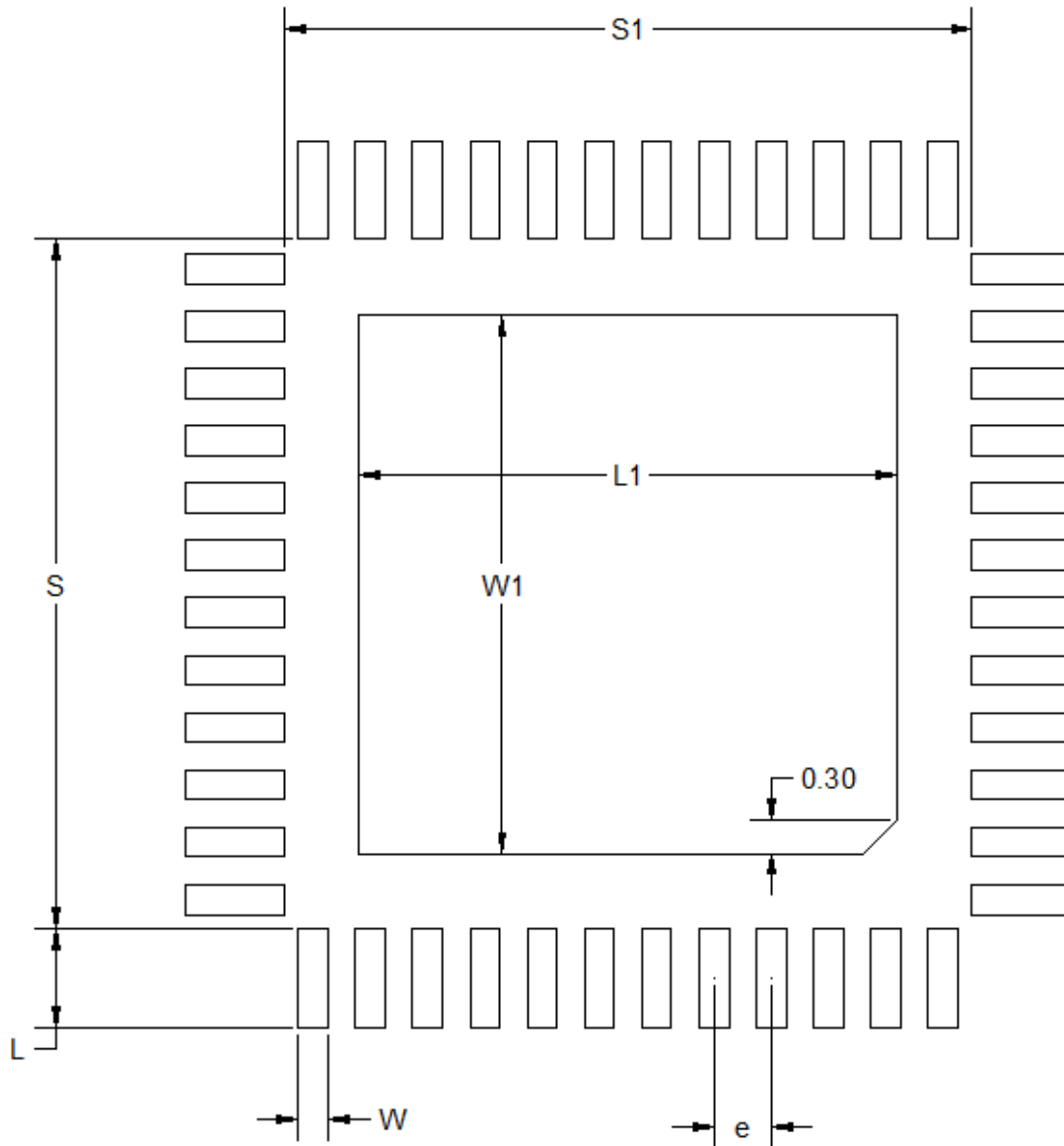


Figure 8.2. QFN48 PCB Land Pattern Drawing