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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Not For New Designs
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, I ² C, IrDA, SD, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 37x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dn512zvll10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Terminology and guidelines

Field	Description	Values
FFF	Program flash memory size	 32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB 512 = 512 KB 1M0 = 1 MB 2M0 = 2 MB
R	Silicon revision	 Z = Initial (Blank) = Main A = Revision after main
Т	Temperature range (°C)	 V = -40 to 105 C = -40 to 85
PP	Package identifier	 FM = 32 QFN (5 mm x 5 mm) FT = 48 QFN (7 mm x 7 mm) LF = 48 LQFP (7 mm x 7 mm) LH = 64 LQFP (10 mm x 10 mm) MP = 64 MAPBGA (5 mm x 5 mm) LK = 80 LQFP (12 mm x 12 mm) LL = 100 LQFP (14 mm x 14 mm) MC = 121 MAPBGA (8 mm x 8 mm) LQ = 144 LQFP (20 mm x 20 mm) MD = 144 MAPBGA (13 mm x 13 mm) MJ = 256 MAPBGA (17 mm x 17 mm)
СС	Maximum CPU frequency (MHz)	 5 = 50 MHz 7 = 72 MHz 10 = 100 MHz 12 = 120 MHz 15 = 150 MHz
Ν	Packaging type	 R = Tape and reel (Blank) = Trays

2.4 Example

This is an example part number:

MK10DN512ZVMD10

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DD_VBAT}	Average current when CPU is not accessing RTC registers					10
	• @ 1.8V					
	• @ -40 to 25°C	_	0.71	0.81	μA	
	• @ 70°C	_	1.01	1.3	μA	
	• @ 105°C	_	2.82	4.3	μA	
	• @ 3.0V					
	• @ -40 to 25°C	_	0.84	0.94	μA	
	• @ 70°C	_	1.17	1.5	μA	
	• @ 105°C	_	3.16	4.6	μA	

Table 6. Power consumption operating behaviors (continued)

- 1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
- 3. 100MHz core and system clock, 50MHz bus and FlexBus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 4. Max values are measured with CPU executing DSP instructions.
- 5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz FlexBus and flash clock. MCG configured for FEI mode.
- 6. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 7. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 8. 2 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
- 9. Data reflects devices with 128 KB of RAM.
- 10. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at greater than 50 MHz frequencies.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL





Figure 2. Run mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors as measured on 144LQFP and 144MAPBGA packages

Symbol	Description	Frequency band (MHz)	144LQFP	144MAPBGA	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	23	12	dBµV	1,2
V _{RE2}	Radiated emissions voltage, band 2	50–150	27	24	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	28	27	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	14	11	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	К	К	—	2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions – TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- 2. $V_{DD} = 3.3 \text{ V}, T_A = 25 \text{ °C}, f_{OSC} = 12 \text{ MHz} \text{ (crystal)}, f_{SYS} = 96 \text{ MHz}, f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	_	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
Normal run mode					
f _{SYS}	System and core clock		100	MHz	
f _{BUS}	Bus clock	_	50	MHz	
FB_CLK	FlexBus clock	_	50	MHz	
f _{FLASH}	Flash clock	_	25	MHz	
f _{LPTMR}	LPTMR clock	_	25	MHz	

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CAN, CMT, and I²C signals.

6.1.2 JTAG electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	25	
	Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	—	ns
	JTAG and CJTAG	20	—	ns
	Serial Wire Debug	10	_	ns
J4	TCLK rise and fall times	_	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	_	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z		17	ns
J13	TRST assert time	100		ns
J14	TRST setup time (negation) to TCLK high	8		ns

Table 14. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
	Serial Wire Debug	0	40	
J2	TCLK cycle period	1/J1	_	ns
J3	TCLK clock pulse width			
	Boundary Scan	50	_	ns
	JTAG and CJTAG	25	_	ns
	Serial Wire Debug	12.5	—	ns
J4	TCLK rise and fall times		3	ns

Table continues on the next page...

Peripheral operating requirements and behaviors

Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	_	ns
J7	TCLK low to boundary scan output data valid	_	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	_	22.1	ns
J13	TRST assert time	100	_	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 14. JTAG full voltage range electricals (continued)



Figure 5. Test clock input timing



Figure 6. Boundary scan (JTAG) timing



Figure 7. Test Access Port timing





6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

Peripheral operating requirements and behaviors

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications Table 18. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{BAT}	Supply voltage	1.71	_	3.6	V
R _F	Internal feedback resistor		100	_	MΩ
C _{para}	Parasitical capacitance of EXTAL32 and XTAL32		5	7	pF
V _{pp} ¹	Peak-to-peak amplitude of oscillation		0.6	_	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32 kHz oscillator frequency specifications Table 19. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{osc_lo}	Oscillator crystal	—	32.768	_	kHz	
t _{start}	Crystal start-up time	—	1000		ms	1
f _{ec_extal32}	Externally provided input clock frequency	—	32.768	_	kHz	2
V _{ec_extal32}	Externally provided input clock amplitude	700		V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.

This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The
oscillator remains enabled and XTAL32 must be left unconnected.

3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT} .

6.4 Memories and memory interfaces

Peripheral operating requirements and behaviors

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	FB_CLK	MHz	
FB1	Clock period	20	_	ns	
FB2	Address, data, and control output valid	—	11.5	ns	1
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and FB_TA input setup	8.5	_	ns	2
FB5	Data and FB_TA input hold	0.5	—	ns	2

Table 25. Flexbus limited voltage range switching specifications

1. Specification is valid for all FB_AD[31:0], FB_BE/BWEn, FB_CSn, FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.

2. Specification is valid for all FB_AD[31:0] and FB_TA.

Table 26. Flexbus full voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation		FB_CLK	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	_	13.5	ns	1
FB3	Address, data, and control output hold	0	—	ns	1
FB4	Data and FB_TA input setup	13.7	_	ns	2
FB5	Data and FB_TA input hold	0.5		ns	2

1. Specification is valid for all FB_AD[31:0], FB_BE/BWEn, FB_CSn, FB_OE, FB_R/W, FB_TBST, FB_TSIZ[1:0], FB_ALE, and FB_TS.

2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB}_{-}\text{TA}}.$

6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in Table 27 and Table 28 are achievable on the differential pins ADCx_DP0, ADCx_DM0, ADCx_DP1, ADCx_DM1, ADCx_DP3, and ADCx_DM3.

The ADCx_DP2 and ADCx_DM2 ADC inputs are connected to the PGA outputs and are not direct device pins. Accuracy specifications for these pins are defined in Table 29 and Table 30.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
V _{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV_{DDA}	Supply voltage	Delta to V _{DD} (V _{DD} - V _{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V _{SS} (V _{SS} - V _{SSA})	-100	0	+100	mV	2
V _{REFH}	ADC reference voltage high		1.13	V _{DDA}	V _{DDA}	V	
V _{REFL}	ADC reference voltage low		V _{SSA}	V _{SSA}	V _{SSA}	V	
V _{ADIN}	Input voltage	16-bit differential mode	VREFL	_	31/32 * VREFH	V	
		All other modes	VREFL	—	VREFH		
C _{ADIN}	Input capacitance	16-bit mode	—	8	10	pF	
		 8-bit / 10-bit / 12-bit modes 	_	4	5		
R _{ADIN}	Input resistance		—	2	5	kΩ	
R _{AS}	Analog source resistance	13-bit / 12-bit modes f _{ADCK} < 4 MHz	_	_	5	kΩ	3
f _{ADCK}	ADC conversion clock frequency	≤ 13-bit mode	1.0		18.0	MHz	4
f _{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	_	12.0	MHz	4
C _{rate}	ADC conversion	≤ 13-bit modes					5
	rate	No ADC hardware averaging	20.000	—	818.330	Ksps	
		Continuous conversions enabled, subsequent conversion time					

6.6.1.1 16-bit ADC operating conditions Table 27. 16-bit ADC operating conditions

Table continues on the next page...

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	16-bit mode					5
	rate	No ADC hardware averaging	37.037	_	461.467	Ksps	
		Continuous conversions enabled, subsequent conversion time					

 Table 27.
 16-bit ADC operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
- 2. DC potential difference.
- This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
- 4. To use the maximum ADC conversion clock frequency, the ADHSC bit must be set and the ADLPC bit must be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.



Figure 12. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 28. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215		1.7	mA	3

Table continues on the next page ...

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
G	Gain ⁴	• PGAG=0	0.95	1	1.05		$R_{AS} < 100\Omega$
		• PGAG=1	1.9	2	2.1		
		• PGAG=2	3.8	4	4.2		
		• PGAG=3	7.6	8	8.4		
		• PGAG=4	15.2	16	16.6		
		• PGAG=5	30.0	31.6	33.2		
		• PGAG=6	58.8	63.3	67.8		
BW	Input signal	16-bit modes	_	—	4	kHz	
	bandwidth	 < 16-bit modes 	_	_	40	kHz	
PSRR	Power supply rejection ratio	Gain=1	-	-84		dB	V _{DDA} = 3V ±100mV, f _{VDDA} = 50Hz, 60Hz
CMRR	Common mode	Gain=1	_	-84		dB	V _{CM} =
	rejection ratio	• Gain=64	-	-85	_	dB	f _{VCM} = 50Hz, 100Hz
V _{OFS}	Input offset voltage		-	0.2	_	mV	Output offset = V _{OFS} *(Gain+1)
T _{GSW}	Gain switching settling time		_	_	10	μs	5
E _{IL}	Input leakage error	All modes		$I_{ln} \times R_{AS}$		mV	I _{In} = leakage current
							(refer to the MCU's voltage and current operating ratings)
V _{PP,DIFF}	Maximum differential input		$\left(\frac{(\min(v))}{(v)}\right)$	(x,V _{DDA} –V _x) Gain	-0.2)×4)	V	6
	signal swing		where V	x = V _{REFPG}	_A × 0.583		
SNR	Signal-to-noise	• Gain=1	80	90		dB	16-bit
	ratio	• Gain=64	52	66	_	dB	differential mode, Average=32
THD	Total harmonic	Gain=1	85	100	—	dB	16-bit
	distortion	• Gain=64	49	95		dB	differential mode, Average=32, f _{in} =100Hz
SFDR	Spurious free	• Gain=1	85	105		dB	16-bit
	uynamic range	• Gain=64	53	88		dB	Average=32, f _{in} =100Hz

Table 30. 16-bit ADC with PGA characteristics (continued)

Table continues on the next page...

6.6.3.2 12-bit DAC operating behaviors Table 33. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL}	Supply current — low-power mode	—	_	150	μΑ	
I _{DDA_DACH} P	Supply current — high-speed mode	_	—	700	μΑ	
tDACLP	Full-scale settling time (0x080 to 0xF7F) — low-power mode	_	100	200	μs	1
tDACHP	Full-scale settling time (0x080 to 0xF7F) — high-power mode		15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	_	_	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	—	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V _{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	—	—	±1	LSB	4
V _{OFFSET}	Offset error	_	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	_	3.7	_	μV/C	6
T _{GE}	Temperature coefficient gain error	_	0.000421	_	%FSR/C	
Rop	Output resistance load = $3 \text{ k}\Omega$	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	Low power (SP _{LP})	0.05	0.12	—		
СТ	Channel to channel cross talk	_	—	-80	dB	
BW	3dB bandwidth				kHz	
	• High power (SP _{HP})	550	_	—		
	Low power (SP _{LP})	40	-	—		

1. Settling within ±1 LSB

- 2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV
- 4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
- 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} 100 mV
- V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

6. C_b = total capacitance of the one bus line in pF.



Figure 23. Timing definition for fast and standard mode devices on the I²C bus

6.8.5 UART switching specifications

See General switching specifications.

6.8.6 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Num	Symbol	Description	Min.	Max.	Unit	
SD1	fpp	Clock frequency (low speed)	0	400	kHz	
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz	
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz	
	f _{OD}	Clock frequency (identification mode)	0	400	kHz	
SD2	t _{WL}	Clock low time	7	—	ns	
SD3	t _{WH}	Clock high time	7	—	ns	
SD4	t _{TLH}	Clock rise time	—	3	ns	
SD5	t _{THL}	Clock fall time	_	3	ns	
		SDHC output / card inputs SDHC_CMD, SDHC_DAT	(reference to	SDHC_CLK)		
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns	
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)					
SD7	t _{ISU}	SDHC input setup time	5	—	ns	
SD8	t _{IH}	SDHC input hold time	0	—	ns	

Table 43. SDHC switching specifications





Figure 24. SDHC timing

6.8.7 I²S switching specifications

This section provides the AC timings for the I²S in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (TCR[TSCKP] = 0, RCR[RSCKP] = 0) and a non-inverted frame sync (TCR[TFSI] = 0, RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (I2S_BCLK) and/or the frame sync (I2S_FS) shown in the figures below.

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
S1	I2S_MCLK cycle time	2 x t _{SYS}		ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_BCLK cycle time	5 x t _{SYS}	—	ns
S4	I2S_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_BCLK to I2S_FS output valid	—	15	ns
S6	I2S_BCLK to I2S_FS output invalid	-2.5	—	ns
S7	I2S_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_BCLK to I2S_TXD invalid	-3	_	ns
S9	I2S_RXD/I2S_FS input setup before I2S_BCLK	20	—	ns
S10	I2S_RXD/I2S_FS input hold after I2S_BCLK	0		ns

Table 44. I²S master mode timing (limited voltage range)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number				
100-pin LQFP	98ASS23308W				

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	PTE0	ADC1_SE4a	ADC1_SE4a	PTE0	SPI1_PCS1	UART1_TX	SDHC0_D1		I2C1_SDA		
2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX	SDHC0_D0		I2C1_SCL		
3	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_CTS_b	SDHC0_DCLK				
4	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_RTS_b	SDHC0_CMD				
5	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	UART3_TX	SDHC0_D3				
6	PTE5	DISABLED		PTE5	SPI1_PCS2	UART3_RX	SDHC0_D2				
7	PTE6	DISABLED		PTE6	SPI1_PCS3	UART3_CTS_b	I2S0_MCLK		I2S0_CLKIN		
8	VDD	VDD	VDD								
9	VSS	VSS	VSS								
10	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
11	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPT0_ALT3		
12	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
13	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				

100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
14	ADC0_DP1	ADC0_DP1	ADC0_DP1								
15	ADC0_DM1	ADC0_DM1	ADC0_DM1								
16	ADC1_DP1	ADC1_DP1	ADC1_DP1								
17	ADC1_DM1	ADC1_DM1	ADC1_DM1								
18	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3	PGA0_DP/ ADC0_DP0/ ADC1_DP3								
19	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3	PGA0_DM/ ADC0_DM0/ ADC1_DM3								
20	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
21	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
22	VDDA	VDDA	VDDA								
23	VREFH	VREFH	VREFH								
24	VREFL	VREFL	VREFL								
25	VSSA	VSSA	VSSA								
26	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
27	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
28	XTAL32	XTAL32	XTAL32								
29	EXTAL32	EXTAL32	EXTAL32								
30	VBAT	VBAT	VBAT								
31	PTE24	ADC0_SE17	ADC0_SE17	PTE24	CAN1_TX	UART4_TX			EWM_OUT_b		
32	PTE25	ADC0_SE18	ADC0_SE18	PTE25	CAN1_RX	UART4_RX			EWM_IN		
33	PTE26	DISABLED		PTE26		UART4_CTS_b			RTC_CLKOUT		
34	PTAO	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
35	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
36	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
37	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UART0_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
38	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
39	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT	I2S0_RX_BCLK	JTAG_TRST	
40	VDD	VDD	VDD								

K10 Sub-Family Data Sheet Data Sheet, Rev. 7, 02/2013.

Pinout

Pinout

100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
99	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0		
100	PTD7			PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Rev. No.	Date	Substantial Changes					
3	3/2011	Added sections that were inadvertently removed in previous revision					
4	3/2011	Reworded IIC footnote in "Voltage and Current Operating Requirements" table.					
		Added paragraph to "Peripheral operating requirements and behaviors" section.					
		Added "JTAG full voltage range electricals" table to the "JTAG electricals" section.					
5	6/2011	 Added 'TAG' full voltage range electricals' table to the 'TAG' electricals' section. Changed bC injection current specs in "Voltage and current operating requirements" table Changed Input leakage current and internal pullup/pulldown resistor specs in "Voltage and current operating behaviors" table Split Low power stop mode current specs by temperature range in "Power consumption operating behaviors" table Changed Uprical (D_D, V_{BAT} spec in "Power consumption operating behaviors" table Added LPTMR clock specs to "Device clock specifications' table Changed Minimum external reset pulse width in "General switching specifications" table Changed Alcock specs to "Device clock specifications" table Changed Alcock specs to "Device clock specifications" table Changed PLL operating current in "MCG specifications" table Changed Crystal startup time in "Oscillator DC electrical specifications" table Changed Crystal startup time in "Oscillator frequency specifications" table Changed dille of "FlexBus switching specifications" table Changed ADC asynchronous clock source specs in "16-bit ADC characteristics" table Changed ADC asynchronous clock source specs in "16-bit ADC with PGA characteristics" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications" table Changed Analog comparator initialization delay in "Comparator and 6-bit DAC electrical specifications"					
6	01/2012	 Added AC electrical specifications. Replaced TBDs with silicon data throughout. In "Power mode transition operating behaviors" table, removed entry times. Updated "EMC radiated emissions operating behaviors" to remove SAE level and also added data for 144LQFP. Clarified "EP7" in "EzPort switching specifications" table and "EzPort Timing Diagram". Added "ENOB vs. ADC_CLK for 16-bit differential and 16-bit single-ended modes" figures. Updated I_{DD_RUN} numbers in 'Power consumption operating behaviors' section. Clarified 'Diagram: Typical IDD_RUN operating behavior' section and updated 'Run mode supply current vs. core frequency — all peripheral clocks disabled' figure. In 'Voltage reference electrical specifications' section, updated C_L, V_{tdrift}, and V_{vdrift} values. 					

Table 49. Revision History (continued)

Table continues on the next page...