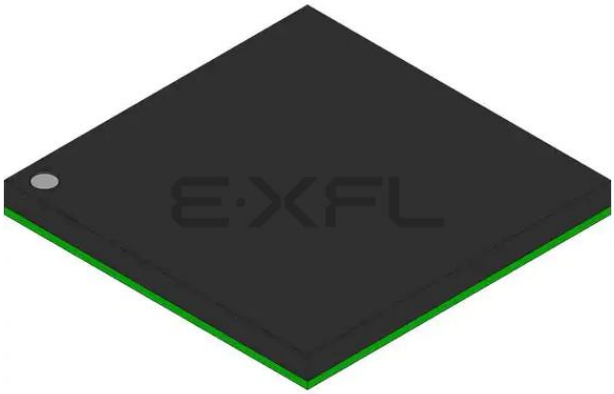


Welcome to E-XFL.COM

Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	200MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 100°C
Mounting Type	Surface Mount
Package / Case	196-LBGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56321vf200

Table 1. DSP56321 Features (Continued)

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>Internal Memories</td><td>
• 192 × 24-bit bootstrap ROM
• 192 K × 24-bit RAM total
• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:
<table>
<tr><th>Program RAM Size</th><th>Instruction Cache Size</th><th>X Data RAM Size*</th><th>Y Data RAM Size*</th><th>Instruction Cache</th><th>MSW2</th><th>MSW1</th><th>MSW0</th></tr>
<tr><td>32 K × 24-bit</td><td>0</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>31 K × 24-bit</td><td>1024 × 24-bit</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>40 K × 24-bit</td><td>0</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>39 K × 24-bit</td><td>1024 × 24-bit</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48 K × 24-bit</td><td>0</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>47 K × 24-bit</td><td>1024 × 24-bit</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>64 K × 24-bit</td><td>0</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>63 K × 24-bit</td><td>1024 × 24-bit</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>72 K × 24-bit</td><td>0</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>71 K × 24-bit</td><td>1024 × 24-bit</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>80 K × 24-bit</td><td>0</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>79 K × 24-bit</td><td>1024 × 24-bit</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>96 K × 24-bit</td><td>0</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>95 K × 24-bit</td><td>1024 × 24-bit</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>112 K × 24-bit</td><td>0</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>111 K × 24-bit</td><td>1024 × 24-bit</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="8">*Includes 12 K × 24-bit shared memory (that is, 24 K total memory shared by the core and the EFCOP)</td></tr>
</table>
</td></tr>
<tr><td>External Memory Expansion</td><td>
• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines
• Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines
• External memory expansion port
• Chip select logic for glueless interface to static random access memory (SRAMs)
</td></tr>
<tr><td>Power Dissipation</td><td>
• Very low-power CMOS design
• Wait and Stop low-power standby modes
• Fully static design specified to operate down to 0 Hz (dc)
• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
</td></tr>
<tr><td>Packaging</td><td>
• Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.
</td></tr>
</table>

Target Applications

DSP56321 applications require high performance, low power, small packaging, and a large amount of internal memory. The EFCOP can accelerate general filtering applications. Examples include:

- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- Security encryption systems
- Home entertainment systems
- DSP resource boards
- High-speed modem banks
- IP telephony

1.4 External Memory Expansion Port (Port A)

Note: When the DSP56321 enters a low-power standby mode (stop or wait), it releases bus mastership and tri-states the relevant Port A signals: A[0–17], D[0–23], AA[0–3], $\overline{RD}$, $\overline{WR}$, $\overline{BB}$.

1.4.1 External Address Bus

Table 1-5. External Address Bus Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
A[0–17]	Output	Tri-stated	**Address Bus**—When the DSP is the bus master, A[0–17] are active-high outputs that specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–17] do not change state when external memory spaces are not being accessed.

1.4.2 External Data Bus

Table 1-6. External Data Bus Signals

Signal Name	Type	State During Reset	State During Stop or Wait	Signal Description
D[0–23]	Input/ Output	Ignored Input	Last state: *Input*: Ignored *Output*: Last value	**Data Bus**—When the DSP is the bus master, D[0–23] are active-high, bidirectional input/outputs that provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] drivers are tri-stated. If the last state is output, these lines have weak keepers to maintain the last output state if all drivers are tri-stated.

1.4.3 External Bus Control

Table 1-7. External Bus Control Signals

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
AA[0–3]	Output	Tri-stated	**Address Attribute**—When defined as AA, these signals can be used as chip selects or additional address lines. The default use defines a priority scheme under which only one AA signal can be asserted at a time. Setting the AA priority disable (APD) bit (Bit 14) of the Operating Mode Register, the priority mechanism is disabled and the lines can be used together as four external lines that can be decoded externally into 16 chip select signals.
$\overline{RD}$	Output	Tri-stated	**Read Enable**—When the DSP is the bus master, $\overline{RD}$ is an active-low output that is asserted to read external memory on the data bus (D[0–23]). Otherwise, $\overline{RD}$ is tri-stated.
$\overline{WR}$	Output	Tri-stated	**Write Enable**—When the DSP is the bus master, $\overline{WR}$ is an active-low output that is asserted to write external memory on the data bus (D[0–23]). Otherwise, the signals are tri-stated.

1.5 Interrupt and Mode Control

The interrupt and mode control signals select the chip operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 1-8. Interrupt and Mode Control

Signal Name	Type	State During Reset	Signal Description
MODA	Input	Schmitt-trigger Input	**Mode Select A**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the RESET signal is deasserted.
IRQA	Input		**External Interrupt Request A**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the STOP or WAIT standby state and IRQA is asserted, the processor exits the STOP or WAIT state.
MODB	Input	Schmitt-trigger Input	**Mode Select B**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the RESET signal is deasserted.
IRQB	Input		**External Interrupt Request B**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and IRQB is asserted, the processor exits the WAIT state.
MODC	Input	Schmitt-trigger Input	**Mode Select C**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the RESET signal is deasserted.
IRQC	Input		**External Interrupt Request C**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and IRQC is asserted, the processor exits the WAIT state.
MODD	Input	Schmitt-trigger Input	**Mode Select D**—MODA, MODB, MODC, and MODD select one of 16 initial chip operating modes, latched into the Operating Mode Register when the RESET signal is deasserted.
IRQD	Input		**External Interrupt Request D**—After reset, this input becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input during normal instruction processing. If the processor is in the WAIT standby state and IRQD is asserted, the processor exits the WAIT state.
RESET	Input	Schmitt-trigger Input	**Reset**—Places the chip in the Reset state and resets the internal phase generator. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted after powerup.
PINIT	Input	Schmitt-trigger Input	**PLL Initial**—During assertion of RESET, the value of PINIT determines whether the DPLL is enabled or disabled.
NMI	Input		**Nonmaskable Interrupt**—After RESET deassertion and during normal instruction processing, this Schmitt-trigger input is the negative-edge-triggered NMI request.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	44	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	25	°C/W
Junction-to-ambient, @200 ft/min air flow, single-layer board (1s)[1,3]	$R_{\theta JMA}$	35	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	13	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	7	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage[1]: • Core (V_{CCQL}) • I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		 1.5 3.0	 1.6 3.3	 1.7 3.6	 V V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD/$\overline{IRQ}$[2] $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CCQH}$	 — — —	 $V_{CCQH} + 0.3$ $V_{CCQH} + 0.3$ V_{CCQH}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CCQH}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[8] • TTL (I_{OH} = –0.4 mA)[6] • CMOS (I_{OH} = –10 µA)[6]	V_{OH}	 2.4 $V_{CCQH} - 0.01$	 — —	 — —	 V V
Output low voltage[8] • TTL (I_{OL} = 3.0 mA)[6] • CMOS (I_{OL} = 10 µA)[6]	V_{OL}	 — —	 — —	 0.4 0.01	 V V

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.
2. This timing depends on several settings:
   • For DPLL disable, using internal oscillator (DPLL Control Register (PCTL) Bit 2 = 0) and oscillator disabled during Stop (PCTL Bit 1 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For DPLL disable, using internal oscillator (PCTL Bit 2 = 0) and oscillator enabled during Stop (PCTL Bit 1 = 1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For DPLL disable, using external clock (PCTL Bit 2 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 1 and Operating Mode Register Bit 6 settings.
   • For DPLL enable, if PCTL Bit 1 is 0, the DPLL is shut down during Stop. Recovering from Stop requires the DPLL to lock. The DPLL lock procedure duration is defined in **Table 2-6** and will be refined after silicon characterization. This procedure is followed by the stop delay counter. Stop recovery ends when the stop delay counter completes its count.
   • The DPLT value for DPLL disable is 0.
3. Periodically sampled and not 100 percent tested.
4. For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. V_{CCQH} = 3.3 V ±0.3 V, V_{CCQL} = 1.6 V ±0.1 V; T_J = –40°C to +100°C, C_L = 50 pF.
6. WS = number of wait states (measured in clock cycles, number of T_C).
7. Use the expression to compute a maximum value.

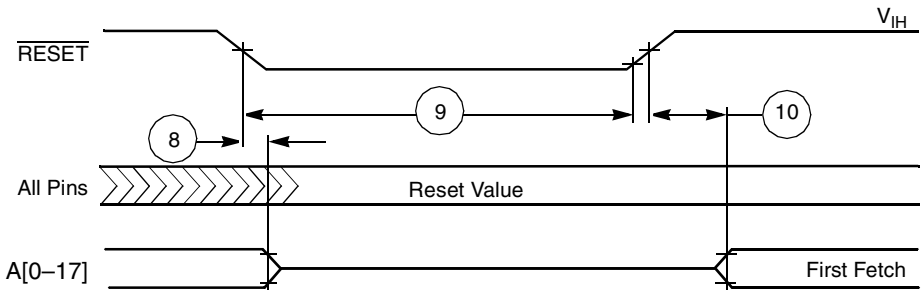
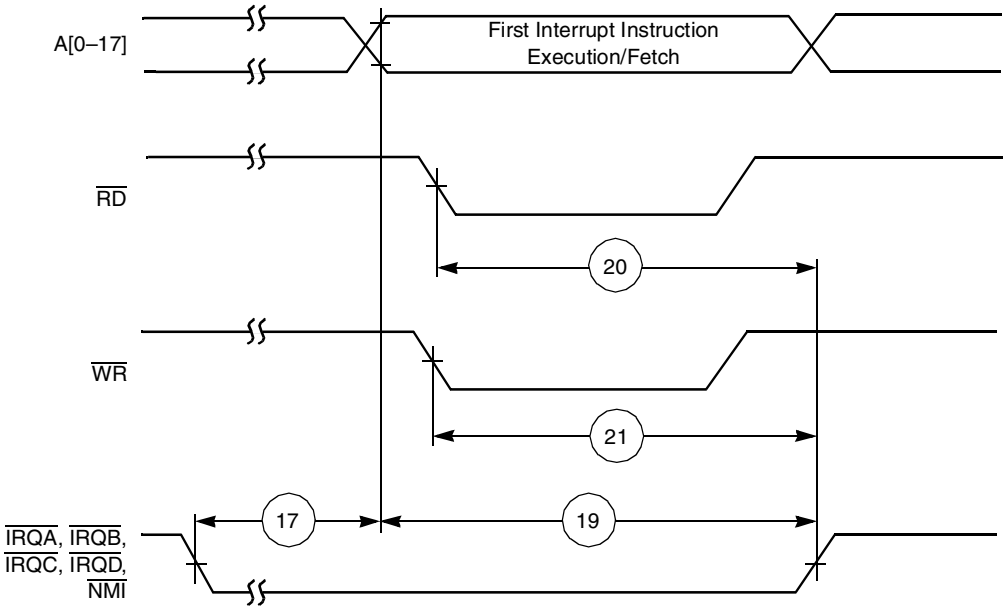
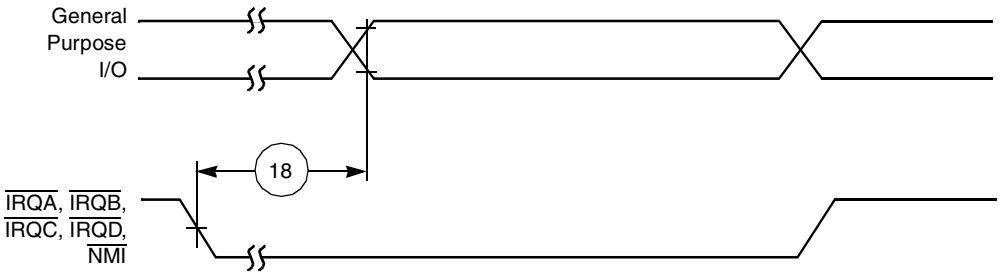


Figure 2-3. Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

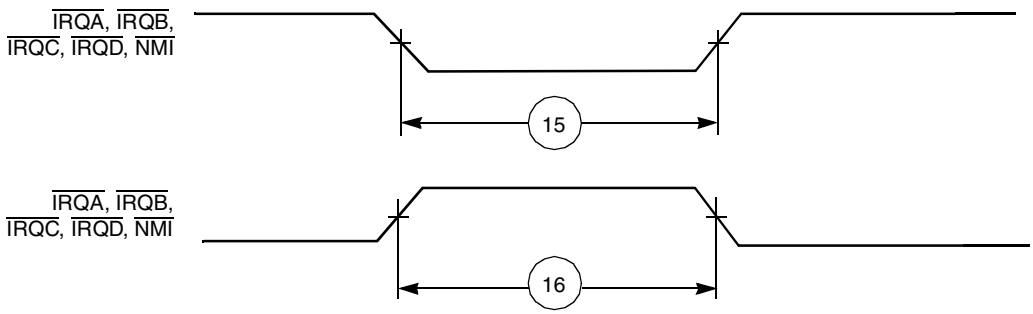
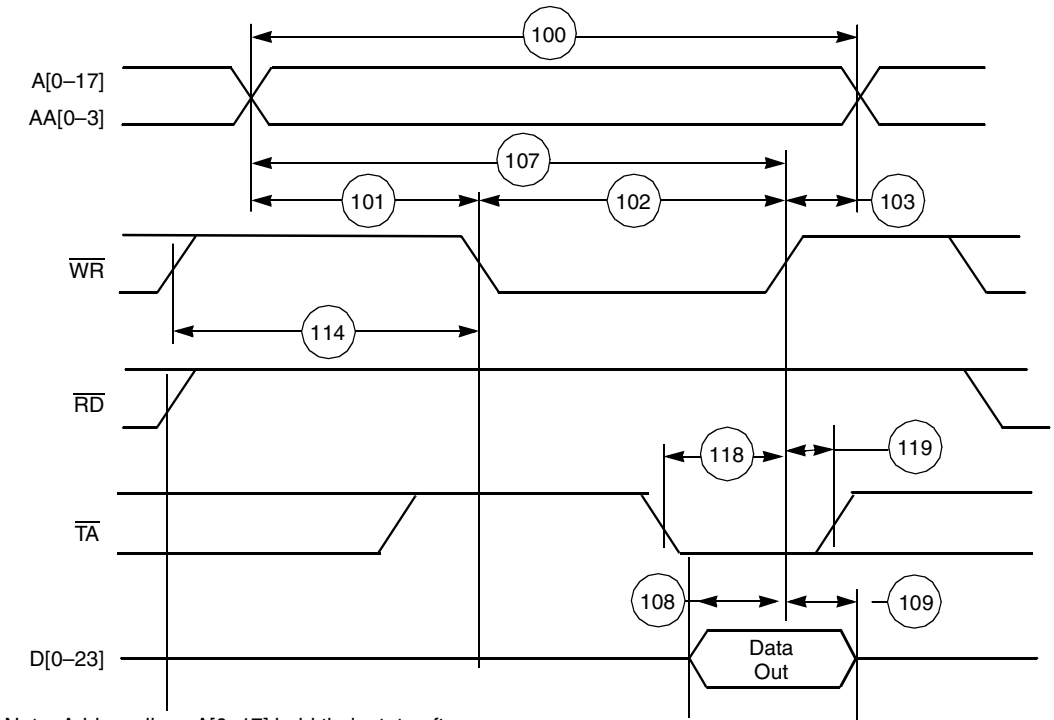


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-11. SRAM Write Access

2.4.5.2 Asynchronous Bus Arbitration Timings

Table 2-9. Asynchronous Bus Timings

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 Mhz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion.	2.5 × Tc + 5	—	17.5	—	16.4	—	15.4	—	14.1	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 × Tc + 5	15	—	14.1	—	13.3	—	12.27	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enable Asynchronous Arbitration mode.
2. To guarantee timings 250 and 251, it is recommended that you assert non-overlapping $\overline{BG}$ inputs to different DSP56300 devices (on the same bus), as shown in **Figure 2-12**, where $\overline{BG1}$ is the $\overline{BG}$ signal for one DSP56300 device while $\overline{BG2}$ is the $\overline{BG}$ signal for a second DSP56300 device.

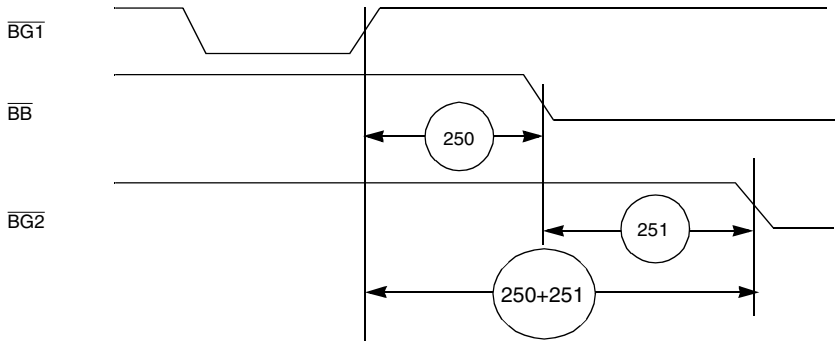


Figure 2-12. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal synchronization circuits on $\overline{BG}$ and $\overline{BB}$ inputs. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part may assume mastership and assert $\overline{BB}$, for some time after $\overline{BG}$ is deasserted. This is the reason for timing 250.

Once $\overline{BB}$ is asserted, there is a synchronization delay from $\overline{BB}$ assertion to the time this assertion is exposed to other DSP56300 components that are potential masters on the same bus. If $\overline{BG}$ input is asserted before that time, and $\overline{BG}$ is asserted and $\overline{BB}$ is deasserted, another DSP56300 component may assume mastership at the same time. Therefore, some non-overlap period between one $\overline{BG}$ input active to another $\overline{BG}$ input active is required. Timing 251 ensures that overlaps are avoided.

2.4.6 Host Interface Timing

Table 2-10. Host Interface Timings[1,2,12]

No.	Characteristic[10]	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
317	Read data strobe assertion width[5] $\overline{HACK}$ assertion width	$T_C + 4.95$	9.95	—	9.05	—	8.3	—	7.77	—	ns
318	Read data strobe deassertion width[5] $\overline{HACK}$ deassertion width		4.95	—	4.5	—	4.13	—	4.0	—	ns
319	Read data strobe deassertion width[5] after "Last Data Register" reads[8,11], or between two consecutive CVR, ICR, or ISR reads[3] $\overline{HACK}$ deassertion width after "Last Data Register" reads[8,11]	$2.5 \times T_C + 3.3$	15.8	—	14.7	—	13.7	—	12.39	—	ns
320	Write data strobe assertion width[6]		6.6	—	6.0	—	5.5	—	5.1	—	ns
321	Write data strobe deassertion width[8] $\overline{HACK}$ write deassertion width • after ICR, CVR and "Last Data Register" writes	$2.5 \times T_C + 3.3$	15.8	—	14.7	—	13.7	—	12.39	—	ns
	• after IVR writes, or after TXH:TXM:TXL writes (with HLEND= 0), or after TXL:TXM:TXH writes (with HLEND = 1)		8.25	—	7.5	—	6.88	—	6.28	—	ns
322	$\overline{HAS}$ assertion width		4.95	—	4.5	—	4.13	—	4.0	—	ns

Table 2-10. Host Interface Timings[1,2,12] (Continued)

No.	Characteristic[10]	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	

Notes:
1. See the Programmer's Model section in the chapter on the HI08 in the *DSP56321 Reference Manual*.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. This timing is applicable only if two consecutive reads from one of these registers are executed.
4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8. The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Big Endian mode (HLEND = 0; HLEND is the Interface Control Register bit 7—ICR[7]), or RXH/TXH in the Little Endian mode (HLEND = 1).
9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10. V_{CCQH} = 3.3 V ± 0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
12. After the external host writes a new value to the ICR, the HI08 will be ready for operation after three DSP clock cycles (3 × Tc).

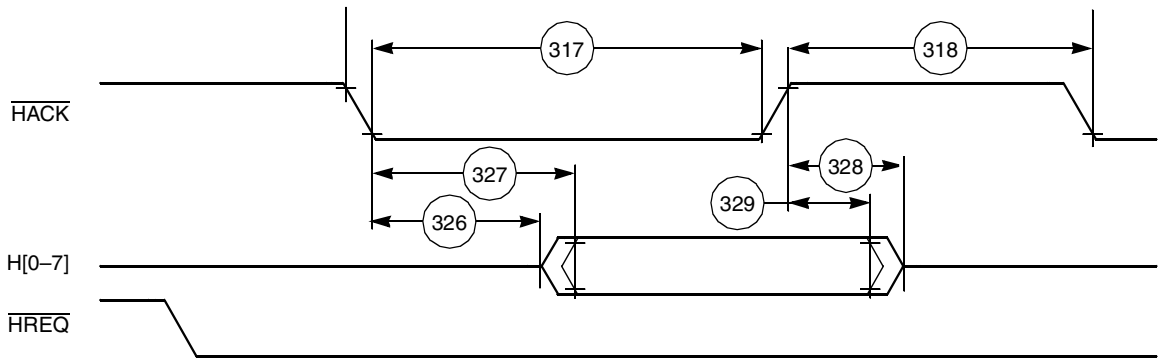


Figure 2-13. Host Interrupt Vector Register (IVR) Read Timing Diagram

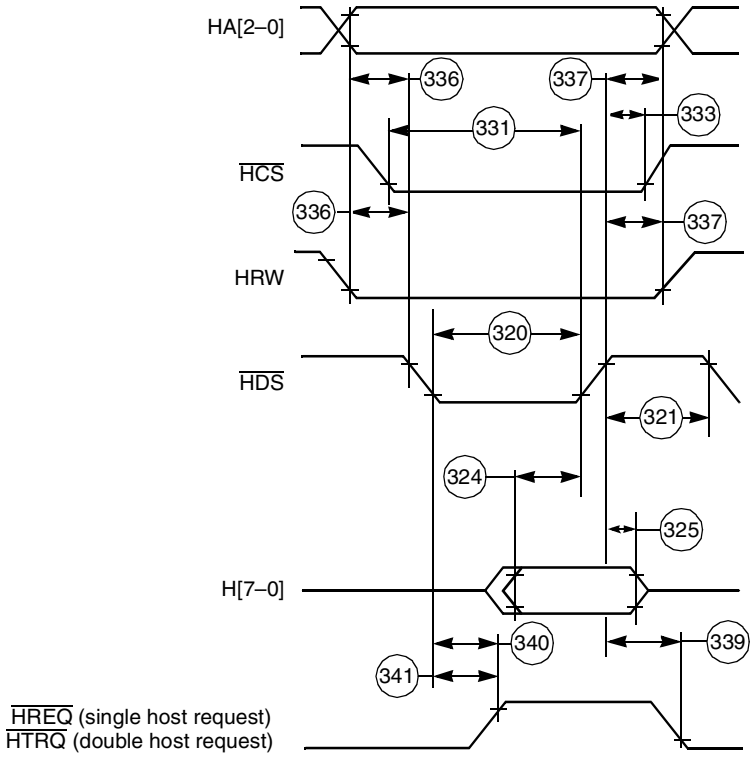


Figure 2-16. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

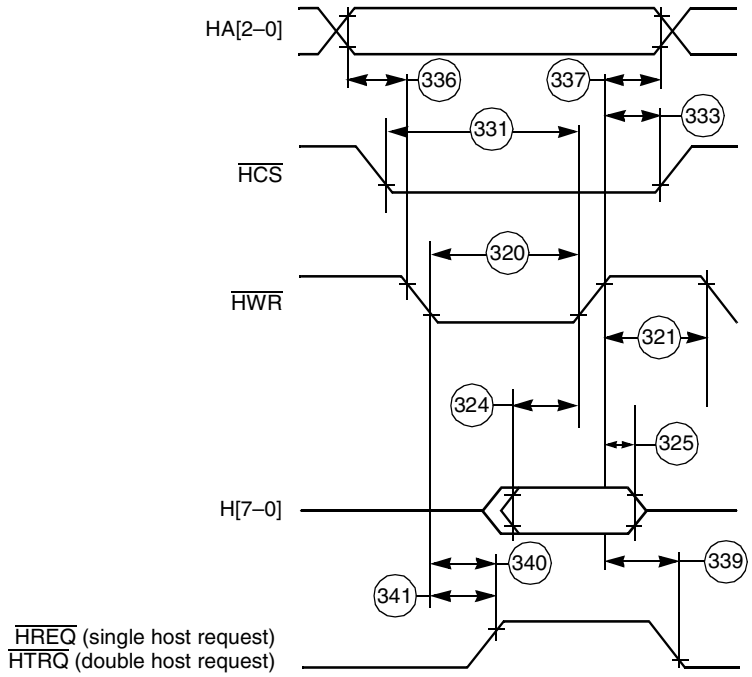


Figure 2-17. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

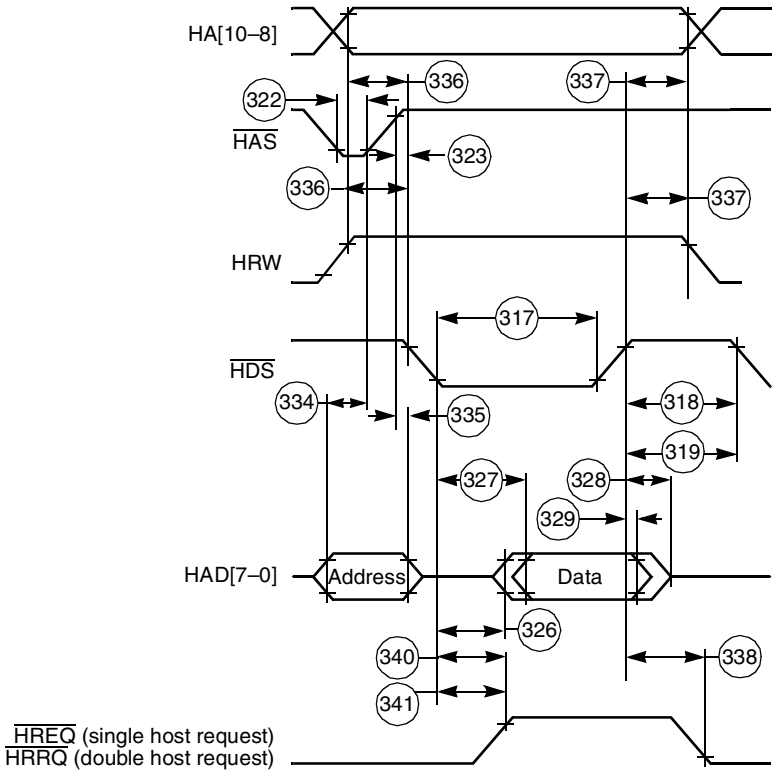


Figure 2-18. Read Timing Diagram, Multiplexed Bus, Single Data Strobe

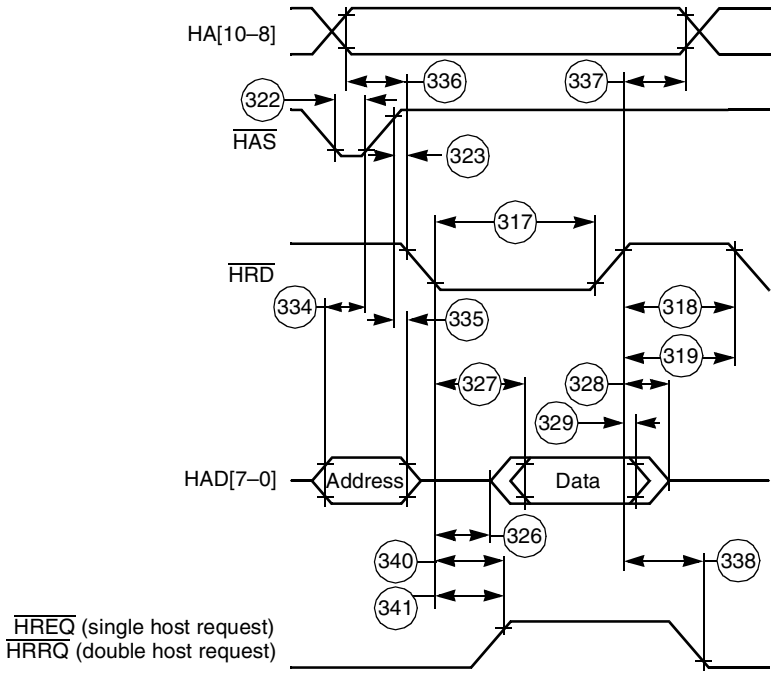
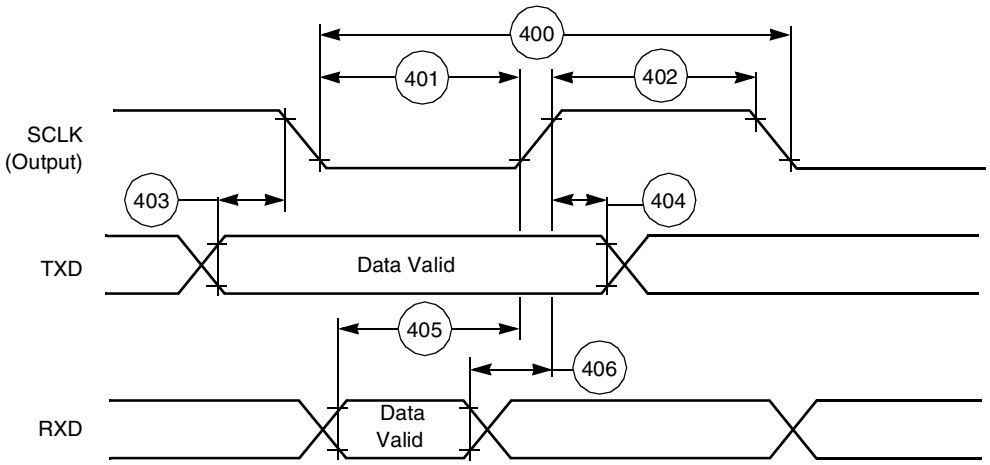
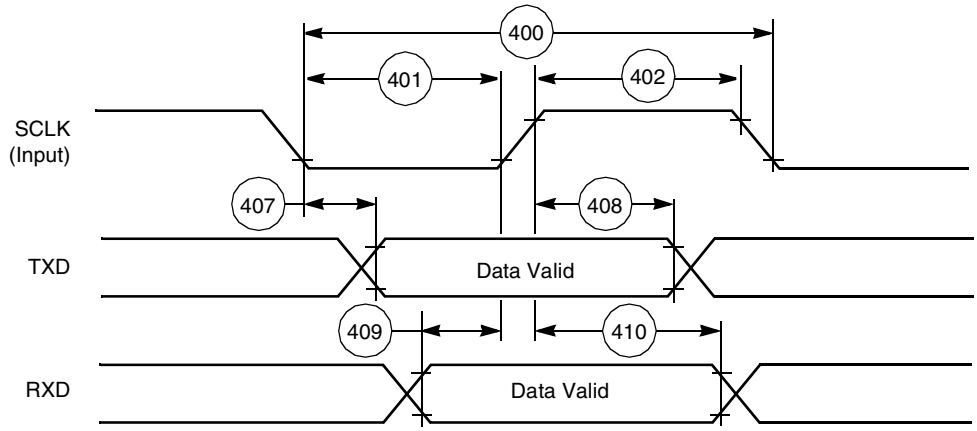


Figure 2-19. Read Timing Diagram, Multiplexed Bus, Double Data Strobe



a) Internal Clock



b) External Clock

Figure 2-22. SCI Synchronous Mode Timing

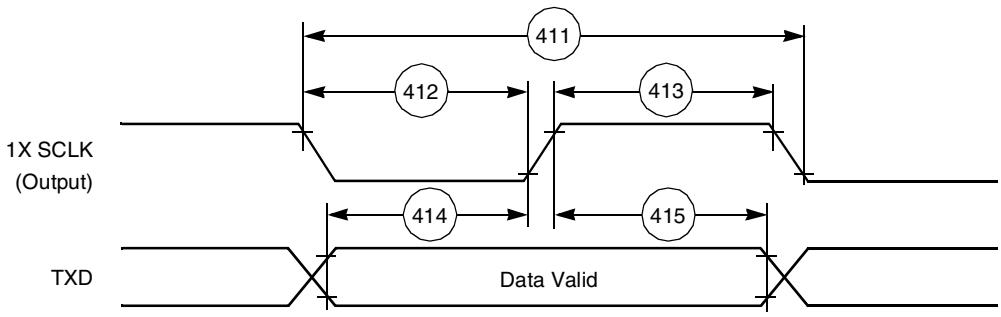


Figure 2-23. SCI Asynchronous Mode Timing

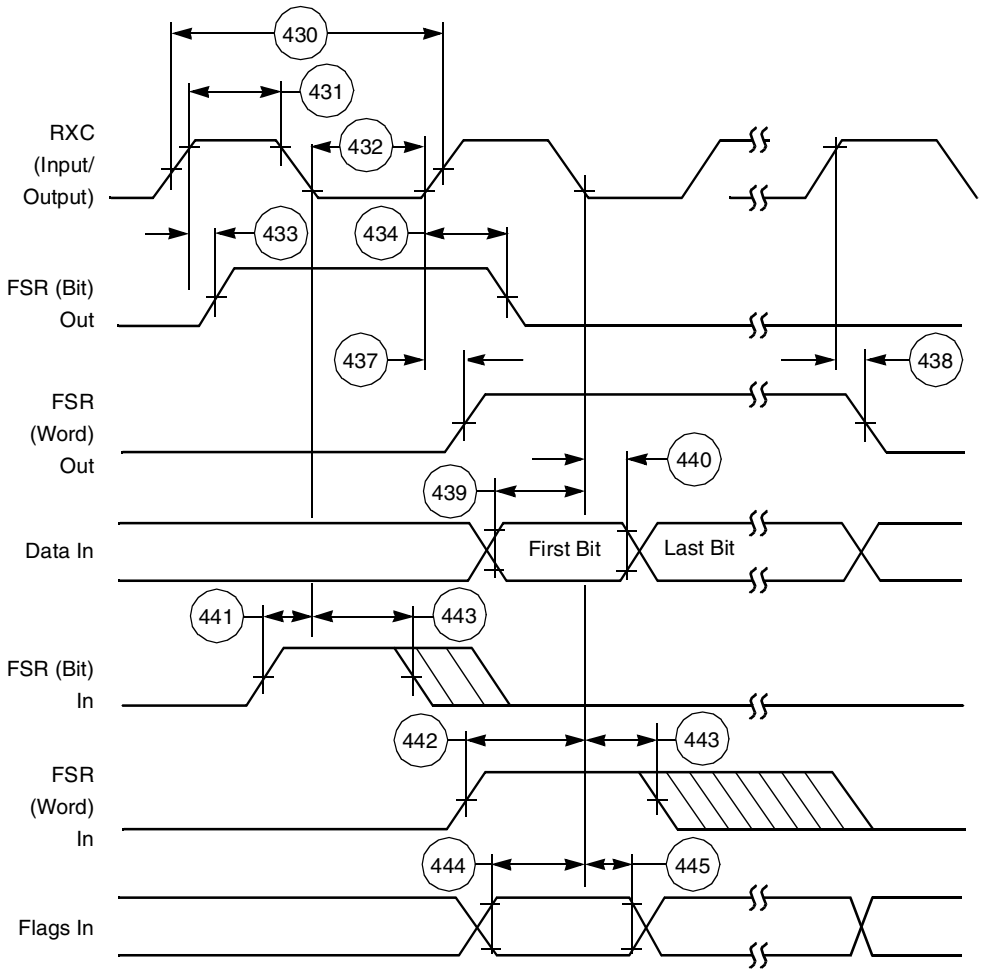


Figure 2-25. ESSI Receiver Timing

2.4.9 Timer Timing

Table 2-13. Timer Timings

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		240 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	12.0	—	11.1	—	10.3	—	9.27	—	ns
481	TIO High	$2 \times T_C + 2.0$	12.0	—	11.1	—	10.3	—	9.27	—	ns
486	Synchronous delay time from Timer input rising edge to the external memory address out valid caused by the first interrupt instruction execution	$10.25 \times T_C + 10.0$	61.25	—	56.64	—	52.74	—	47.27	—	ns

Notes:
1. V_{CCQH} = 3.3 V ±0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
2. The maximum frequency of pulses generated by a timer will be defined after device characterization is completed.
3. In the timing diagrams below, TIO is drawn using the rising edge as the reference. TIO polarity is programmable in the Timer Control/Status Register (TCSR). Refer to the *DSP56321 Reference Manual* for details.

2.4.11 JTAG Timing

Table 2-14. JTAG Timing

No.	Characteristics	All frequencies		Unit
		Min	Max	
500	TCK frequency of operation (1/(T_C × 3); absolute maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	—	ns
502	TCK clock pulse width measured at 1.6 V	20.0	—	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	—	ns
505	Boundary scan input data hold time	24.0	—	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	—	ns
509	TMS, TDI data hold time	25.0	—	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	$\overline{\text{TRST}}$ assert time	100.0	—	ns
513	$\overline{\text{TRST}}$ setup time to TCK low	40.0	—	ns

Notes:
1. V_{CCQH} = 3.3 V ± 0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF.
2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.

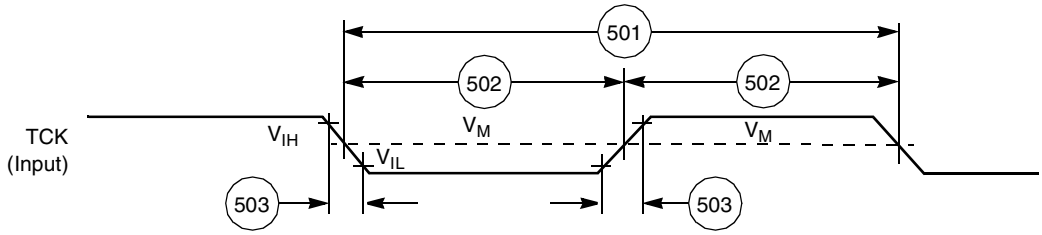


Figure 2-28. Test Clock Input Timing Diagram

2.4.12 OnCE Module TimIng

Table 2-15. OnCE Module Timing

No.	Characteristics	Expression	All Frequencies		Unit
			Min	Max	
500	TCK frequency of operation (1/(T_C × 3); maximum 22 MHz)	Max 22.0 MHz	0.0	22.0	MHz
514	$\overline{DE}$ assertion time in order to enter Debug mode	1.5 × T_C + 10.0	20.0	—	ns
515	Response time when DSP56321 is executing NOP instructions from internal memory	5.5 × T_C + 30.0	—	67.0	ns
516	Debug acknowledge assertion time	3 × T_C + 5.0	25.0	—	ns
Note:	V_{CCQH} = 3.3 V ± 0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF				

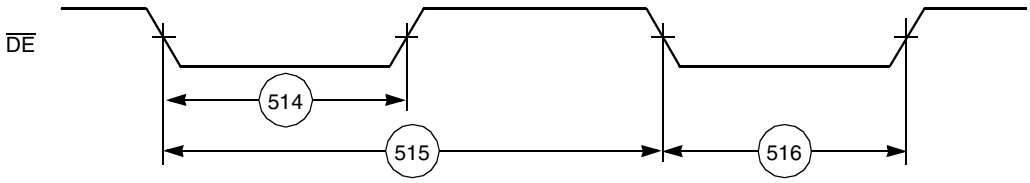


Figure 2-32. OnCE—Debug Request

3.1 Package Description

Top and bottom views of the MAP-BGA packages are shown in **Figure 3-1** and **Figure 3-2** with their pin-outs.

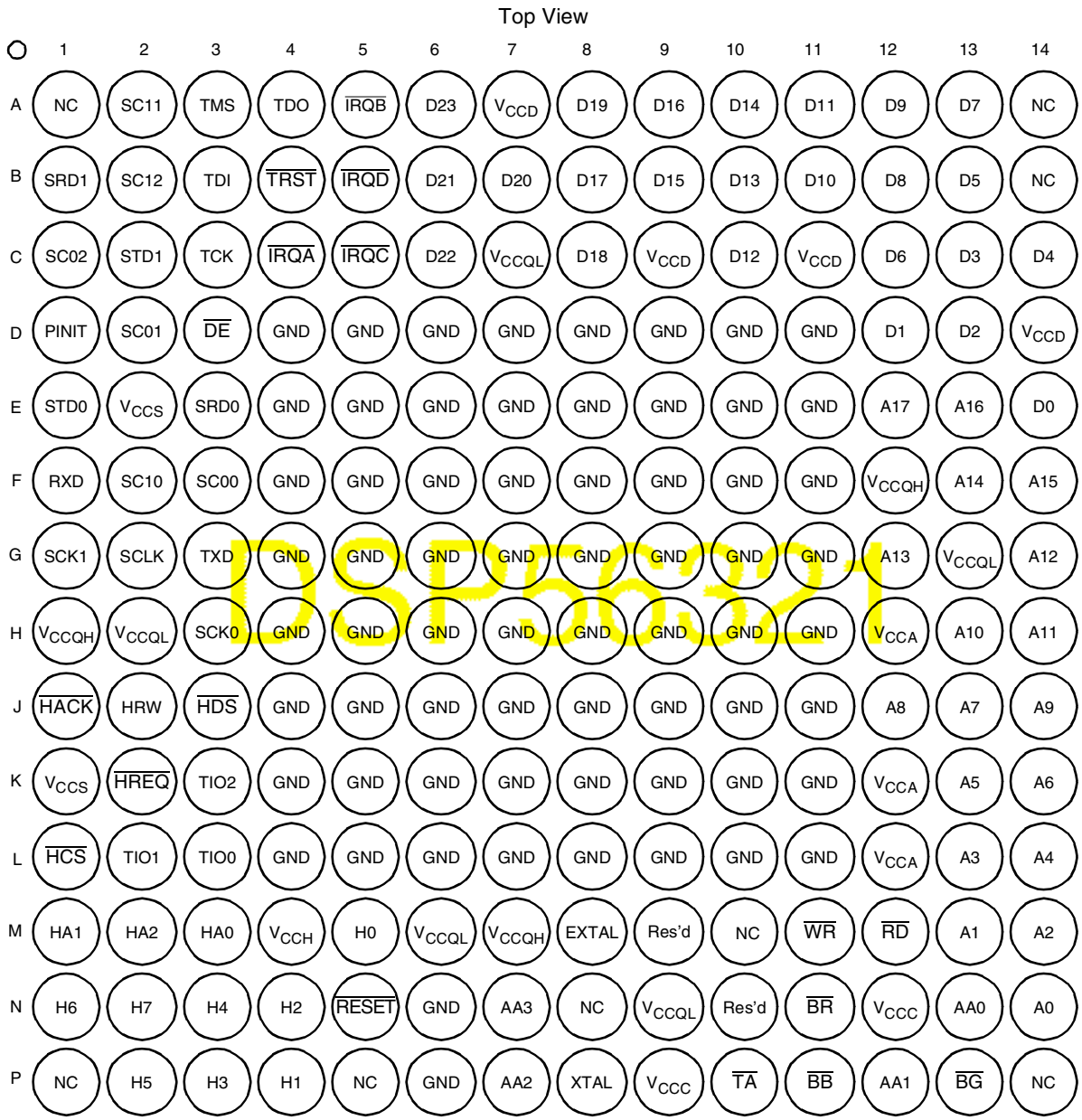


Figure 3-1. DSP56321 MAP-BGA Package, Top View

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $/\ \text{MIPS} = I/\ \text{MHz} = (I_{typF2} - I_{typF1})/\ (\text{F2} - \text{F1})$

Where:

I_{typF2}	=	current at F2
I_{typF1}	=	current at F1
F2	=	high frequency (any specified operating frequency)
F1	=	low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

```
M_IAL0 EQU 0                        ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1                        ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2                        ; IRQA Mode Trigger Mode
M_IBL EQU $38                       ; IRQB Mode Mask
M_IBL0 EQU 3                        ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4                        ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5                        ; IRQB Mode Trigger Mode
M_ICL EQU $1C0                      ; IRQC Mode Mask
M_ICL0 EQU 6                        ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7                        ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8                        ; IRQC Mode Trigger Mode
M_IDL EQU $E00                      ; IRQD Mode Mask
M_IDL0 EQU 9                        ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10                       ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11                       ; IRQD Mode Trigger Mode
M_D0L EQU $3000                     ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12                       ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13                       ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000                     ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14                       ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15                       ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000                    ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16                       ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17                       ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000                    ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18                       ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19                       ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000                   ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20                       ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21                       ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000                   ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22                       ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23                       ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3                        ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0                        ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1                        ; Host Interrupt Priority Level (high)
M_S0L EQU $C                        ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2                        ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3                        ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30                       ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4                        ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5                        ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0                       ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6                        ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7                        ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300                      ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8                        ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9                        ; TIMER Interrupt Priority Level (high)


;---------------------------------------------------------------------------
;
;       EQUATES for TIMER
;
;---------------------------------------------------------------------------

;       Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F                 ; Timer 0 Control/Status Register
```

```
M_DPR0 EQU 17                    ; DMA Channel Priority Level (low)
M_DPR1 EQU 18                    ; DMA Channel Priority Level (high)
M_DTM EQU $380000                ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19                    ; DMA Transfer Mode 0
M_DTM1 EQU 20                    ; DMA Transfer Mode 1
M_DTM2 EQU 21                    ; DMA Transfer Mode 2
M_DIE EQU 22                     ; DMA Interrupt Enable bit
M_DE EQU 23                      ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F                    ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0                     ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1                     ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2                     ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3                     ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4                     ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5                     ; DMA Channel Transfer Done Status 5
M_DACT EQU  8                    ; DMA Active State
M_DCH EQU  $E00                  ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9                    ; DMA Active Channel 0
M_DCH1 EQU  10                   ; DMA Active Channel 1
M_DCH2 EQU  11                   ; DMA Active Channel 2

;---------------------------------------------------------------------
;
;       EQUATES for Enhanced Filter Co-Processor (EFCOP)
;
;---------------------------------------------------------------------

M_FDIR   EQU     $FFFFB0         ; EFCOP Data Input Register
M_FDOR   EQU     $FFFFB1         ; EFCOP Data Output Register
M_FKIR   EQU     $FFFFB2         ; EFCOP K-Constant Register
M_FCNT   EQU     $FFFFB3         ; EFCOP Filter Counter
M_FCSR   EQU     $FFFFB4         ; EFCOP Control Status Register
M_FACR   EQU     $FFFFB5         ; EFCOP ALU Control Register
M_FDBA   EQU     $FFFFB6         ; EFCOP Data Base Address
M_FCBA   EQU     $FFFFB7         ; EFCOP Coefficient Base Address
M_FDCH   EQU     $FFFFB8         ; EFCOP Decimation/Channel Register



;---------------------------------------------------------------------
;
;       EQUATES for Phase Locked Loop (PLL)
;
;---------------------------------------------------------------------

;       Register Addresses Of PLL

M_DMFR   EQU     $FFFFD0
M_DPSC   EQU     $FFFFD0
M_PCTL   EQU     $FFFFD1         ; PLL Control Register

;       PLL Control Register

M_MFI    EQU     $F              ; Multiplication Factor Intager Bits Mask (MFI0-MFI3)
M_MFN    EQU     $7F0            ; Multiplication Factor Bits Mask (MFN0-MFN6)
M_MFD    EQU     $3F800          ; Multiplication Factor Bits Mask (MFD0-MFD6)
M_PDF    EQU     $3C0000         ; PreDivider Factor Bits Mask (PD0-PD3)
M_CPLM  EQU     22               ;
M_MFO   EQU     23               ;
M_CDF    EQU     $70             ; Division Factor Bits Mask (DF0-DF2)
```

```
;---------------------------------------------------------------------
; Non-Maskable interrupts
;---------------------------------------------------------------------
I_RESET EQU I_VEC+$00             ; Hardware RESET
I_STACK EQU I_VEC+$02             ; Stack Error
I_ILL EQU I_VEC+$04               ; Illegal Instruction
I_DBG EQU I_VEC+$06               ; Debug Request
I_TRAP EQU I_VEC+$08              ; Trap
I_NMI EQU I_VEC+$0A               ; Non Maskable Interrupt

;---------------------------------------------------------------------
; Interrupt Request Pins
;---------------------------------------------------------------------
I_IRQA EQU I_VEC+$10              ; IRQA
I_IRQB EQU I_VEC+$12              ; IRQB
I_IRQC EQU I_VEC+$14              ; IRQC
I_IRQD EQU I_VEC+$16              ; IRQD

;---------------------------------------------------------------------
; DMA Interrupts
;---------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18              ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A              ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C              ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E              ; DMA Channel 3
I_DMA4 EQU I_VEC+$20              ; DMA Channel 4
I_DMA5 EQU I_VEC+$22              ; DMA Channel 5

;---------------------------------------------------------------------
; Timer Interrupts
;---------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24             ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26            ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28             ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A            ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C             ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E            ; TIMER 2 overflow

;---------------------------------------------------------------------
; ESSI Interrupts
;---------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30             ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32            ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34            ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36             ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38            ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A            ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40             ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42            ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44            ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46             ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48            ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A            ; ESSI1 Transmit last slot

;---------------------------------------------------------------------
; SCI Interrupts
;---------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50             ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52            ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54             ; SCI Transmit Data
I_SCIIL EQU I_VEC+$56             ; SCI Idle Line
I_SCITM EQU I_VEC+$58             ; SCI Timer
```