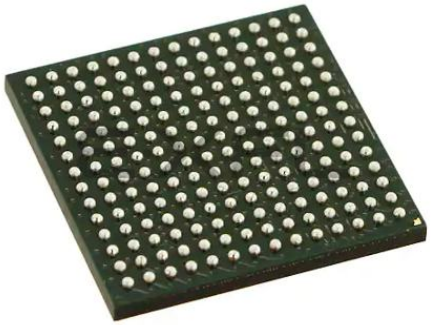

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	200MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56321vf200r2

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Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Signals/Connections 1

The DSP56321 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56321 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56321 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
Address bus	Port A[1]	18
Data bus		24
Bus control		10
Interrupt and mode control		6
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. Eight signal lines are not connected internally. These are designated as no connect (NC) in the package description (see **Chapter 3**). There are also two reserved lines.

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. See the *DSP56321 Reference Manual* for details on these configuration registers.

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCQL}	**Quiet Core (Low) Power**—An isolated power for the core processing and clock logic. This input must be isolated externally from all other chip power inputs.
V_{CCQH}	**Quiet External (High) Power**—A quiet power source for I/O lines. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds

Name	Description
GND	**Ground**—Connected to an internal device ground plane.
Note: The user must provide adequate external decoupling capacitors for all GND connections.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

Table 1-12. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-13. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

Table 1-13. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Timers

The DSP56321 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56321 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-14. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.11 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56321 support circuit-board test strategies based on the **IEEE® Std.** 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-15. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted during and after power-up (see EB610/D for details).
$\overline{\text{DE}}$	Input/ Output	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	44	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	25	°C/W
Junction-to-ambient, @200 ft/min air flow, single-layer board (1s)[1,3]	$R_{\theta JMA}$	35	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	13	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	7	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage[1]: • Core (V_{CCQL}) • I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		 1.5 3.0	 1.6 3.3	 1.7 3.6	 V V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD/$\overline{IRQ}$[2] $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CCQH}$	 — — —	 $V_{CCQH} + 0.3$ $V_{CCQH} + 0.3$ V_{CCQH}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CCQH}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[8] • TTL (I_{OH} = –0.4 mA)[6] • CMOS (I_{OH} = –10 µA)[6]	V_{OH}	 2.4 $V_{CCQH} - 0.01$	 — —	 — —	 V V
Output low voltage[8] • TTL (I_{OL} = 3.0 mA)[6] • CMOS (I_{OL} = 10 µA)[6]	V_{OL}	 — —	 — —	 0.4 0.01	 V V

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7]	(WS + 3.25) × T_C – 10.94	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7] • SRAM WS = 3 • SRAM WS ≥ 4	 (WS + 3) × T_C – 10.94 (WS + 2.5) × T_C – 10.94	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 ns ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		8.0	—	8.0	—	8.0	—	8.0	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop (PCTL Bit 1 = 1; Implies No Stop Delay)	 DPLT + (128K × T_C) DPLT + (23.75 ± 0.5) × T_C (10.0 ± 1.75) × T_C	 662.2 µs 6.9 41.25	 209.9 ms 188.8 58.8	 662.2 µs 6.9 37.5	 209.9 ms 188.8 53.3	 662.2 µs 6.9 34.4	 209.9 ms 188.8 49.0	 662.2 µs 6.9 30.0	 209.9 ms 188.8 43.0	 — µs ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop ((PCTL bit 1 = 0; implies no Stop delay)	 DPLT + (128 K × T_C) DPLT + (20.5 ± 0.5) × T_C 5.5 × T_C	 805.4 150.1 27.5	 — — —	 805.4 150.1 25	 — — —	 805.4 150.1 22.9	 — — —	 805.4 150.1 20.0	 — — —	 µs µs ns
27	Interrupt Request Rate • HI08, ESSI, SCI, Timer • DMA • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) • $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	 12T_C 8T_C 8T_C 12T_C	 — — — —	 60.0 40.0 40.0 60.0	 — — — —	 54.6 36.4 36.4 54.6	 — — — —	 50.0 33.4 33.4 50.0	 — — — —	 43.7 29.2 29.2 43.7	 ns ns ns ns
28	DMA Request Rate • Data read from HI08, ESSI, SCI • Data write to HI08, ESSI, SCI • Timer • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	 6T_C 7T_C 2T_C 3T_C	 — — — —	 30.0 35.0 10.0 15.0	 — — — —	 27.3 31.9 9.1 13.7	 — — — —	 25.0 29.2 8.3 12.5	 — — — —	 21.84 25.48 7.28 10.92	 ns ns ns ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	4.25 × T_C + 2.0	23.25	—	21.34	—	19.72	—	17.45	—	ns

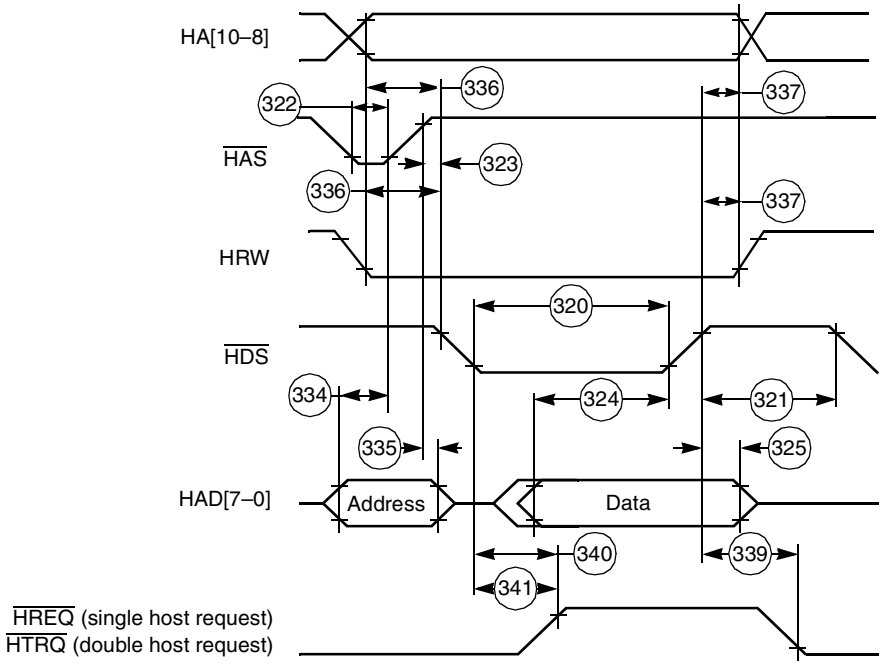


Figure 2-20. Write Timing Diagram, Multiplexed Bus, Single Data Strobe

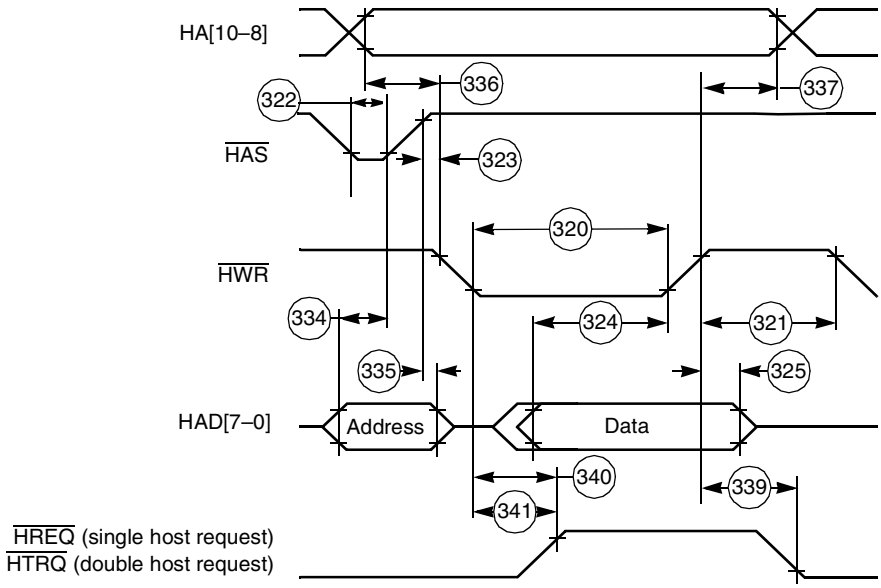


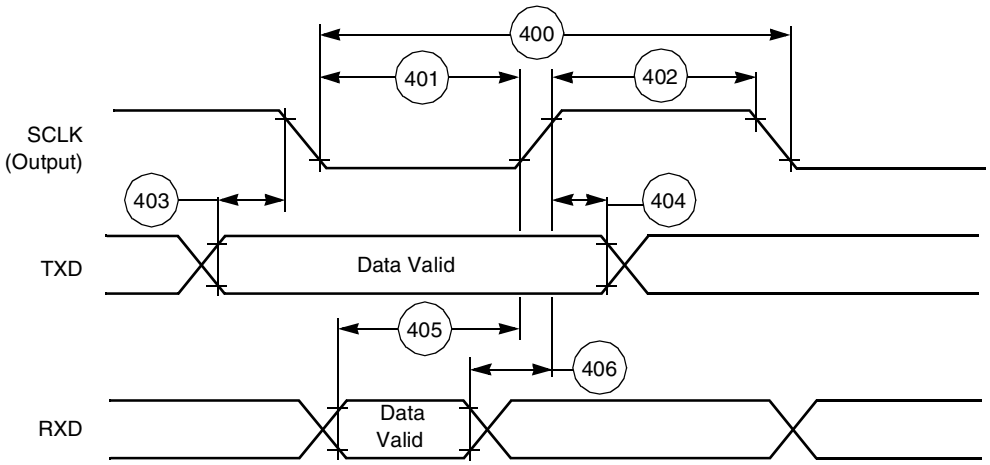
Figure 2-21. Write Timing Diagram, Multiplexed Bus, Double Data Strobe

2.4.7 SCI Timing

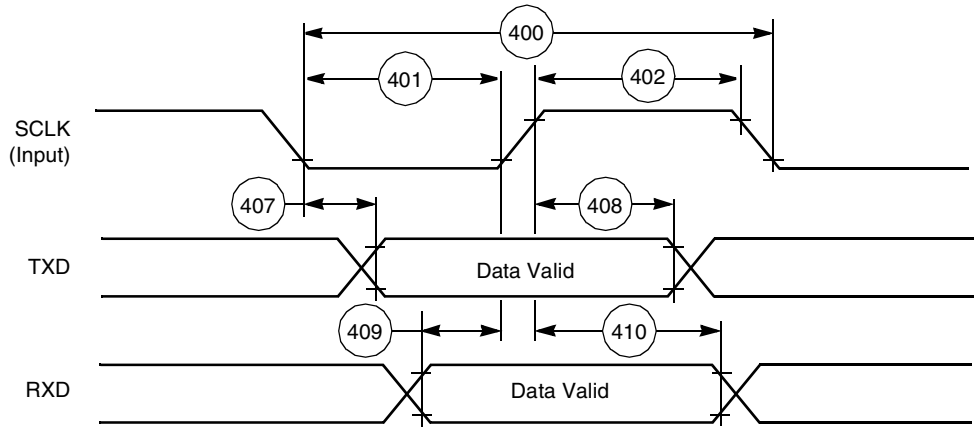
Table 2-11. SCI Timings

No.	Characteristics[1]	Symbol	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$16 \times T_C$	80.0	—	72.8	—	66.7	—	58.0	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	30.0	—	26.4	—	23.4	—	19.0	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	30.0	—	26.4	—	23.4	—	19.0	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	5.5	—	3.5	—	1.76	—	–0.68	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 1.5 \times T_C$	13	—	11.5	—	10	—	9.04	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	47.5	—	45.5	—	43.8	—	41.32	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	17.0	—	15.0	—	13.8	—	10.81	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	—	32.0	—	32.0	—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	13.0	—	12.6	—	12.2	—	11.64	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	0.0	—	0.0	—	0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	9.0	—	9.0	—	9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	320.0	—	291.2	—	266.9	—	232.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	150.0	—	135.6	—	123.5	—	106.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	150.0	—	135.6	—	123.5	—	106.0	—	ns
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	130.0	—	115.6	—	103.5	—	86.0	—	ns
415	Output data hold after clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	130.0	—	115.6	—	103.5	—	86.0	—	ns

Notes:
1. $V_{CCQH} = 3.3\ V \pm 0.3\ V$, $V_{CCQL} = 1.6\ V \pm 0.1\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.
2. t_{SCC} = synchronous clock cycle time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C).
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (for internal clock, t_{ACC} is determined by the SCI clock control register and T_C).
4. In the timing diagrams that follow, the SCLK is drawn using the clock falling edge as a the first reference. Clock polarity is programmable in the SCI Control Register (SCR). Refer to the *DSP56321 Reference Manual* for details.



a) Internal Clock



b) External Clock

Figure 2-22. SCI Synchronous Mode Timing

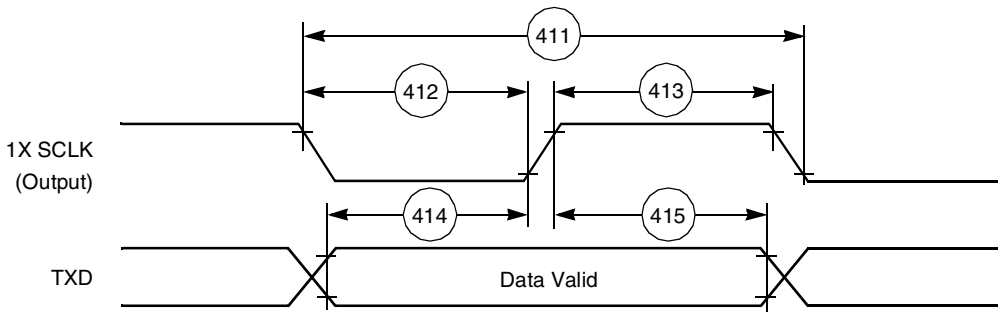


Figure 2-23. SCI Asynchronous Mode Timing

2.4.8 ESSI0/ESSI1 Timing

Table 2-12. ESSI Timings

No.	Characteristics[4, 6]	Symbol	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max	Min	Max		
430	Clock cycle[1]	T_{ECCX} T_{ECCI}	$6 \times T_C$ $8 \times T_C$	30.0 40.0	— —	27.3 36.6	— —	25.0 33.3	— —	21.5 25.0	— —	x ck i ck	ns ns
431	Clock high period • For internal clock • For external clock		 $T_{ECCX}/2 - 3.7$ $T_{ECCI}/2 - 10.0$	 11.3 10.0	 — —	 9.9 8.2	 — —	 8.8 6.7	 — —	 7.21 2.5	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $T_{ECCX}/2 - 3.7$ $T_{ECCI}/2 - 10.0$	 11.3 10.0	 — —	 9.9 8.2	 — —	 8.8 6.7	 — —	 7.21 2.5	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns

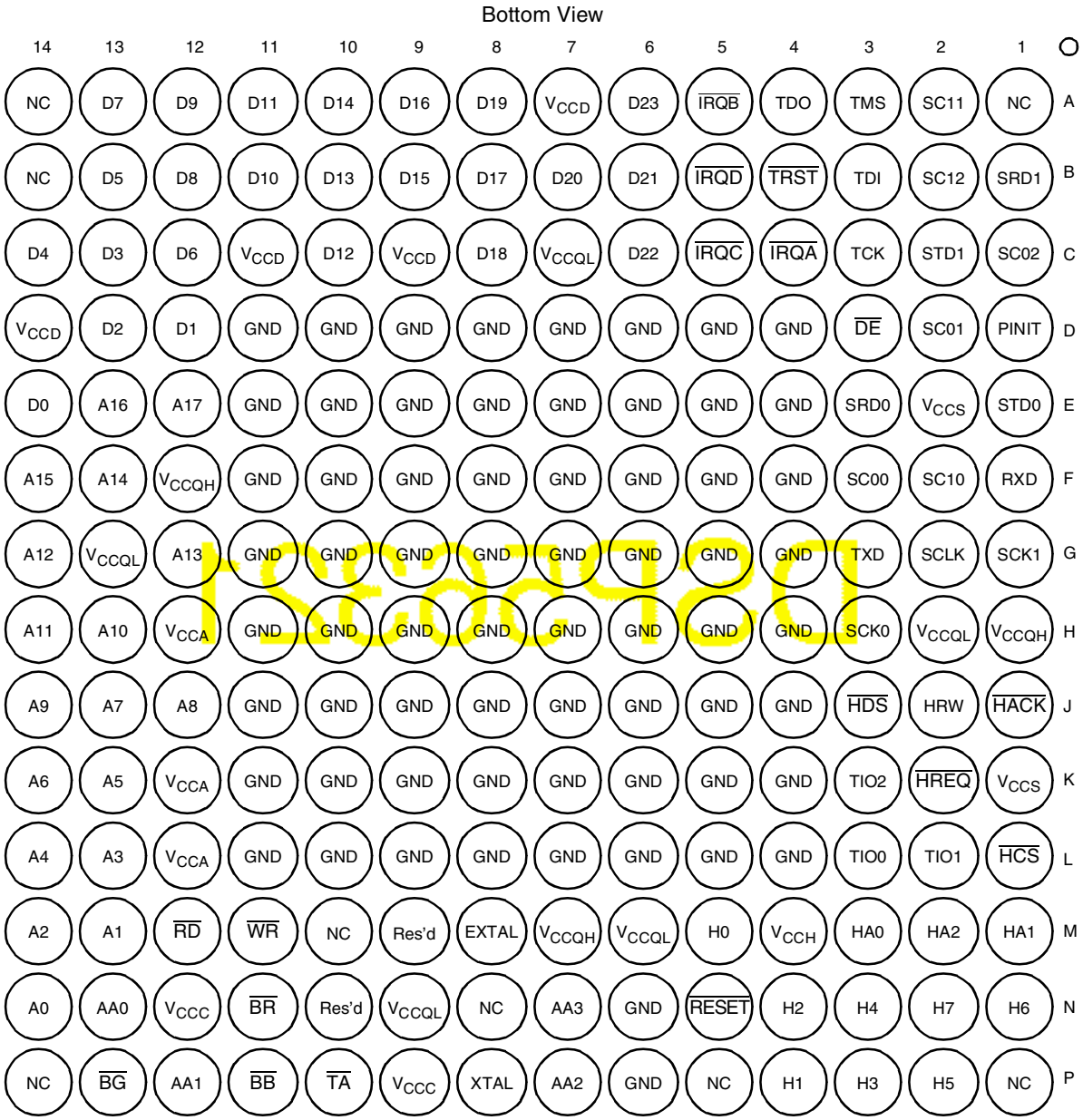


Figure 3-2. DSP56321 MAP-BGA Package, Bottom View

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $/\ \text{MIPS} = I/\ \text{MHz} = (I_{typF2} - I_{typF1})/\ (\text{F2} - \text{F1})$

Where:

I_{typF2}	=	current at F2
I_{typF1}	=	current at F1
F2	=	high frequency (any specified operating frequency)
F1	=	low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

Power Consumption Benchmark A

The following benchmark program evaluates DSP56321 power use in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;*************************************************************************
;*************************************************************************
;*                                                                       *
;*                    CHECKS   Typical Power Consumption                 *
;*                                                                       *
;*************************************************************************

       page   200,55,0,0,0
       nolist

I_VEC EQU $000000; Interrupt vectors for program debug only
START EQU $8000; MAIN (external) program starting address
INT_PROG  EQU $100 ; INTERNAL program memory starting address
INT_XDAT  EQU $0; INTERNAL X-data memory starting address
INT_YDAT  EQU $0; INTERNAL Y-data memory starting address

       INCLUDE "ioequ.asm"
       INCLUDE "intequ.asm"

       list

       org    P:START
;
       movep #$0243FF,x:M_BCR ;   ; BCR: Area 3 = 2 w.s (SRAM)
; Default: 2w.s (SRAM)
;
       movep  #$00000F,x:M_PCTL   ; XTAL disable
                                  ; PLL enable
;
; Load the program
;
       move   #INT_PROG,r0
       move   #PROG_START,r1
       do     #(PROG_END-PROG_START),PLOAD_LOOP
       move   p:(r1)+,x0
       move   x0,p:(r0)+
       nop
PLOAD_LOOP
;
; Load the X-data
;
       move   #INT_XDAT,r0
       move   #XDAT_START,r1
       do     #(XDAT_END-XDAT_START),XLOAD_LOOP
       move   p:(r1)+,x0
       move   x0,x:(r0)+
XLOAD_LOOP
```

```
        dc      $B3829
        dc      $8BF7AE
        dc      $63A94F
        dc      $EF78DC
        dc      $242DE5
        dc      $A3E0BA
        dc      $EBAB6B
        dc      $8726C8
        dc      $CA361
        dc      $2F6E86
        dc      $A57347
        dc      $4BE774
        dc      $8F349D
        dc      $A1ED12
        dc      $4BFCE3
        dc      $EA26E0
        dc      $CD7D99
        dc      $4BA85E
        dc      $27A43F
        dc      $A8B10C
        dc      $D3A55
        dc      $25EC6A
        dc      $2A255B
        dc      $A5F1F8
        dc      $2426D1
        dc      $AE6536
        dc      $CBBC37
        dc      $6235A4
        dc      $37F0D
        dc      $63BEC2
        dc      $A5E4D3
        dc      $8CE810
        dc      $3FF09
        dc      $60E50E
        dc      $CFFB2F
        dc      $40753C
        dc      $8262C5
        dc      $CA641A
        dc      $EB3B4B
        dc      $2DA928
        dc      $AB6641
        dc      $28A7E6
        dc      $4E2127
        dc      $482FD4
        dc      $7257D
        dc      $E53C72
        dc      $1A8C3
        dc      $E27540
XDAT_END

YDAT_START
;       org     y:0
        dc      $5B6DA
        dc      $C3F70B
        dc      $6A39E8
        dc      $81E801
        dc      $C666A6
        dc      $46F8E7
        dc      $AAEC94
        dc      $24233D
        dc      $802732
        dc      $2E3C83
        dc      $A43E00
```

```
;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF               ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE               ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED               ; DMA0 Counter
M_DCR0 EQU $FFFFEC               ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB               ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA               ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9               ; DMA1 Counter
M_DCR1 EQU $FFFFE8               ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7               ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6               ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5               ; DMA2 Counter
M_DCR2 EQU $FFFFE4               ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3               ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2               ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1               ; DMA3 Counter
M_DCR3 EQU $FFFFE0               ; DMA3 Control Register

;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF               ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE               ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD               ; DMA4 Counter
M_DCR4 EQU $FFFFDC               ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB               ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA               ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9               ; DMA5 Counter
M_DCR5 EQU $FFFFD8               ; DMA5 Control Register

;      DMA Control Register

M_DSS EQU $3                     ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0                     ; DMA Source Memory space 0
M_DSS1 EQU 1                     ; DMA Source Memory space 1
M_DDS EQU $C                     ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2                     ; DMA Destination Memory Space 0
M_DDS1 EQU 3                     ; DMA Destination Memory Space 1
M_DAM EQU $3f0                   ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4                    ; DMA Address Mode 0
M_DAM1  EQU 5                    ; DMA Address Mode 1
M_DAM2  EQU 6                    ; DMA Address Mode 2
M_DAM3  EQU 7                    ; DMA Address Mode 3
M_DAM4  EQU 8                    ; DMA Address Mode 4
M_DAM5  EQU 9                    ; DMA Address Mode 5
M_D3D EQU 10                     ; DMA Three Dimensional Mode
M_DRS EQU $F800                  ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16                    ; DMA Continuous Mode
M_DPR EQU $60000                 ; DMA Channel Priority
```

```
M_DPR0 EQU 17                    ; DMA Channel Priority Level (low)
M_DPR1 EQU 18                    ; DMA Channel Priority Level (high)
M_DTM EQU $380000                ; DMA Transfer Mode Mask (DTM2-DTM0)
M_DTM0 EQU 19                    ; DMA Transfer Mode 0
M_DTM1 EQU 20                    ; DMA Transfer Mode 1
M_DTM2 EQU 21                    ; DMA Transfer Mode 2
M_DIE EQU 22                     ; DMA Interrupt Enable bit
M_DE EQU 23                      ; DMA Channel Enable bit

;       DMA Status Register

M_DTD EQU $3F                    ; Channel Transfer Done Status MASK (DTD0-DTD5)
M_DTD0 EQU 0                     ; DMA Channel Transfer Done Status 0
M_DTD1 EQU 1                     ; DMA Channel Transfer Done Status 1
M_DTD2 EQU 2                     ; DMA Channel Transfer Done Status 2
M_DTD3 EQU 3                     ; DMA Channel Transfer Done Status 3
M_DTD4 EQU 4                     ; DMA Channel Transfer Done Status 4
M_DTD5 EQU 5                     ; DMA Channel Transfer Done Status 5
M_DACT EQU  8                    ; DMA Active State
M_DCH EQU  $E00                  ; DMA Active Channel Mask (DCH0-DCH2)
M_DCH0 EQU  9                    ; DMA Active Channel 0
M_DCH1 EQU  10                   ; DMA Active Channel 1
M_DCH2 EQU  11                   ; DMA Active Channel 2

;---------------------------------------------------------------------
;
;       EQUATES for Enhanced Filter Co-Processor (EFCOP)
;
;---------------------------------------------------------------------

M_FDIR   EQU     $FFFFB0         ; EFCOP Data Input Register
M_FDOR   EQU     $FFFFB1         ; EFCOP Data Output Register
M_FKIR   EQU     $FFFFB2         ; EFCOP K-Constant Register
M_FCNT   EQU     $FFFFB3         ; EFCOP Filter Counter
M_FCSR   EQU     $FFFFB4         ; EFCOP Control Status Register
M_FACR   EQU     $FFFFB5         ; EFCOP ALU Control Register
M_FDBA   EQU     $FFFFB6         ; EFCOP Data Base Address
M_FCBA   EQU     $FFFFB7         ; EFCOP Coefficient Base Address
M_FDCH   EQU     $FFFFB8         ; EFCOP Decimation/Channel Register



;---------------------------------------------------------------------
;
;       EQUATES for Phase Locked Loop (PLL)
;
;---------------------------------------------------------------------

;       Register Addresses Of PLL

M_DMFR   EQU     $FFFFD0
M_DPSC   EQU     $FFFFD0
M_PCTL   EQU     $FFFFD1         ; PLL Control Register

;       PLL Control Register

M_MFI    EQU     $F              ; Multiplication Factor Intager Bits Mask (MFI0-MFI3)
M_MFN    EQU     $7F0            ; Multiplication Factor Bits Mask (MFN0-MFN6)
M_MFD    EQU     $3F800          ; Multiplication Factor Bits Mask (MFD0-MFD6)
M_PDF    EQU     $3C0000         ; PreDivider Factor Bits Mask (PD0-PD3)
M_CPLM  EQU     22               ;
M_MFO   EQU     23               ;
M_CDF    EQU     $70             ; Division Factor Bits Mask (DF0-DF2)
```

Ordering Information

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Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
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					Lead-bearing	DSP56321VF200
				220	Lead-free	DSP56321VL220
					Lead-bearing	DSP56321VF220
				240	Lead-free	DSP56321VL240
					Lead-bearing	DSP56321VF240
				275	Lead-free	DSP56321VL275
					Lead-bearing	DSP56321VF275

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