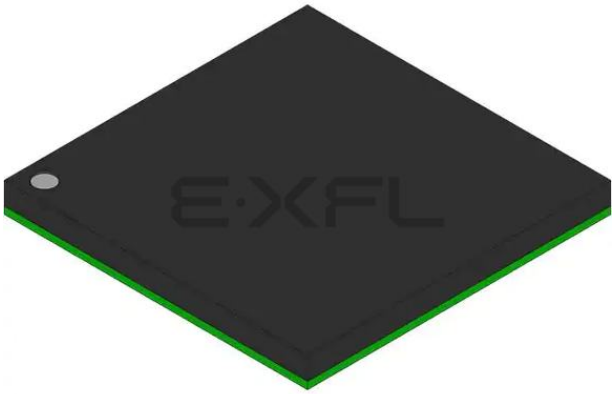

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	220MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56321vf220

Features

Table 1 lists the features of the DSP56321 device.

Table 1. DSP56321 Features

Feature	Description
High-Performance DSP56300 Core	• 275 million multiply-accumulates per second (MMACS) (550 MMACS using the EFCOP in filtering applications) with a 275 MHz clock at 1.6 V core and 3.3 V I/O • Object code compatible with the DSP56000 core with highly parallel instruction set • Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control • Program control unit (PCU) with position independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts • Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals • Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination • Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)

Enhanced Filter Coprocessor (EFCOP)	• Internal 24 × 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core
	• Operation at the same frequency as the core (up to 275 MHz)
	• Support for a variety of filter modes, some of which are optimized for cellular base station applications:
	  • Real finite impulse response (FIR) with real taps
	  • Complex FIR with complex taps
	  • Complex FIR generating pure real or pure imaginary outputs alternately
	  • A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16
	  • Direct form 1 (DFI) Infinite Impulse Response (IIR) filter
	  • Direct form 2 (DFII) IIR filter
	  • Four scaling factors (1, 4, 8, 16) for IIR output
	  • Adaptive FIR filter with true least mean square (LMS) coefficient updates
	  • Adaptive FIR filter with delayed LMS coefficient updates

Internal Peripherals	• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

Signals/Connections 1

The DSP56321 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56321 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56321 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
Address bus	Port A[1]	18
Data bus		24
Bus control		10
Interrupt and mode control		6
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. Eight signal lines are not connected internally. These are designated as no connect (NC) in the package description (see **Chapter 3**). There are also two reserved lines.

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. See the *DSP56321 Reference Manual* for details on these configuration registers.

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCQL}	**Quiet Core (Low) Power**—An isolated power for the core processing and clock logic. This input must be isolated externally from all other chip power inputs.
V_{CCQH}	**Quiet External (High) Power**—A quiet power source for I/O lines. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds

Name	Description
GND	**Ground**—Connected to an internal device ground plane.
Note: The user must provide adequate external decoupling capacitors for all GND connections.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

1.6 Host Interface (HI08)

The HI08 provides a fast, 8-bit, parallel data port that connects directly to the host bus. The HI08 supports a variety of standard buses and connects directly to a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

1.6.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-9**.

Table 1-9. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), the host interface programmer should use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	The host interface programmer should not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.
Asynchronous write to host vector	The host interface programmer must change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

1.6.2 Host Port Configuration

HI08 signal functions vary according to the programmed configuration of the interface as determined by the 16 bits in the HI08 Port Control Register.

Table 1-10. Host Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
H[0–7]	Input/Output	Ignored Input	**Host Data—**When the HI08 is programmed to interface with a non-multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional Data bus.
HAD[0–7]	Input/Output		**Host Address—**When the HI08 is programmed to interface with a multiplexed host bus and the HI function is selected, these signals are lines 0–7 of the bidirectional multiplexed Address/Data bus.
PB[0–7]	Input or Output		**Port B 0–7—**When the HI08 is configured as GPIO through the HI08 Port Control Register, these signals are individually programmed as inputs or outputs through the HI08 Data Direction Register.

1.7 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Freescale serial peripheral interface (SPI).

Table 1-11. Enhanced Synchronous Serial Interface 0

Signal Name	Type	State During Reset[1,2]	Signal Description
SC00	Input or Output	Ignored Input	**Serial Control 0**—For asynchronous mode, this signal is used for the receive clock I/O (Schmitt-trigger input). For synchronous mode, this signal is used either for transmitter 1 output or for serial I/O flag 0.
PC0	Input or Output		**Port C 0**—The default configuration following reset is GPIO input PC0. When configured as PC0, signal direction is controlled through the Port C Direction Register. The signal can be configured as ESSI signal SC00 through the Port C Control Register.
SC01	Input/Output	Ignored Input	**Serial Control 1**—For asynchronous mode, this signal is the receiver frame sync I/O. For synchronous mode, this signal is used either for transmitter 2 output or for serial I/O flag 1.
PC1	Input or Output		**Port C 1**—The default configuration following reset is GPIO input PC1. When configured as PC1, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC01 through the Port C Control Register.
SC02	Input/Output	Ignored Input	**Serial Control Signal 2**—The frame sync for both the transmitter and receiver in synchronous mode, and for the transmitter only in asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		**Port C 2**—The default configuration following reset is GPIO input PC2. When configured as PC2, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SC02 through the Port C Control Register.
SCK0	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK0 is a clock input or output, used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		**Port C 3**—The default configuration following reset is GPIO input PC3. When configured as PC3, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SCK0 through the Port C Control Register.
SRD0	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD0 is an input when data is received.
PC4	Input or Output		**Port C 4**—The default configuration following reset is GPIO input PC4. When configured as PC4, signal direction is controlled through the Port C Direction Register. The signal can be configured as an ESSI signal SRD0 through the Port C Control Register.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	44	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	25	°C/W
Junction-to-ambient, @200 ft/min air flow, single-layer board (1s)[1,3]	$R_{\theta JMA}$	35	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	13	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	7	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage[1]: • Core (V_{CCQL}) • I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		 1.5 3.0	 1.6 3.3	 1.7 3.6	 V V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD/$\overline{IRQ}$[2] $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CCQH}$	 — — —	 $V_{CCQH} + 0.3$ $V_{CCQH} + 0.3$ V_{CCQH}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CCQH}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[8] • TTL (I_{OH} = –0.4 mA)[6] • CMOS (I_{OH} = –10 µA)[6]	V_{OH}	 2.4 $V_{CCQH} - 0.01$	 — —	 — —	 V V
Output low voltage[8] • TTL (I_{OL} = 3.0 mA)[6] • CMOS (I_{OL} = 10 µA)[6]	V_{OL}	 — —	 — —	 0.4 0.01	 V V

Table 2-6. CLKGEN and DPLL Characteristics (Continued)

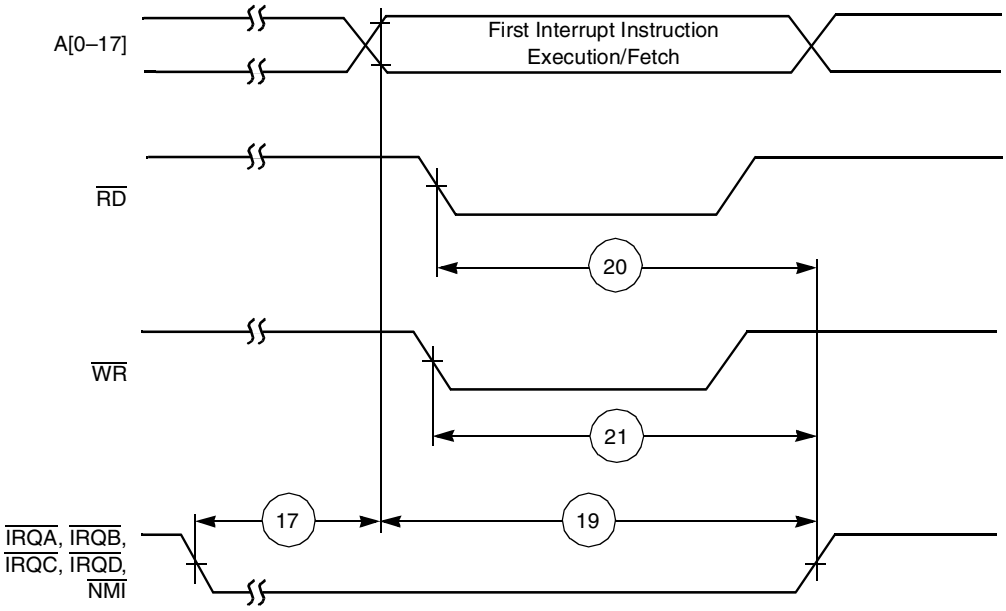
Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	

Notes:
1. Refer to the *DSP56321 User's Manual* for a detailed description of register reset values.
2. The total multiplication factor (MF) includes both integer and fractional parts (that is, MF = MFI + MFN/MFD).
3. The numerator (MFN) should be less than the denominator (MFD).
4. DPLL lock procedure duration is specified for the case when an external clock source is supplied to the EXTAL pin.
5. Frequency-only Lock Mode or non-integer MF, after partial reset.
6. Frequency and Phase Lock Mode, integer MF, after full reset.

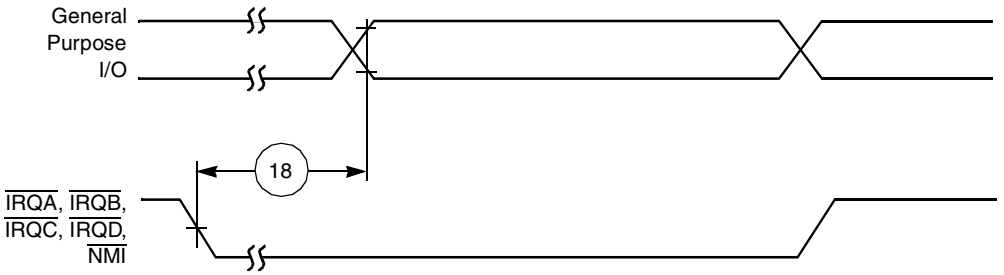
2.4.4 Reset, Stop, Mode Select, and Interrupt Timing

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5]

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
8	Delay from $\overline{\text{RESET}}$ assertion to all pins at reset value[3]	—	—	26	—	26	—	26	—	26	ns
9	Required $\overline{\text{RESET}}$ duration[4]										
	• Power on, external clock generator, DPLL disabled	$50 \times ET_C$	250.0	—	227.5	—	208.5	—	182.0	—	ns
	• Power on, external clock generator, DPLL enabled	$1000 \times ET_C$	5.0	—	4.55	—	4.17	—	3.64	—	µs
	• Power on, internal oscillator	$75000 \times ET_C$	0.375	—	0.341	—	0.313	—	0.273	—	ms
	• During STOP, XTAL disabled	$75000 \times ET_C$	0.375	—	0.341	—	0.313	—	0.273	—	ms
	• During STOP, XTAL enabled	$2.5 \times T_C$	12.5	—	11.38	—	10.43	—	9.1	—	ns
	• During normal operation	$2.5 \times T_C$	17	—	16	—	15	—	9.1	—	ns
10	Delay from asynchronous $\overline{\text{RESET}}$ deassertion to first external address output (internal reset deassertion)										
	• Minimum	$3.25 \times T_C + 2.0$	18.25	—	16.77	—	15.55	—	13.82	—	ns
	• Maximum		—	180	—	163	—	150	—	140	ns
13	Mode select setup time		30.0	—	30.0	—	30.0	—	30.0	—	ns
14	Mode select hold time		0.0	—	0.0	—	0.0	—	0.0	—	ns
15	Minimum edge-triggered interrupt request assertion width		4.0	—	4.0	—	4.0	—	4.0	—	ns
16	Minimum edge-triggered interrupt request deassertion width		4.0	—	4.0	—	4.0	—	4.0	—	ns
17	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to external memory access address out valid										
	• Caused by first interrupt instruction fetch	$4.25 \times T_C + 2.0$	23.25	—	21.24	—	19.72	—	17.45	—	ns
	• Caused by first interrupt instruction execution	$7.25 \times T_C + 2.0$	38.25	—	34.99	—	32.23	—	28.36	—	ns
18	Delay from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{NMI}}$ assertion to general-purpose transfer output valid caused by first interrupt instruction execution	$8.9 \times T_C$	44.5	—	40.45	—	37.0	—	32.37	—	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7]	$(WS + 3.75) \times T_C - 10.94$	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

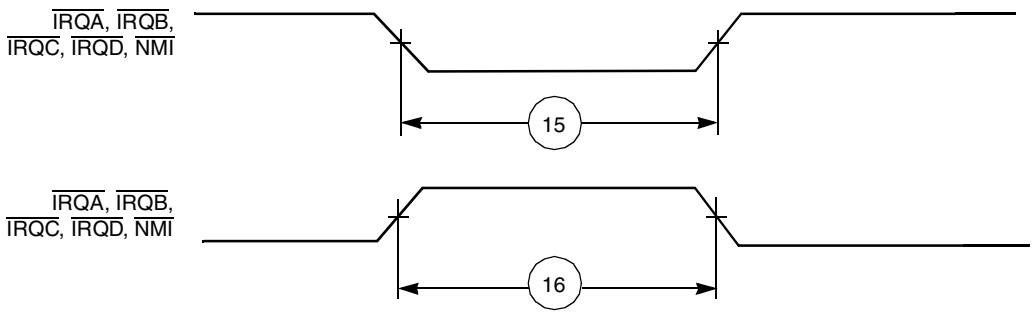


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)

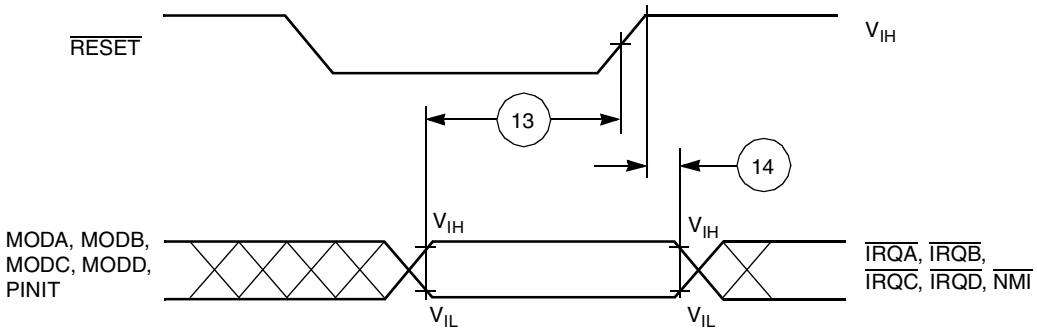


Figure 2-6. Operating Mode Select Timing

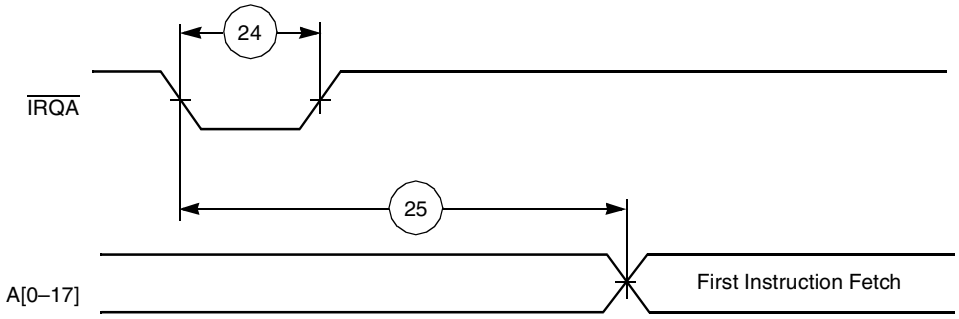


Figure 2-7. Recovery from Stop State Using IRQA

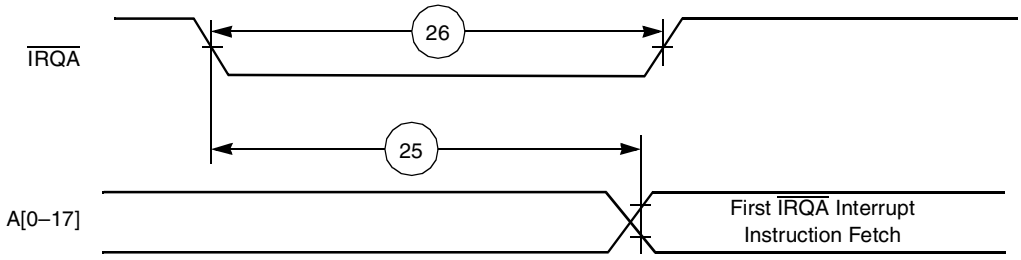


Figure 2-8. Recovery from Stop State Using IRQA Interrupt Service

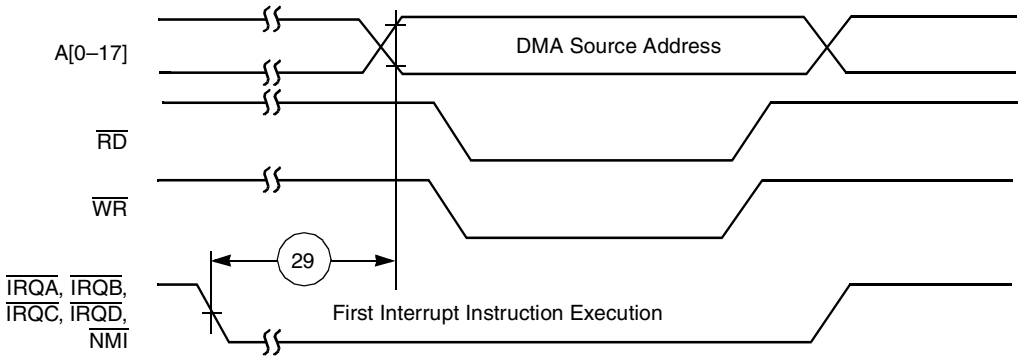


Figure 2-9. External Memory Access (DMA Source) Timing

Table 2-10. Host Interface Timings[1,2,12] (Continued)

No.	Characteristic[10]	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	

Notes:
1. See the Programmer's Model section in the chapter on the HI08 in the *DSP56321 Reference Manual*.
2. In the timing diagrams below, the controls pins are drawn as active low. The pin polarity is programmable.
3. This timing is applicable only if two consecutive reads from one of these registers are executed.
4. The data strobe is Host Read (HRD) or Host Write (HWR) in the Dual Data Strobe mode and Host Data Strobe (HDS) in the Single Data Strobe mode.
5. The read data strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
6. The write data strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
7. The host request is HREQ in the Single Host Request mode and HRRQ and HTRQ in the Double Host Request mode.
8. The "Last Data Register" is the register at address $7, which is the last location to be read or written in data transfers. This is RXL/TXL in the Big Endian mode (HLEND = 0; HLEND is the Interface Control Register bit 7—ICR[7]), or RXH/TXH in the Little Endian mode (HLEND = 1).
9. In this calculation, the host request signal is pulled up by a 4.7 kΩ resistor in the Open-drain mode.
10. V_{CCQH} = 3.3 V ± 0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
11. This timing is applicable only if a read from the "Last Data Register" is followed by a read from the RXL, RXM, or RXH registers without first polling RXDF or HREQ bits, or waiting for the assertion of the HREQ signal.
12. After the external host writes a new value to the ICR, the HI08 will be ready for operation after three DSP clock cycles (3 × Tc).

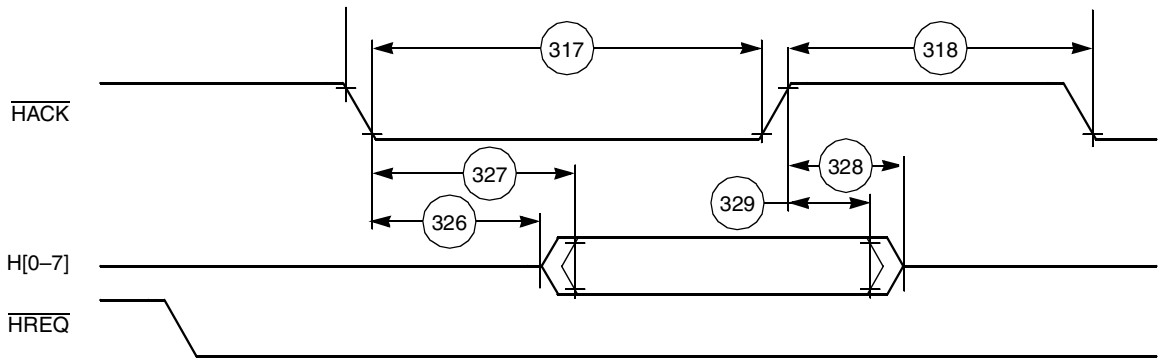


Figure 2-13. Host Interrupt Vector Register (IVR) Read Timing Diagram

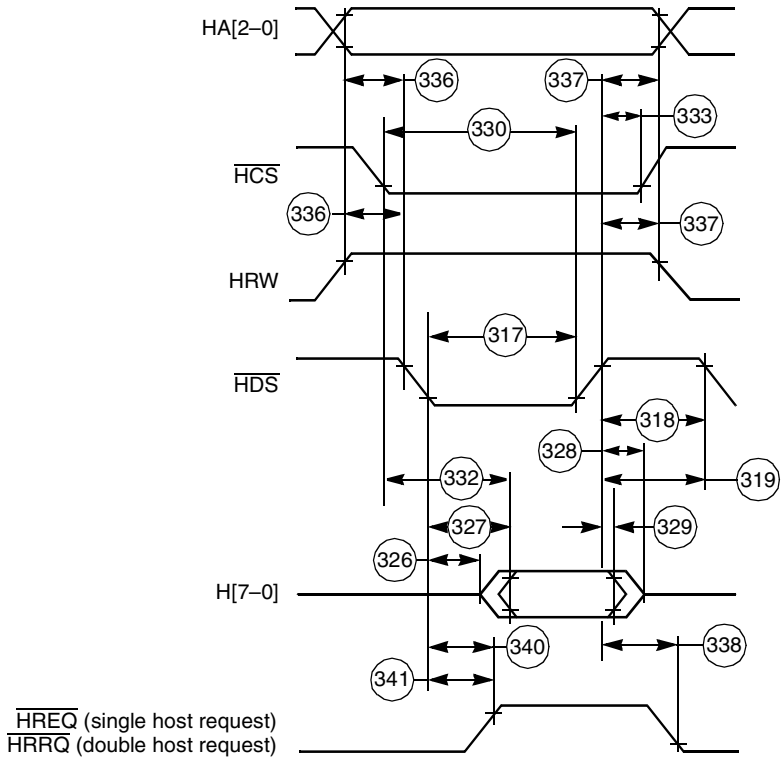


Figure 2-14. Read Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

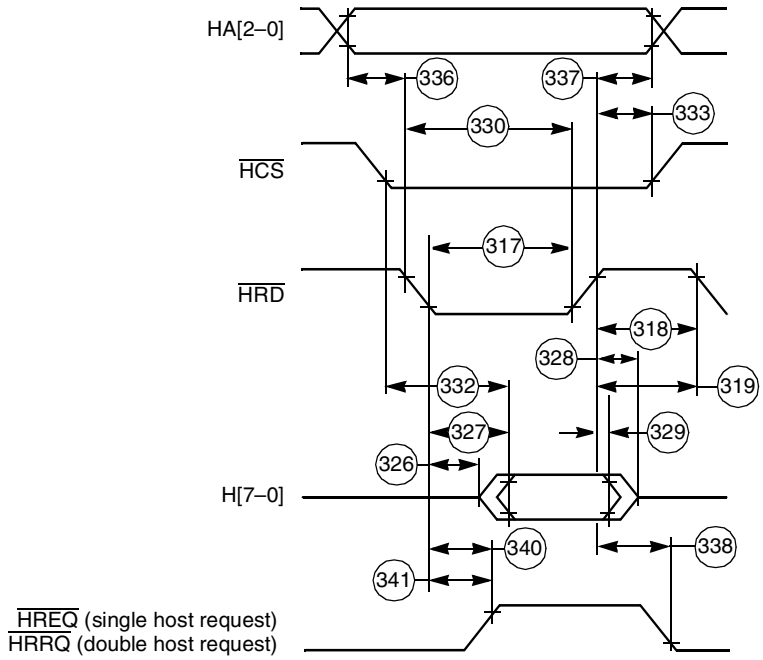


Figure 2-15. Read Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

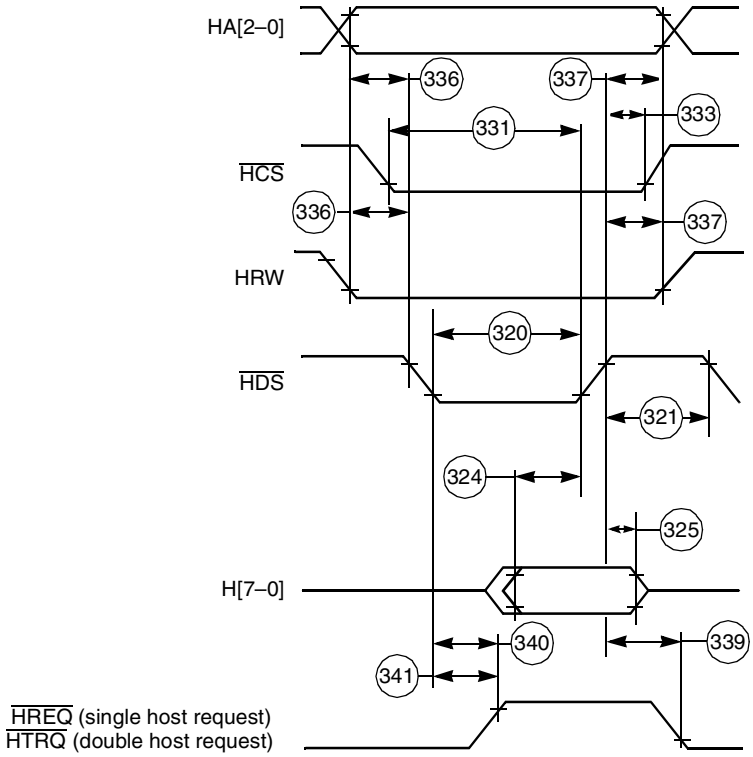


Figure 2-16. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

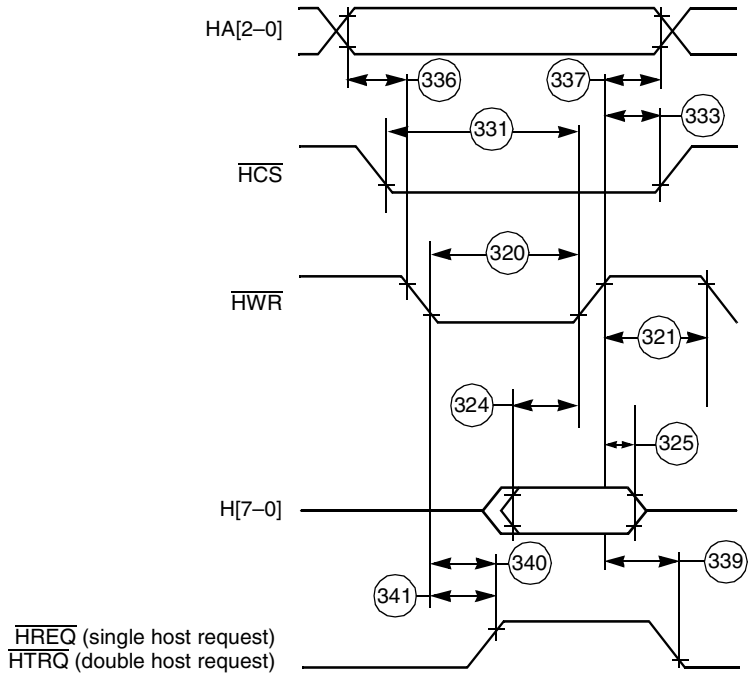


Figure 2-17. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

Table 3-1. Signal List by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	Not Connected (NC)	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-2. Signal List by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
GND	F9	GND	K4	HA1	M1
GND	F10	GND	K5	HA10	L1
GND	F11	GND	K6	HA2	M2
GND	G4	GND	K7	HA8	M1
GND	G5	GND	K8	HA9	M2
GND	G6	GND	K9	$\overline{\text{HACK}}$/HACK	J1
GND	G7	GND	K10	HAD0	M5
GND	G8	GND	K11	HAD1	P4
GND	G9	GND	L4	HAD2	N4
GND	G10	GND	L5	HAD3	P3
GND	G11	GND	L6	HAD4	N3
GND	H4	GND	L7	HAD5	P2
GND	H5	GND	L8	HAD6	N1
GND	H6	GND	L9	HAD7	N2
GND	H7	GND	L10	$\overline{\text{HAS}}$/HAS	M3
GND	H8	GND	L11	$\overline{\text{HCS}}$/HCS	L1
GND	H9	GND	N6	$\overline{\text{HDS}}$/HDS	J3
GND	H10	GND	P6	$\overline{\text{HRD}}$/HRD	J2
GND	H11	H0	M5	$\overline{\text{HREQ}}$/HREQ	K2
GND	J4	H1	P4	$\overline{\text{HRRQ}}$/HRRQ	J1
GND	J5	H2	N4	HRW	J2
GND	J6	H3	P3	$\overline{\text{HTRQ}}$/HTRQ	K2
GND	J7	H4	N3	$\overline{\text{HWR}}$/HWR	J3
GND	J8	H5	P2	$\overline{\text{IRQA}}$	C4
GND	J9	H6	N2	$\overline{\text{IRQB}}$	A5
GND	J10	H7	N2	$\overline{\text{IRQC}}$	C5
GND	J11	HA0	M3	$\overline{\text{IRQD}}$	B5

- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.
- If the temperature of the package case (T_T) is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation $(T_J - T_T)/P_D$.

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or Ψ_{JT}, has been defined to be $(T_J - T_T)/P_D$. This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

4.2 Electrical Design Considerations

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V_{CC}).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.
- Use at least four 0.01–0.1 µF bypass capacitors for V_{CCQL} (core) and at least six 0.01–0.1 µF bypass capacitors for the other V_{CC} (I/O) power connections positioned as closely as possible to the four sides of the package to connect the power sources to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V_{CC} and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, $\overline{\text{IRQD}}$, $\overline{\text{TA}}$, and $\overline{\text{BG}}$ pins. Maximum PCB trace lengths on the order of 6 inches are recommended.

```
M_HOD EQU $8                    ; Host Request Open Drain mode
M_HDSP EQU $9                   ; Host Data Strobe Polarity
M_HASP EQU $A                   ; Host Address Strobe Polarity
M_HMUX EQU $B                   ; Host Multiplexed bus select
M_HD_HS EQU $C                  ; Host Double/Single Strobe select
M_HCSP EQU $D                   ; Host Chip Select Polarity
M_HRP EQU $E                    ; Host Request Polarity
M_HAP EQU $F                    ; Host Acknowledge Polarity


;------------------------------------------------------------------------
;
;       EQUATES for Serial Communications Interface (SCI)
;
;------------------------------------------------------------------------

;       Register Addresses

M_STXH EQU $FFFF97              ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96              ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95              ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A              ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99              ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98              ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94              ; SCI Transmit Address Register
M_SCR EQU $FFFF9C               ; SCI Control Register
M_SSR EQU $FFFF93               ; SCI Status Register
M_SCCR EQU $FFFF9B              ; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7                    ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0                    ; Word Select 0
M_WDS1 EQU 1                    ; Word Select 1
M_WDS2 EQU 2                    ; Word Select 2
M_SSFTD EQU 3                   ; SCI Shift Direction
M_SBK EQU 4                     ; Send Break
M_WAKE EQU 5                    ; Wakeup Mode Select
M_RWU EQU 6                     ; Receiver Wakeup Enable
M_WOMS EQU 7                    ; Wired-OR Mode Select
M_SCRE EQU 8                    ; SCI Receiver Enable
M_SCTE EQU 9                    ; SCI Transmitter Enable
M_ILIE EQU 10                   ; Idle Line Interrupt Enable
M_SCRIE EQU 11                  ; SCI Receive Interrupt Enable
M_SCTIE EQU 12                  ; SCI Transmit Interrupt Enable
M_TMIE EQU 13                   ; Timer Interrupt Enable
M_TIR EQU 14                    ; Timer Interrupt Rate
M_SCKP EQU 15                   ; SCI Clock Polarity
M_REIE EQU 16                   ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0                    ; Transmitter Empty
M_TDRE EQU 1                    ; Transmit Data Register Empty
M_RDRF EQU 2                    ; Receive Data Register Full
M_IDLE EQU 3                    ; Idle Line Flag
M_OR EQU 4                      ; Overrun Error Flag
M_PE EQU 5                      ; Parity Error
M_FE EQU 6                      ; Framing Error Flag
M_R8 EQU 7                      ; Received Bit 8 (R8) Address

;       SCI Clock Control Register
```

```
M_IAL0 EQU 0                        ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1                        ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2                        ; IRQA Mode Trigger Mode
M_IBL EQU $38                       ; IRQB Mode Mask
M_IBL0 EQU 3                        ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4                        ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5                        ; IRQB Mode Trigger Mode
M_ICL EQU $1C0                      ; IRQC Mode Mask
M_ICL0 EQU 6                        ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7                        ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8                        ; IRQC Mode Trigger Mode
M_IDL EQU $E00                      ; IRQD Mode Mask
M_IDL0 EQU 9                        ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10                       ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11                       ; IRQD Mode Trigger Mode
M_D0L EQU $3000                     ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12                       ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13                       ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000                     ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14                       ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15                       ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000                    ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16                       ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17                       ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000                    ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18                       ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19                       ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000                   ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20                       ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21                       ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000                   ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22                       ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23                       ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3                        ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0                        ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1                        ; Host Interrupt Priority Level (high)
M_S0L EQU $C                        ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2                        ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3                        ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30                       ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4                        ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5                        ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0                       ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6                        ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7                        ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300                      ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8                        ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9                        ; TIMER Interrupt Priority Level (high)


;---------------------------------------------------------------------------
;
;       EQUATES for TIMER
;
;---------------------------------------------------------------------------

;       Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F                 ; Timer 0 Control/Status Register
```

```
M_TLR0 EQU  $FFFF8E              ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D              ; TIMER0 Compare Register
M_TCR0 EQU  $FFFF8C              ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B              ; TIMER1 Control/Status Register
M_TLR1 EQU  $FFFF8A              ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89              ; TIMER1 Compare Register
M_TCR1 EQU  $FFFF88              ; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87              ; TIMER2 Control/Status Register
M_TLR2 EQU  $FFFF86              ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85              ; TIMER2 Compare Register
M_TCR2 EQU  $FFFF84              ; TIMER2 Count Register
M_TPLR EQU  $FFFF83              ; TIMER Prescaler Load Register
M_TPCR EQU  $FFFF82              ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0                       ; Timer Enable
M_TOIE EQU 1                     ; Timer Overflow Interrupt Enable
M_TCIE EQU 2                     ; Timer Compare Interrupt Enable
M_TC EQU $F0                     ; Timer Control Mask (TC0-TC3)
M_INV EQU 8                      ; Inverter Bit
M_TRM EQU 9                      ; Timer Restart Mode
M_DIR EQU 11                     ; Direction Bit
M_DI EQU 12                      ; Data Input
M_DO EQU 13                      ; Data Output
M_PCE EQU  15                    ; Prescaled Clock Enable
M_TOF EQU 20                     ; Timer Overflow Flag
M_TCF EQU 21                     ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000                ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4                      ; Timer Control 0
M_TC1 EQU 5                      ; Timer Control 1
M_TC2 EQU 6                      ; Timer Control 2
M_TC3 EQU 7                      ; Timer Control 3


;---------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;---------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                ; DMA Status Register
M_DOR0 EQU $FFFFF3               ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2               ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1               ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0               ; DMA Offset Register 3
```

Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
DSP56321	1.6 V core 3.3 V I/O	Molded Array Process-Ball Grid Array (MAP-BGA)	196	200	Lead-free	DSP56321VL200
					Lead-bearing	DSP56321VF200
				220	Lead-free	DSP56321VL220
					Lead-bearing	DSP56321VF220
				240	Lead-free	DSP56321VL240
					Lead-bearing	DSP56321VF240
				275	Lead-free	DSP56321VL275
					Lead-bearing	DSP56321VF275

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Document Order No.: DSP56321
Rev. 11
2/2005