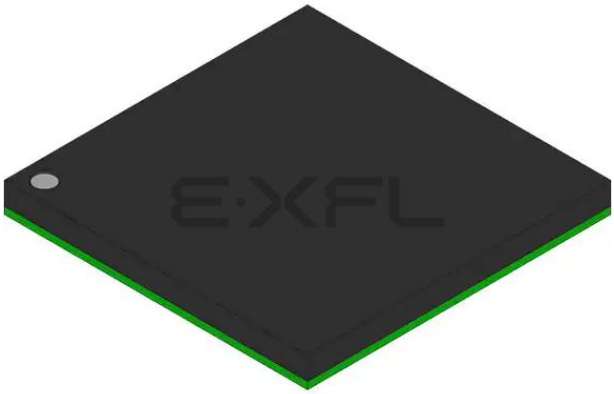

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Active
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	240MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=dsp56321vf240

Signals/Connections 1

The DSP56321 input and output signals are organized into functional groups as shown in **Table 1-1**. **Figure 1-1** diagrams the DSP56321 signals by functional group. The remainder of this chapter describes the signal pins in each functional group.

Table 1-1. DSP56321 Functional Signal Groupings

Functional Group		Number of Signals
Power (V_{CC})		20
Ground (GND)		66
Clock		2
Address bus	Port A[1]	18
Data bus		24
Bus control		10
Interrupt and mode control		6
Host interface (HI08)	Port B[2]	16
Enhanced synchronous serial interface (ESSI)	Ports C and D[3]	12
Serial communication interface (SCI)	Port E[4]	3
Timer		3
OnCE/JTAG Port		6

Notes:
1. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
2. Port B signals are the HI08 port signals multiplexed with the GPIO signals.
3. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
4. Port E signals are the SCI port signals multiplexed with the GPIO signals.
5. Eight signal lines are not connected internally. These are designated as no connect (NC) in the package description (see **Chapter 3**). There are also two reserved lines.

Note: This chapter refers to a number of configuration registers used to select individual multiplexed signal functionality. See the *DSP56321 Reference Manual* for details on these configuration registers.

1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V_{CCQL}	**Quiet Core (Low) Power**—An isolated power for the core processing and clock logic. This input must be isolated externally from all other chip power inputs.
V_{CCQH}	**Quiet External (High) Power**—A quiet power source for I/O lines. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCA}	**Address Bus Power**—An isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCD}	**Data Bus Power**—An isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCC}	**Bus Control Power**—An isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCH}	**Host Power**—An isolated power for the HI08 I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
V_{CCS}	**ESSI, SCI, and Timer Power**—An isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs, *except* V_{CCQL}.
Note: The user must provide adequate external decoupling capacitors for all power connections.	

1.2 Ground

Table 1-3. Grounds

Name	Description
GND	**Ground**—Connected to an internal device ground plane.
Note: The user must provide adequate external decoupling capacitors for all GND connections.	

1.3 Clock

Table 1-4. Clock Signals

Signal Name	Type	State During Reset	Signal Description
EXTAL	Input	Input	**External Clock/Crystal Input**—Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	**Crystal Output**—Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

Table 1-13. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Timers

The DSP56321 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56321 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-14. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

2.2 Thermal Characteristics

Table 2-2. Thermal Characteristics

Thermal Resistance Characteristic	Symbol	MAP-BGA Value	Unit
Junction-to-ambient, natural convection, single-layer board (1s)[1,2]	$R_{\theta JA}$	44	°C/W
Junction-to-ambient, natural convection, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	25	°C/W
Junction-to-ambient, @200 ft/min air flow, single-layer board (1s)[1,3]	$R_{\theta JMA}$	35	°C/W
Junction-to-ambient, @200 ft/min air flow, four-layer board (2s2p)[1,3]	$R_{\theta JMA}$	22	°C/W
Junction-to-board[4]	$R_{\theta JB}$	13	°C/W
Junction-to-case thermal resistance[5]	$R_{\theta JC}$	7	°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

2.3 DC Electrical Characteristics

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Supply voltage[1]: • Core (V_{CCQL}) • I/O (V_{CCQH}, V_{CCA}, V_{CCD}, V_{CCC}, V_{CCH}, and V_{CCS})		 1.5 3.0	 1.6 3.3	 1.7 3.6	 V V
Input high voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$ • MOD/$\overline{IRQ}$[2] $\overline{RESET}$, PINIT/$\overline{NMI}$ and all JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IH} V_{IHP} V_{IHX}	 2.0 2.0 $0.8 \times V_{CCQH}$	 — — —	 $V_{CCQH} + 0.3$ $V_{CCQH} + 0.3$ V_{CCQH}	 V V V
Input low voltage • D[0–23], $\overline{BG}$, $\overline{BB}$, $\overline{TA}$, MOD/$\overline{IRQ}$[2], $\overline{RESET}$, PINIT • All JTAG/ESSI/SCI/Timer/HI08 pins • EXTAL[9]	 V_{IL} V_{ILP} V_{ILX}	 –0.3 –0.3 –0.3	 — — —	 0.8 0.8 $0.2 \times V_{CCQH}$	 V V V
Input leakage current	I_{IN}	–10	—	10	µA
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I_{TSI}	–10	—	10	µA
Output high voltage[8] • TTL (I_{OH} = –0.4 mA)[6] • CMOS (I_{OH} = –10 µA)[6]	V_{OH}	 2.4 $V_{CCQH} - 0.01$	 — —	 — —	 V V
Output low voltage[8] • TTL (I_{OL} = 3.0 mA)[6] • CMOS (I_{OL} = 10 µA)[6]	V_{OL}	 — —	 — —	 0.4 0.01	 V V

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7]	(WS + 3.25) × T_C – 10.94	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7] • SRAM WS = 3 • SRAM WS ≥ 4	 (WS + 3) × T_C – 10.94 (WS + 2.5) × T_C – 10.94	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 ns ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		8.0	—	8.0	—	8.0	—	8.0	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop (PCTL Bit 1 = 1; Implies No Stop Delay)	 DPLT + (128K × T_C) DPLT + (23.75 ± 0.5) × T_C (10.0 ± 1.75) × T_C	 662.2 µs 6.9 41.25	 209.9 ms 188.8 58.8	 662.2 µs 6.9 37.5	 209.9 ms 188.8 53.3	 662.2 µs 6.9 34.4	 209.9 ms 188.8 49.0	 662.2 µs 6.9 30.0	 209.9 ms 188.8 43.0	 — µs ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop ((PCTL bit 1 = 0; implies no Stop delay)	 DPLT + (128 K × T_C) DPLT + (20.5 ± 0.5) × T_C 5.5 × T_C	 805.4 150.1 27.5	 — — —	 805.4 150.1 25	 — — —	 805.4 150.1 22.9	 — — —	 805.4 150.1 20.0	 — — —	 µs µs ns
27	Interrupt Request Rate • HI08, ESSI, SCI, Timer • DMA • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) • $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	 12T_C 8T_C 8T_C 12T_C	 — — — —	 60.0 40.0 40.0 60.0	 — — — —	 54.6 36.4 36.4 54.6	 — — — —	 50.0 33.4 33.4 50.0	 — — — —	 43.7 29.2 29.2 43.7	 ns ns ns ns
28	DMA Request Rate • Data read from HI08, ESSI, SCI • Data write to HI08, ESSI, SCI • Timer • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	 6T_C 7T_C 2T_C 3T_C	 — — — —	 30.0 35.0 10.0 15.0	 — — — —	 27.3 31.9 9.1 13.7	 — — — —	 25.0 29.2 8.3 12.5	 — — — —	 21.84 25.48 7.28 10.92	 ns ns ns ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	4.25 × T_C + 2.0	23.25	—	21.34	—	19.72	—	17.45	—	ns

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	

Notes:

1. When fast interrupts are used and $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$, $\overline{\text{IRQC}}$, and $\overline{\text{IRQD}}$ are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when fast interrupts are used. Long interrupts are recommended for Level-sensitive mode.
2. This timing depends on several settings:
   • For DPLL disable, using internal oscillator (DPLL Control Register (PCTL) Bit 2 = 0) and oscillator disabled during Stop (PCTL Bit 1 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
   • For DPLL disable, using internal oscillator (PCTL Bit 2 = 0) and oscillator enabled during Stop (PCTL Bit 1 = 1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
   • For DPLL disable, using external clock (PCTL Bit 2 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 1 and Operating Mode Register Bit 6 settings.
   • For DPLL enable, if PCTL Bit 1 is 0, the DPLL is shut down during Stop. Recovering from Stop requires the DPLL to lock. The DPLL lock procedure duration is defined in **Table 2-6** and will be refined after silicon characterization. This procedure is followed by the stop delay counter. Stop recovery ends when the stop delay counter completes its count.
   • The DPLT value for DPLL disable is 0.
3. Periodically sampled and not 100 percent tested.
4. For an external clock generator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.
   For an internal oscillator, $\overline{\text{RESET}}$ duration is measured while $\overline{\text{RESET}}$ is asserted and V_{CC} is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
   When the V_{CC} is valid, but the other "required $\overline{\text{RESET}}$ duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
5. V_{CCQH} = 3.3 V ±0.3 V, V_{CCQL} = 1.6 V ±0.1 V; T_J = –40°C to +100°C, C_L = 50 pF.
6. WS = number of wait states (measured in clock cycles, number of T_C).
7. Use the expression to compute a maximum value.

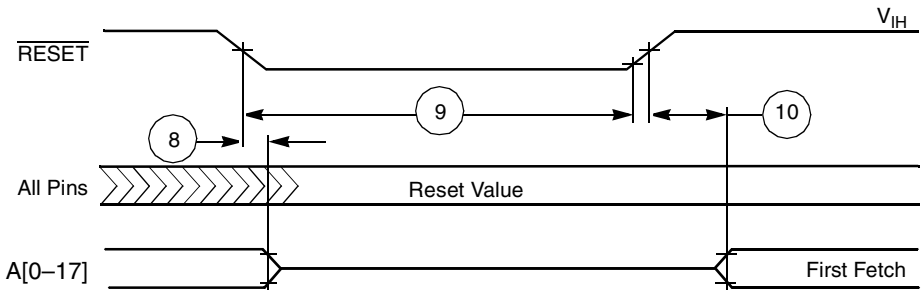
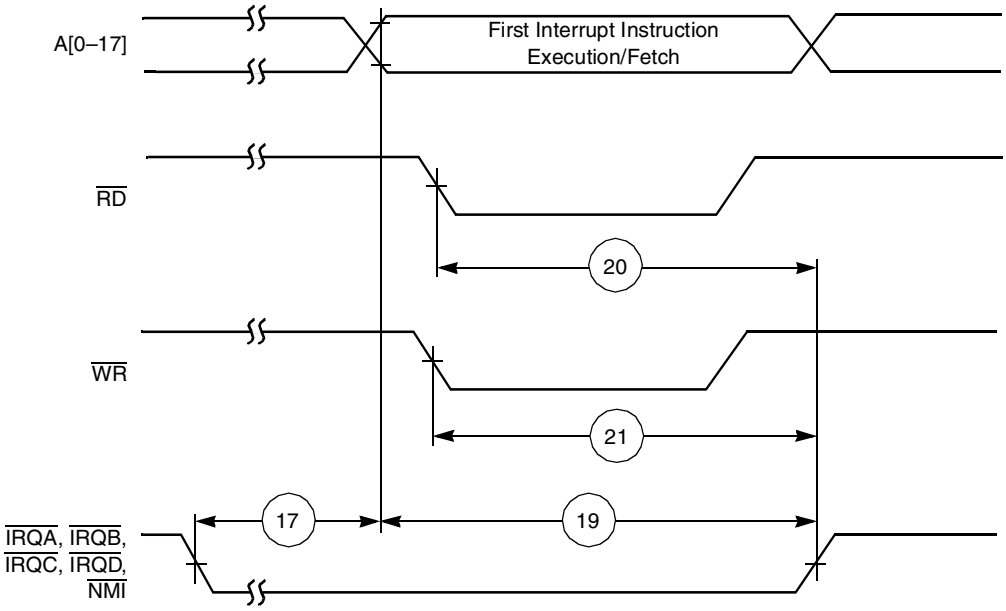
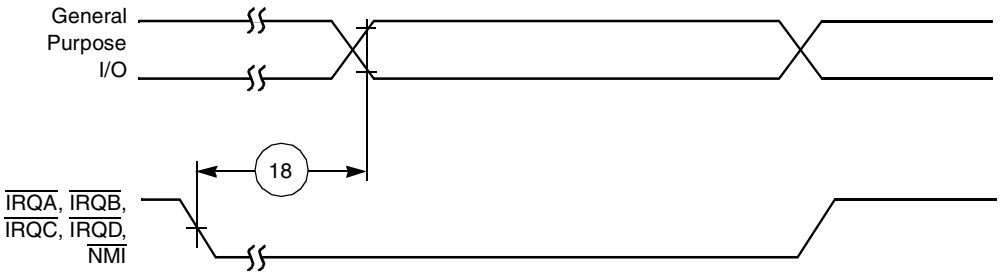


Figure 2-3. Reset Timing



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

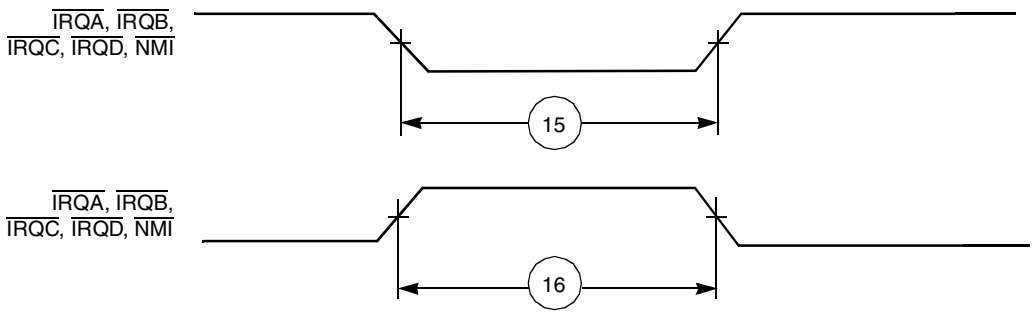
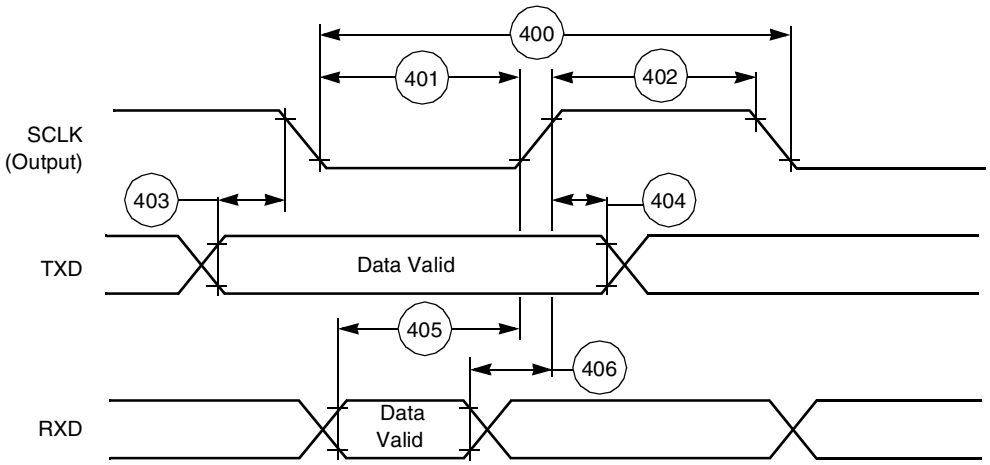
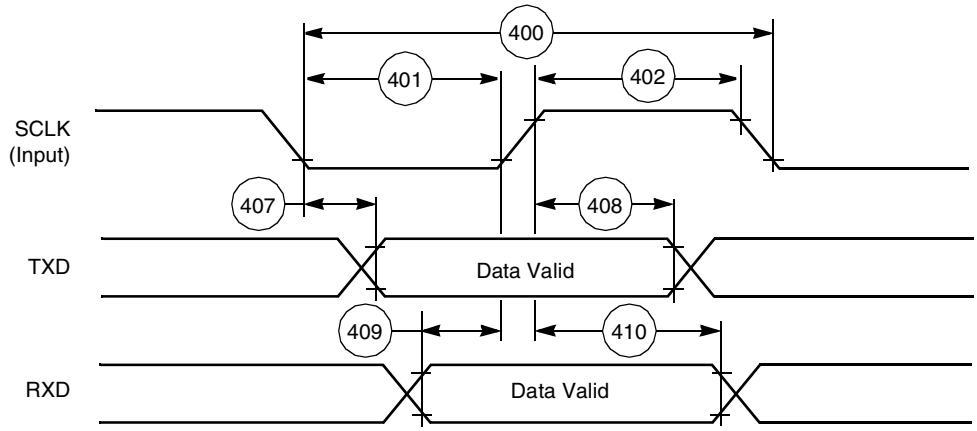


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)



a) Internal Clock



b) External Clock

Figure 2-22. SCI Synchronous Mode Timing

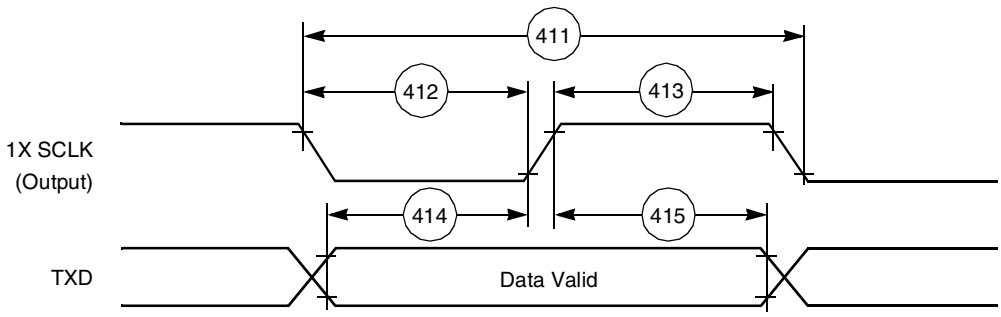


Figure 2-23. SCI Asynchronous Mode Timing

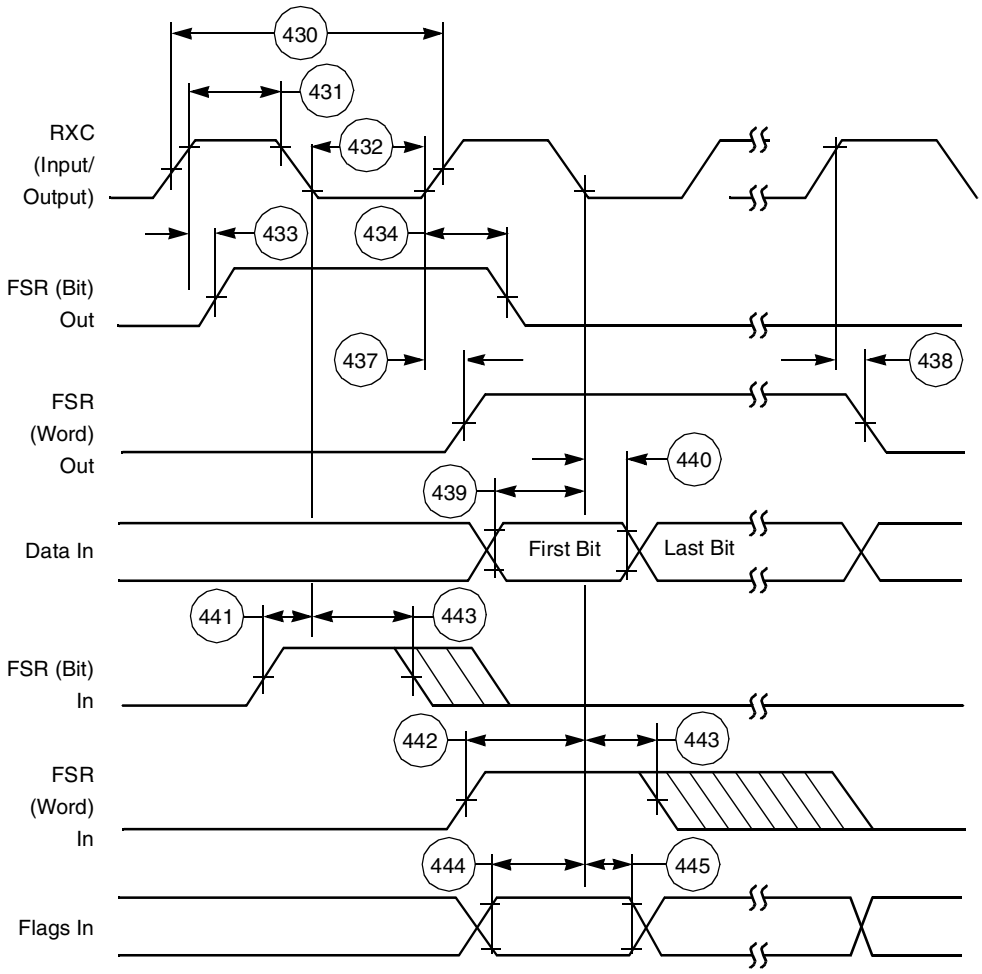


Figure 2-25. ESSI Receiver Timing

2.4.9 Timer Timing

Table 2-13. Timer Timings

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		240 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
480	TIO Low	$2 \times T_C + 2.0$	12.0	—	11.1	—	10.3	—	9.27	—	ns
481	TIO High	$2 \times T_C + 2.0$	12.0	—	11.1	—	10.3	—	9.27	—	ns
486	Synchronous delay time from Timer input rising edge to the external memory address out valid caused by the first interrupt instruction execution	$10.25 \times T_C + 10.0$	61.25	—	56.64	—	52.74	—	47.27	—	ns

Notes:
1. V_{CCQH} = 3.3 V ±0.3 V, V_{CCQL} = 1.6 V ± 0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
2. The maximum frequency of pulses generated by a timer will be defined after device characterization is completed.
3. In the timing diagrams below, TIO is drawn using the rising edge as the reference. TIO polarity is programmable in the Timer Control/Status Register (TCSR). Refer to the *DSP56321 Reference Manual* for details.

Packaging 3

This section includes diagrams of the DSP56321 package pin-outs and tables showing how the signals described in **Chapter 1** are allocated for the package. The DSP56321 is available in a 196-pin molded array plastic-ball grid array (MAP-BGA) package.

Table 3-1. Signal List by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	Not Connected (NC)	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-2. Signal List by Signal Name

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
A0	N14	$\overline{BR}$	N11	D9	A12
A1	M13	D0	E14	$\overline{DE}$	D3
A10	H13	D1	D12	EXTAL	M8
A11	H14	D10	B11	GND	D4
A12	G14	D11	A11	GND	D5
A13	G12	D12	C10	GND	D6
A14	F13	D13	B10	GND	D7
A15	F14	D14	A10	GND	D8
A16	E13	D15	B9	GND	D9
A17	E12	D16	A9	GND	D10
A2	M14	D17	B8	GND	D11
A3	L13	D18	C8	GND	E4
A4	L14	D19	A8	GND	E5
A5	K13	D2	D13	GND	E6
A6	K14	D20	B7	GND	E7
A7	J13	D21	B6	GND	E8
A8	J12	D22	C6	GND	E9
A9	J14	D23	A6	GND	E10
AA0	N13	D3	C13	GND	E11
AA1	P12	D4	C14	GND	F4
AA2	P7	D5	B13	GND	F5
AA3	N7	D6	C12	GND	F6
$\overline{BB}$	P11	D7	A13	GND	F7
$\overline{BG}$	P13	D8	B12	GND	F8

Table 3-2. Signal List by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
GND	F9	GND	K4	HA1	M1
GND	F10	GND	K5	HA10	L1
GND	F11	GND	K6	HA2	M2
GND	G4	GND	K7	HA8	M1
GND	G5	GND	K8	HA9	M2
GND	G6	GND	K9	$\overline{\text{HACK}}$/HACK	J1
GND	G7	GND	K10	HAD0	M5
GND	G8	GND	K11	HAD1	P4
GND	G9	GND	L4	HAD2	N4
GND	G10	GND	L5	HAD3	P3
GND	G11	GND	L6	HAD4	N3
GND	H4	GND	L7	HAD5	P2
GND	H5	GND	L8	HAD6	N1
GND	H6	GND	L9	HAD7	N2
GND	H7	GND	L10	$\overline{\text{HAS}}$/HAS	M3
GND	H8	GND	L11	$\overline{\text{HCS}}$/HCS	L1
GND	H9	GND	N6	$\overline{\text{HDS}}$/HDS	J3
GND	H10	GND	P6	$\overline{\text{HRD}}$/HRD	J2
GND	H11	H0	M5	$\overline{\text{HREQ}}$/HREQ	K2
GND	J4	H1	P4	$\overline{\text{HRRQ}}$/HRRQ	J1
GND	J5	H2	N4	HRW	J2
GND	J6	H3	P3	$\overline{\text{HTRQ}}$/HTRQ	K2
GND	J7	H4	N3	$\overline{\text{HWR}}$/HWR	J3
GND	J8	H5	P2	$\overline{\text{IRQA}}$	C4
GND	J9	H6	N2	$\overline{\text{IRQB}}$	A5
GND	J10	H7	N2	$\overline{\text{IRQC}}$	C5
GND	J11	HA0	M3	$\overline{\text{IRQD}}$	B5

```
        dc      $C2B639
        dc      $85A47E
        dc      $ABFDDF
        dc      $F3A2C
        dc      $2D7CF5
        dc      $E16A8A
        dc      $ECB8FB
        dc      $4BED18
        dc      $43F371
        dc      $83A556
        dc      $E1E9D7
        dc      $ACA2C4
        dc      $8135AD
        dc      $2CE0E2
        dc      $8F2C73
        dc      $432730
        dc      $A87FA9
        dc      $4A292E
        dc      $A63CCF
        dc      $6BA65C
        dc      $E06D65
        dc      $1AA3A
        dc      $A1B6EB
        dc      $48AC48
        dc      $EF7AE1
        dc      $6E3006
        dc      $62F6C7
        dc      $6064F4
        dc      $87E41D
        dc      $CB2692
        dc      $2C3863
        dc      $C6BC60
        dc      $43A519
        dc      $6139DE
        dc      $ADF7BF
        dc      $4B3E8C
        dc      $6079D5
        dc      $E0F5EA
        dc      $8230DB
        dc      $A3B778
        dc      $2BFE51
        dc      $E0A6B6
        dc      $68FFB7
        dc      $28F324
        dc      $8F2E8D
        dc      $667842
        dc      $83E053
        dc      $A1FD90
        dc      $6B2689
        dc      $85B68E
        dc      $622EAF
        dc      $6162BC
        dc      $E4A245
YDAT_END

;*************************************************************************
;
;     EQUATES for DSP56321 I/O registers and ports
;
;*************************************************************************

        page    132,55,0,0,0
        opt     mex
```

```
M_HOD EQU $8                    ; Host Request Open Drain mode
M_HDSP EQU $9                   ; Host Data Strobe Polarity
M_HASP EQU $A                   ; Host Address Strobe Polarity
M_HMUX EQU $B                   ; Host Multiplexed bus select
M_HD_HS EQU $C                  ; Host Double/Single Strobe select
M_HCSP EQU $D                   ; Host Chip Select Polarity
M_HRP EQU $E                    ; Host Request Polarity
M_HAP EQU $F                    ; Host Acknowledge Polarity


;------------------------------------------------------------------------
;
;       EQUATES for Serial Communications Interface (SCI)
;
;------------------------------------------------------------------------

;       Register Addresses

M_STXH EQU $FFFF97              ; SCI Transmit Data Register (high)
M_STXM EQU $FFFF96              ; SCI Transmit Data Register (middle)
M_STXL EQU $FFFF95              ; SCI Transmit Data Register (low)
M_SRXH EQU $FFFF9A              ; SCI Receive Data Register (high)
M_SRXM EQU $FFFF99              ; SCI Receive Data Register (middle)
M_SRXL EQU $FFFF98              ; SCI Receive Data Register (low)
M_STXA EQU $FFFF94              ; SCI Transmit Address Register
M_SCR EQU $FFFF9C               ; SCI Control Register
M_SSR EQU $FFFF93               ; SCI Status Register
M_SCCR EQU $FFFF9B              ; SCI Clock Control Register

;       SCI Control Register Bit Flags

M_WDS EQU $7                    ; Word Select Mask (WDS0-WDS3)
M_WDS0 EQU 0                    ; Word Select 0
M_WDS1 EQU 1                    ; Word Select 1
M_WDS2 EQU 2                    ; Word Select 2
M_SSFTD EQU 3                   ; SCI Shift Direction
M_SBK EQU 4                     ; Send Break
M_WAKE EQU 5                    ; Wakeup Mode Select
M_RWU EQU 6                     ; Receiver Wakeup Enable
M_WOMS EQU 7                    ; Wired-OR Mode Select
M_SCRE EQU 8                    ; SCI Receiver Enable
M_SCTE EQU 9                    ; SCI Transmitter Enable
M_ILIE EQU 10                   ; Idle Line Interrupt Enable
M_SCRIE EQU 11                  ; SCI Receive Interrupt Enable
M_SCTIE EQU 12                  ; SCI Transmit Interrupt Enable
M_TMIE EQU 13                   ; Timer Interrupt Enable
M_TIR EQU 14                    ; Timer Interrupt Rate
M_SCKP EQU 15                   ; SCI Clock Polarity
M_REIE EQU 16                   ; SCI Error Interrupt Enable (REIE)

;       SCI Status Register Bit Flags

M_TRNE EQU 0                    ; Transmitter Empty
M_TDRE EQU 1                    ; Transmit Data Register Empty
M_RDRF EQU 2                    ; Receive Data Register Full
M_IDLE EQU 3                    ; Idle Line Flag
M_OR EQU 4                      ; Overrun Error Flag
M_PE EQU 5                      ; Parity Error
M_FE EQU 6                      ; Framing Error Flag
M_R8 EQU 7                      ; Received Bit 8 (R8) Address

;       SCI Clock Control Register
```

```
M_CD EQU $FFF                       ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                        ; Clock Out Divider
M_SCP EQU 13                        ; Clock Prescaler
M_RCM EQU 14                        ; Receive Clock Mode Source Bit
M_TCM EQU 15                        ; Transmit Clock Source Bit

;-------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;-------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                  ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                  ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                  ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                  ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                   ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                  ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                  ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                 ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                 ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                 ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                 ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                  ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                  ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                  ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                  ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                   ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                  ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                  ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                 ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                 ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                 ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                 ; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF                        ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                        ; Prescaler Range
M_DC EQU $1F000                     ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18                        ; Alignment Control (ALC)
M_WL EQU $380000                    ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22                       ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3                         ; Serial Output Flag Mask
M_OF0 EQU 0                         ; Serial Output Flag 0
M_OF1 EQU 1                         ; Serial Output Flag 1
M_SCD EQU $1C                       ; Serial Control Direction Mask
M_SCD0 EQU 2                        ; Serial Control 0 Direction
M_SCD1 EQU 3                        ; Serial Control 1 Direction
M_SCD2 EQU 4                        ; Serial Control 2 Direction
M_SCKD EQU 5                        ; Clock Source Direction
M_SHFD EQU 6                        ; Shift Direction
M_FSL EQU $180                      ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7                        ; Frame Sync Length 0
```

```
M_IAL0 EQU 0                        ; IRQA Mode Interrupt Priority Level (low)
M_IAL1 EQU 1                        ; IRQA Mode Interrupt Priority Level (high)
M_IAL2 EQU 2                        ; IRQA Mode Trigger Mode
M_IBL EQU $38                       ; IRQB Mode Mask
M_IBL0 EQU 3                        ; IRQB Mode Interrupt Priority Level (low)
M_IBL1 EQU 4                        ; IRQB Mode Interrupt Priority Level (high)
M_IBL2 EQU 5                        ; IRQB Mode Trigger Mode
M_ICL EQU $1C0                      ; IRQC Mode Mask
M_ICL0 EQU 6                        ; IRQC Mode Interrupt Priority Level (low)
M_ICL1 EQU 7                        ; IRQC Mode Interrupt Priority Level (high)
M_ICL2 EQU 8                        ; IRQC Mode Trigger Mode
M_IDL EQU $E00                      ; IRQD Mode Mask
M_IDL0 EQU 9                        ; IRQD Mode Interrupt Priority Level (low)
M_IDL1 EQU 10                       ; IRQD Mode Interrupt Priority Level (high)
M_IDL2 EQU 11                       ; IRQD Mode Trigger Mode
M_D0L EQU $3000                     ; DMA0 Interrupt priority Level Mask
M_D0L0 EQU 12                       ; DMA0 Interrupt Priority Level (low)
M_D0L1 EQU 13                       ; DMA0 Interrupt Priority Level (high)
M_D1L EQU $C000                     ; DMA1 Interrupt Priority Level Mask
M_D1L0 EQU 14                       ; DMA1 Interrupt Priority Level (low)
M_D1L1 EQU 15                       ; DMA1 Interrupt Priority Level (high)
M_D2L EQU $30000                    ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16                       ; DMA2 Interrupt Priority Level (low)
M_D2L1 EQU 17                       ; DMA2 Interrupt Priority Level (high)
M_D3L EQU $C0000                    ; DMA3 Interrupt Priority Level Mask
M_D3L0 EQU 18                       ; DMA3 Interrupt Priority Level (low)
M_D3L1 EQU 19                       ; DMA3 Interrupt Priority Level (high)
M_D4L EQU $300000                   ; DMA4 Interrupt priority Level Mask
M_D4L0 EQU 20                       ; DMA4 Interrupt Priority Level (low)
M_D4L1 EQU 21                       ; DMA4 Interrupt Priority Level (high)
M_D5L EQU $C00000                   ; DMA5 Interrupt priority Level Mask
M_D5L0 EQU 22                       ; DMA5 Interrupt Priority Level (low)
M_D5L1 EQU 23                       ; DMA5 Interrupt Priority Level (high)


;       Interrupt Priority Register Peripheral (IPRP)

M_HPL EQU $3                        ; Host Interrupt Priority Level Mask
M_HPL0 EQU 0                        ; Host Interrupt Priority Level (low)
M_HPL1 EQU 1                        ; Host Interrupt Priority Level (high)
M_S0L EQU $C                        ; SSI0 Interrupt Priority Level Mask
M_S0L0 EQU 2                        ; SSI0 Interrupt Priority Level (low)
M_S0L1 EQU 3                        ; SSI0 Interrupt Priority Level (high)
M_S1L EQU $30                       ; SSI1 Interrupt Priority Level Mask
M_S1L0 EQU 4                        ; SSI1 Interrupt Priority Level (low)
M_S1L1 EQU 5                        ; SSI1 Interrupt Priority Level (high)
M_SCL EQU $C0                       ; SCI  Interrupt Priority Level  Mask
M_SCL0 EQU 6                        ; SCI  Interrupt Priority Level  (low)
M_SCL1 EQU 7                        ; SCI  Interrupt Priority Level  (high)
M_T0L EQU $300                      ; TIMER Interrupt Priority Level Mask
M_T0L0 EQU 8                        ; TIMER Interrupt Priority Level (low)
M_T0L1 EQU 9                        ; TIMER Interrupt Priority Level (high)


;---------------------------------------------------------------------------
;
;       EQUATES for TIMER
;
;---------------------------------------------------------------------------

;       Register Addresses Of TIMER0

M_TCSR0 EQU $FFFF8F                 ; Timer 0 Control/Status Register
```

```
M_PCOD    EQU     0               ; PLL Clock Output Disable Bit
M_PSTP    EQU     1               ; STOP Processing State Bit
M_XTLD    EQU     2               ; XTAL Disable Bit
M_PEN     EQU     3               ; PLL Enable Bit

;------------------------------------------------------------------------
;
;       EQUATES for BIU
;
;------------------------------------------------------------------------

;       Register Addresses Of BIU


M_BCR EQU $FFFFFB               ; Bus Control Register
M_DCR EQU $FFFFFA               ; DRAM Control Register
M_AAR0 EQU $FFFFF9              ; Address Attribute Register 0
M_AAR1 EQU $FFFFF8              ; Address Attribute Register 1
M_AAR2 EQU $FFFFF7              ; Address Attribute Register 2
M_AAR3 EQU $FFFFF6              ; Address Attribute Register 3
M_IDR EQU  $FFFFF5              ; ID Register

;       Bus Control Register

M_BA0W EQU $1F                  ; Area 0 Wait Control Mask (BA0W0-BA0W4)
M_BA1W EQU $3E0                 ; Area 1 Wait Control Mask (BA1W0-BA14)
M_BA2W EQU $1C00                ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M_BA3W EQU $E000                ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M_BDFW EQU $1F0000              ; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21                    ; Bus State
M_BLH EQU 22                    ; Bus Lock Hold
M_BRH EQU 23                    ; Bus Request Hold

;       DRAM Control Register

M_BCW EQU $3                    ; In Page Wait States Bits Mask (BCW0-BCW1)
M_BRW EQU $C                    ; Out Of Page Wait States Bits Mask (BRW0-BRW1)
M_BPS EQU $300                  ; DRAM Page Size Bits Mask (BPS0-BPS1)
M_BPLE EQU 11                   ; Page Logic Enable
M_BME EQU 12                    ; Mastership Enable
M_BRE EQU 13                    ; Refresh Enable
M_BSTR EQU 14                   ; Software Triggered Refresh
M_BRF EQU $7F8000               ; Refresh Rate Bits Mask (BRF0-BRF7)
M_BRP EQU 23                    ; Refresh prescaler

;       Address Attribute Registers

M_BAT EQU $3                    ; Ext. Access Type and Pin Def. Bits Mask (BAT0-BAT1)
M_BAAP EQU 2                    ; Address Attribute Pin Polarity
M_BPEN EQU 3                    ; Program Space Enable
M_BXEN EQU 4                    ; X Data Space Enable
M_BYEN EQU 5                    ; Y Data Space Enable
M_BAM EQU 6                     ; Address Muxing
M_BPAC EQU 7                    ; Packing Enable
M_BNC EQU $F00                  ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M_BAC EQU $FFF000               ; Address to Compare Bits Mask (BAC0-BAC11)


;       control and status bits in SR

M_CP EQU $c00000                ; mask for CORE-DMA priority bits in SR
M_CA EQU 0                      ; Carry
M_V EQU 1                       ; Overflow
```

```
;---------------------------------------------------------------------
; Non-Maskable interrupts
;---------------------------------------------------------------------
I_RESET EQU I_VEC+$00             ; Hardware RESET
I_STACK EQU I_VEC+$02             ; Stack Error
I_ILL EQU I_VEC+$04               ; Illegal Instruction
I_DBG EQU I_VEC+$06               ; Debug Request
I_TRAP EQU I_VEC+$08              ; Trap
I_NMI EQU I_VEC+$0A               ; Non Maskable Interrupt

;---------------------------------------------------------------------
; Interrupt Request Pins
;---------------------------------------------------------------------
I_IRQA EQU I_VEC+$10              ; IRQA
I_IRQB EQU I_VEC+$12              ; IRQB
I_IRQC EQU I_VEC+$14              ; IRQC
I_IRQD EQU I_VEC+$16              ; IRQD

;---------------------------------------------------------------------
; DMA Interrupts
;---------------------------------------------------------------------
I_DMA0 EQU I_VEC+$18              ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A              ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C              ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E              ; DMA Channel 3
I_DMA4 EQU I_VEC+$20              ; DMA Channel 4
I_DMA5 EQU I_VEC+$22              ; DMA Channel 5

;---------------------------------------------------------------------
; Timer Interrupts
;---------------------------------------------------------------------
I_TIM0C EQU I_VEC+$24             ; TIMER 0 compare
I_TIM0OF EQU I_VEC+$26            ; TIMER 0 overflow
I_TIM1C EQU I_VEC+$28             ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A            ; TIMER 1 overflow
I_TIM2C EQU I_VEC+$2C             ; TIMER 2 compare
I_TIM2OF EQU I_VEC+$2E            ; TIMER 2 overflow

;---------------------------------------------------------------------
; ESSI Interrupts
;---------------------------------------------------------------------
I_SI0RD EQU I_VEC+$30             ; ESSI0 Receive Data
I_SI0RDE EQU I_VEC+$32            ; ESSI0 Receive Data w/ exception Status
I_SI0RLS EQU I_VEC+$34            ; ESSI0 Receive last slot
I_SI0TD EQU I_VEC+$36             ; ESSI0 Transmit data
I_SI0TDE EQU I_VEC+$38            ; ESSI0 Transmit Data w/ exception Status
I_SI0TLS EQU I_VEC+$3A            ; ESSI0 Transmit last slot
I_SI1RD EQU I_VEC+$40             ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42            ; ESSI1 Receive Data w/ exception Status
I_SI1RLS EQU I_VEC+$44            ; ESSI1 Receive last slot
I_SI1TD EQU I_VEC+$46             ; ESSI1 Transmit data
I_SI1TDE EQU I_VEC+$48            ; ESSI1 Transmit Data w/ exception Status
I_SI1TLS EQU I_VEC+$4A            ; ESSI1 Transmit last slot

;---------------------------------------------------------------------
; SCI Interrupts
;---------------------------------------------------------------------
I_SCIRD EQU I_VEC+$50             ; SCI Receive Data
I_SCIRDE EQU I_VEC+$52            ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54             ; SCI Transmit Data
I_SCIIL EQU I_VEC+$56             ; SCI Idle Line
I_SCITM EQU I_VEC+$58             ; SCI Timer
```