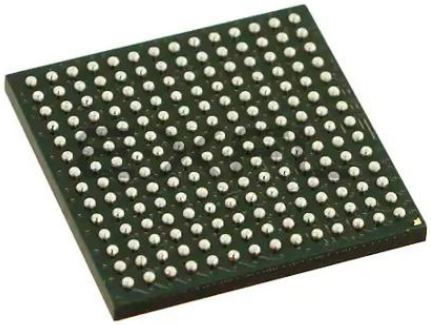

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	240MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp321vf240

Table of Contents

Data Sheet Conventions

$\overline{\text{OVERBAR}}$	Indicates a signal that is active when pulled low (For example, the $\overline{\text{RESET}}$ pin is active when low.)
“asserted”	Means that a high true (active high) signal is high or that a low true (active low) signal is low
“deasserted”	Means that a high true (active high) signal is low or that a low true (active low) signal is high

Examples:	Signal/Symbol	Logic State	Signal State	Voltage
	$\overline{\text{PIN}}$	True	Asserted	V_{IL}/V_{OL}
	$\overline{\text{PIN}}$	False	Deasserted	V_{IH}/V_{OH}
	PIN	True	Asserted	V_{IH}/V_{OH}
	PIN	False	Deasserted	V_{IL}/V_{OL}

Note: Values for V_{IL}, V_{OL}, V_{IH}, and V_{OH} are defined by individual product specifications.

Table 1. DSP56321 Features (Continued)

<table>
<tr><th>Feature</th><th>Description</th></tr>
<tr><td>Internal Memories</td><td>
• 192 × 24-bit bootstrap ROM
• 192 K × 24-bit RAM total
• Program RAM, instruction cache, X data RAM, and Y data RAM sizes are programmable:
<table>
<tr><th>Program RAM Size</th><th>Instruction Cache Size</th><th>X Data RAM Size*</th><th>Y Data RAM Size*</th><th>Instruction Cache</th><th>MSW2</th><th>MSW1</th><th>MSW0</th></tr>
<tr><td>32 K × 24-bit</td><td>0</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>31 K × 24-bit</td><td>1024 × 24-bit</td><td>80 K × 24-bit</td><td>80 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>40 K × 24-bit</td><td>0</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>disabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>39 K × 24-bit</td><td>1024 × 24-bit</td><td>76 K × 24-bit</td><td>76 K × 24-bit</td><td>enabled</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>48 K × 24-bit</td><td>0</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>47 K × 24-bit</td><td>1024 × 24-bit</td><td>72 K × 24-bit</td><td>72 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>64 K × 24-bit</td><td>0</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>disabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>63 K × 24-bit</td><td>1024 × 24-bit</td><td>64 K × 24-bit</td><td>64 K × 24-bit</td><td>enabled</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>72 K × 24-bit</td><td>0</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>71 K × 24-bit</td><td>1024 × 24-bit</td><td>60 K × 24-bit</td><td>60 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>80 K × 24-bit</td><td>0</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>disabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>79 K × 24-bit</td><td>1024 × 24-bit</td><td>56 K × 24-bit</td><td>56 K × 24-bit</td><td>enabled</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>96 K × 24-bit</td><td>0</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>95 K × 24-bit</td><td>1024 × 24-bit</td><td>48 K × 24-bit</td><td>48 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>112 K × 24-bit</td><td>0</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>disabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>111 K × 24-bit</td><td>1024 × 24-bit</td><td>40 K × 24-bit</td><td>40 K × 24-bit</td><td>enabled</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td colspan="8">*Includes 12 K × 24-bit shared memory (that is, 24 K total memory shared by the core and the EFCOP)</td></tr>
</table>
</td></tr>
<tr><td>External Memory Expansion</td><td>
• Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines
• Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines
• External memory expansion port
• Chip select logic for glueless interface to static random access memory (SRAMs)
</td></tr>
<tr><td>Power Dissipation</td><td>
• Very low-power CMOS design
• Wait and Stop low-power standby modes
• Fully static design specified to operate down to 0 Hz (dc)
• Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)
</td></tr>
<tr><td>Packaging</td><td>
• Molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions.
</td></tr>
</table>

Target Applications

DSP56321 applications require high performance, low power, small packaging, and a large amount of internal memory. The EFCOP can accelerate general filtering applications. Examples include:

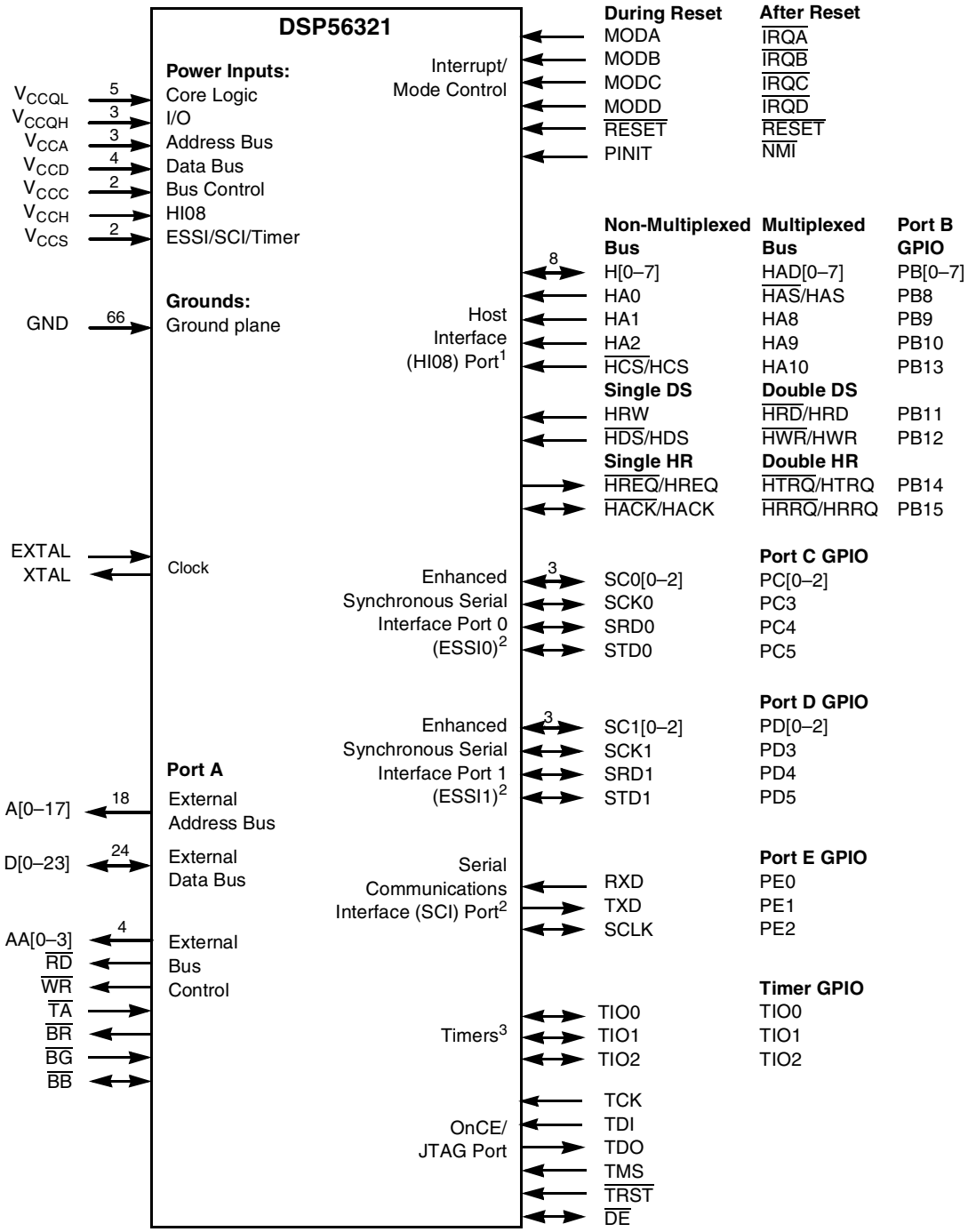
- Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- Security encryption systems
- Home entertainment systems
- DSP resource boards
- High-speed modem banks
- IP telephony

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56321 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56321 Documentation

Name	Description	Order Number
DSP56321 Reference Manual	Detailed functional description of the DSP56321 memory configuration, operation, and register programming	DSP56321RM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56321 product website



Notes:
1. The HI08 port supports a non-multiplexed or a multiplexed bus, single or double data strobe (DS), and single or double host request (HR) configurations. Since each of these modes is configured independently, any combination of these modes is possible. These HI08 signals can also be configured alternatively as GPIO signals (PB[0–15]). Signals with dual designations (for example, HAS/HAS) have configurable polarity.
2. The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0–5]), Port D GPIO signals (PD[0–5]), and Port E GPIO signals (PE[0–2]), respectively.
3. TIO[0–2] can be configured as GPIO signals.

Figure 1-1. Signals Identified by Functional Group

Table 1-12. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-13. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

Table 1-13. Serial Communication Interface (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCLK	Input/Output	Ignored Input	**Serial Clock**—Provides the input or output clock used by the transmitter and/or the receiver.
PE2	Input or Output		**Port E 2**—The default configuration following reset is GPIO input PE2. When configured as PE2, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal SCLK through the Port E Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.10 Timers

The DSP56321 has three identical and independent timers. Each timer can use internal or external clocking and can either interrupt the DSP56321 after a specified number of events (clocks) or signal an external device after counting a specific number of internal events.

Table 1-14. Triple Timer Signals

Signal Name	Type	State During Reset[1,2]	Signal Description
TIO0	Input or Output	Ignored Input	**Timer 0 Schmitt-Trigger Input/Output**— When Timer 0 functions as an external event counter or in measurement mode, TIO0 is used as input. When Timer 0 functions in watchdog, timer, or pulse modulation mode, TIO0 is used as output. The default mode after reset is GPIO input. TIO0 can be changed to output or configured as a timer I/O through the Timer 0 Control/Status Register (TCSR0).
TIO1	Input or Output	Ignored Input	**Timer 1 Schmitt-Trigger Input/Output**— When Timer 1 functions as an external event counter or in measurement mode, TIO1 is used as input. When Timer 1 functions in watchdog, timer, or pulse modulation mode, TIO1 is used as output. The default mode after reset is GPIO input. TIO1 can be changed to output or configured as a timer I/O through the Timer 1 Control/Status Register (TCSR1).
TIO2	Input or Output	Ignored Input	**Timer 2 Schmitt-Trigger Input/Output**— When Timer 2 functions as an external event counter or in measurement mode, TIO2 is used as input. When Timer 2 functions in watchdog, timer, or pulse modulation mode, TIO2 is used as output. The default mode after reset is GPIO input. TIO2 can be changed to output or configured as a timer I/O through the Timer 2 Control/Status Register (TCSR2).

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current:					
• In Normal mode[3]	I_{CCI}				
— at 200 MHz		—	190	—	mA
— at 220 MHz		—	200	—	mA
— at 240 MHz		—	210	—	mA
— at 275 MHz		—	235	—	mA
• In Wait mode[4]	I_{CCW}	—	25	—	mA
• In Stop mode[5]	I_{CCS}	—	15	—	mA
Input capacitance[6]	C_{IN}	—	—	10	pF

Notes:
1. Power-up sequence: During power-up, and throughout the DSP56321 operation, V_{CCQH} voltage must always be higher or equal to V_{CCQL} voltage.
2. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
3. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications.
4. To obtain these results, all inputs must be terminated (that is, not allowed to float).
5. To obtain these results, all inputs not disconnected at Stop mode must be terminated (that is, not allowed to float), and the DPLL and on-chip crystal oscillator must be disabled.
6. Periodically sampled and not 100 percent tested.
7. V_{CCQH} = 3.3 V ±0.3 V, V_{CQLC} = 1.6 V ±0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
8. This characteristic does not apply to XTAL.
9. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CCQH} and the maximum V_{ILX} should be no higher than 0.1 × V_{CCQH}.

2.4 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Notes 7 and 9 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal's transition. DSP56321 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 16 MHz and rated speed with the DPLL enabled.

2.4.1 Internal Clocks

Table 2-4. Internal Clocks

Characteristics	Symbol	Expression		
		Min	Typ	Max
Internal operating frequency	f			
• With DPLL disabled		—	Ef/2	—
• With DPLL enabled		—	(Ef × MF)/(PDF × DF)	—
Internal clock cycle time	T_C			
• With DPLL disabled		—	2 × ET_C	—
• With DPLL enabled		—	ET_C × PDF × DF/MF	—
Internal clock high period	T_H			
• With DPLL disabled		—	ET_C	—
• With DPLL enabled		0.49 × T_C	—	0.51 × T_C

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7]	(WS + 3.25) × T_C – 10.94	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7] • SRAM WS = 3 • SRAM WS ≥ 4	 (WS + 3) × T_C – 10.94 (WS + 2.5) × T_C – 10.94	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 ns ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		8.0	—	8.0	—	8.0	—	8.0	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop (PCTL Bit 1 = 1; Implies No Stop Delay)	 DPLT + (128K × T_C) DPLT + (23.75 ± 0.5) × T_C (10.0 ± 1.75) × T_C	 662.2 µs 6.9 41.25	 209.9 ms 188.8 58.8	 662.2 µs 6.9 37.5	 209.9 ms 188.8 53.3	 662.2 µs 6.9 34.4	 209.9 ms 188.8 49.0	 662.2 µs 6.9 30.0	 209.9 ms 188.8 43.0	 — µs ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop ((PCTL bit 1 = 0; implies no Stop delay)	 DPLT + (128 K × T_C) DPLT + (20.5 ± 0.5) × T_C 5.5 × T_C	 805.4 150.1 27.5	 — — —	 805.4 150.1 25	 — — —	 805.4 150.1 22.9	 — — —	 805.4 150.1 20.0	 — — —	 µs µs ns
27	Interrupt Request Rate • HI08, ESSI, SCI, Timer • DMA • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) • $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	 12T_C 8T_C 8T_C 12T_C	 — — — —	 60.0 40.0 40.0 60.0	 — — — —	 54.6 36.4 36.4 54.6	 — — — —	 50.0 33.4 33.4 50.0	 — — — —	 43.7 29.2 29.2 43.7	 ns ns ns ns
28	DMA Request Rate • Data read from HI08, ESSI, SCI • Data write to HI08, ESSI, SCI • Timer • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	 6T_C 7T_C 2T_C 3T_C	 — — — —	 30.0 35.0 10.0 15.0	 — — — —	 27.3 31.9 9.1 13.7	 — — — —	 25.0 29.2 8.3 12.5	 — — — —	 21.84 25.48 7.28 10.92	 ns ns ns ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	4.25 × T_C + 2.0	23.25	—	21.34	—	19.72	—	17.45	—	ns

2.4.5 External Memory Expansion Port (Port A)

2.4.5.1 SRAM Timing

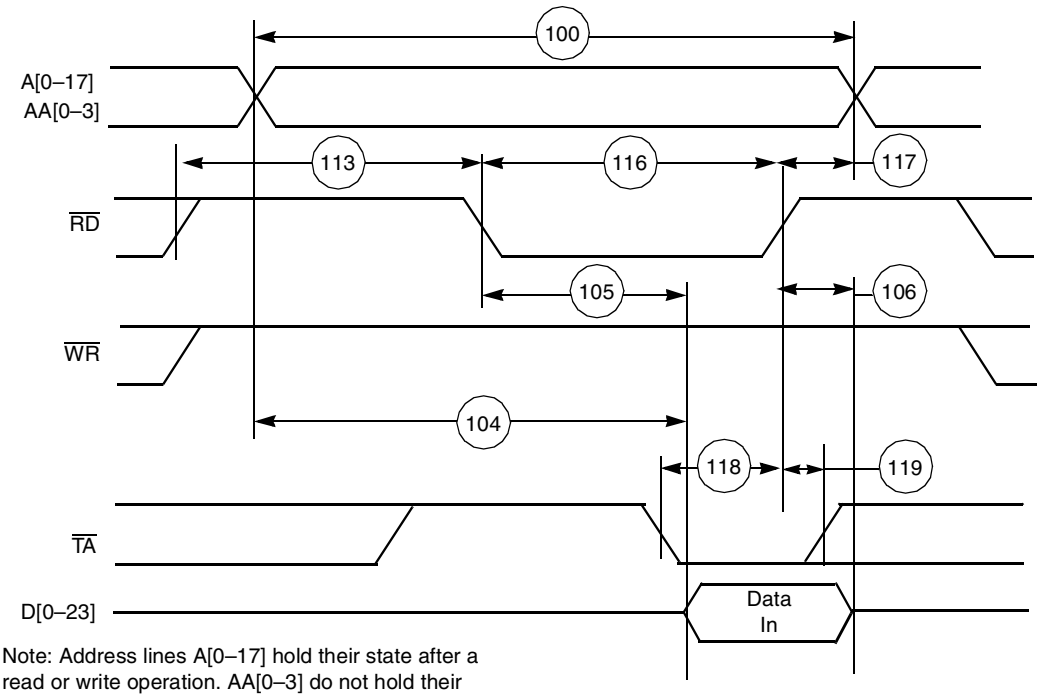
Table 2-8. SRAM Timing

No.	Characteristics	Symbol	Expression[1]	200 MHz		220 MHz		240 MHz		275 MHz		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
100	Address valid and AA assertion pulse width[2]	t_{RC}, t_{WC}	(WS + 2) × T_C –4.0 [3 ≤WS ≤7]	21.0		18.8		16.9		15.0		ns
			(WS + 3) × T_C –4.0 [WS ≥ 8]	51.0	—	46.0	—	41.9	—	36.0	—	ns
101	Address and AA valid to $\overline{WR}$ assertion	t_{AS}	0.75 × T_C – 3.0 [WS = 3]	0.75	—	0.41	—	0.13	—	–0.27	—	ns
			1.25 × T_C – 3.0 [WS ≥ 4]	3.25	—	2.69	—	2.21	—	1.54	—	ns
102	$\overline{WR}$ assertion pulse width	t_{WP}	WS × T_C –4.0 [WS = 3]	11.0	—	9.65	—	8.51	—	6.9	—	ns
			(WS –0.5) × T_C –4.0 [WS ≥ 4]	13.5	—	11.93	—	10.6	—	8.72	—	ns
103	$\overline{WR}$ deassertion to address not valid	t_{WR}	1.25 × T_C –4.0 [3 ≤WS ≤7]	2.25	—	1.69	—	1.21	—	0.54	—	ns
			2.25 × T_C –4.0 [WS ≥ 8]	7.25	—	6.24	—	5.38	—	4.18	—	ns
104	Address and AA valid to input data valid	t_{AA}, t_{AC}	(WS + 0.75) × T_C –5.8 [WS ≥ 3]	—	12.9	—	11.2	—	9.8	—	7.84	ns
105	$\overline{RD}$ assertion to input data valid	t_{OE}	(WS + 0.25) × T_C –6.5 [WS ≥ 3]	—	9.75	—	8.29	—	7.05	—	5.31	ns
106	$\overline{RD}$ deassertion to data not valid (data hold time)	t_{OHZ}		0.0	—	0.0	—	0.0	—	0.0	—	ns
107	Address valid to $\overline{WR}$ deassertion[2]	t_{AW}	(WS + 0.75) × T_C –4.0 [WS ≥ 3]	14.75	—	13.06	—	11.64	—	9.63	—	ns
108	Data valid to $\overline{WR}$ deassertion (data setup time)	t_{DS} (t_{DW})	(WS –0.25) × T_C –5.4 [WS ≥ 3]	8.35	—	7.11	—	6.07	—	4.6	—	ns
109	Data hold time from $\overline{WR}$ deassertion	t_{DH}	1.25 × T_C –4.0 [3 ≤WS ≤7]	2.25	—	1.69	—	1.21	—	0.54	—	ns
			2.25 × T_C –4.0 [WS ≥ 8]	7.25	—	6.23	—	5.38	—	4.18	—	ns
110	$\overline{WR}$ assertion to data active	—	0.25 × T_C –4.0 [WS = 3]	–2.75	—	–2.86	—	–2.96	—	–3.1	—	ns
			–0.25 × T_C –4.0 [WS ≥ 4]	–5.25	—	–5.14	—	–5.04	—	–4.91	—	ns
111	$\overline{WR}$ deassertion to data high impedance	—	1.25 × T_C	6.25	—	5.69	—	5.21	—	4.55	—	ns
112	Previous $\overline{RD}$ deassertion to data active (write)	—	2.25 × T_C –4.0	7.25	—	6.23	—	5.38	—	4.18	—	ns
113	$\overline{RD}$ deassertion time	—	1.75 × T_C –3.0 [3 ≤WS ≤7]	5.75	—	4.96	—	4.3	—	3.36	—	ns
			2.75 × T_C –3.0 [WS ≥ 8]	10.75	—	9.51	—	8.47	—	7.0	—	ns
114	$\overline{WR}$ deassertion time[4]	—	2.0 × T_C –3.0 [3 ≤WS ≤7]	7.0	—	6.1	—	5.3	—	4.27	—	ns
			3.0 × T_C –3.0 [WS ≥ 8]	12.0	—	10.6	—	9.5	—	7.91	—	ns

Table 2-8. SRAM Timing (Continued)

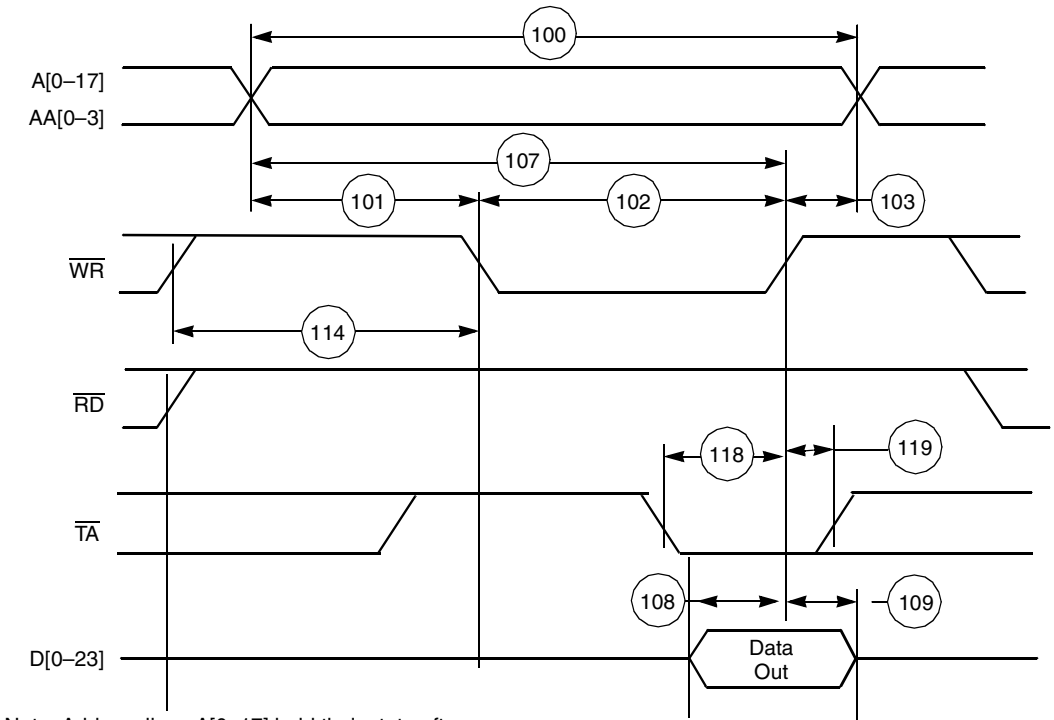
No.	Characteristics	Symbol	Expression[1]	200 MHz		220 MHz		240 MHz		275 MHz		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
115	Address valid to $\overline{RD}$ assertion	—	$0.5 \times T_C - 2.0$	0.5	—	0.3	—	0.1	—	–0.18	—	ns
116	$\overline{RD}$ assertion pulse width	—	$(WS + 0.25) \times T_C - 3.0$ [WS ≥ 3]	13.25	—	11.59	—	10.55	—	8.81	—	ns
117	$\overline{RD}$ deassertion to address not valid	—	$1.25 \times T_C - 4.0$ [3 ≤WS ≤7] $2.25 \times T_C - 4.0$ [WS ≥ 8]	2.25 7.25	— —	1.69 6.24	— —	1.21 5.38	— —	0.54 4.18	— —	ns ns
118	$\overline{TA}$ setup before $\overline{RD}$ or $\overline{WR}$ deassertion[5]	—	$0.25 \times T_C + 2.0$	3.25	—	3.14	—	3.04	—	2.91	—	ns
119	$\overline{TA}$ hold after $\overline{RD}$ or $\overline{WR}$ deassertion	—		0	—	0	—	0	—	0	—	ns

Notes:
1. WS is the number of wait states specified in the BCR. The value is given for the minimum for a given category. (For example, for a category of [3 ≤WS ≤7] timing is specified for 3 wait states.) Three wait states is the minimum value otherwise.
2. Timings 100 and 107 are guaranteed by design, not tested.
3. All timings are measured from $0.5 \times V_{CCQH}$ to $0.5 \times V_{CCQH}$.
4. The WS number applies to the access in which the deassertion of $\overline{WR}$ occurs and assumes the next access uses a minimal number of wait states.
5. Timing 118 is relative to the deassertion edge of $\overline{RD}$ or $\overline{WR}$ even if $\overline{TA}$ remains asserted.



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-10. SRAM Read Access



Note: Address lines A[0–17] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-11. SRAM Write Access

2.4.5.2 Asynchronous Bus Arbitration Timings

Table 2-9. Asynchronous Bus Timings

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 Mhz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
250	$\overline{BB}$ assertion window from $\overline{BG}$ input deassertion.	2.5 × Tc + 5	—	17.5	—	16.4	—	15.4	—	14.1	ns
251	Delay from $\overline{BB}$ assertion to $\overline{BG}$ assertion	2 × Tc + 5	15	—	14.1	—	13.3	—	12.27	—	ns

Notes:
1. Bit 13 in the Operating Mode Register must be set to enable Asynchronous Arbitration mode.
2. To guarantee timings 250 and 251, it is recommended that you assert non-overlapping $\overline{BG}$ inputs to different DSP56300 devices (on the same bus), as shown in **Figure 2-12**, where $\overline{BG1}$ is the $\overline{BG}$ signal for one DSP56300 device while $\overline{BG2}$ is the $\overline{BG}$ signal for a second DSP56300 device.

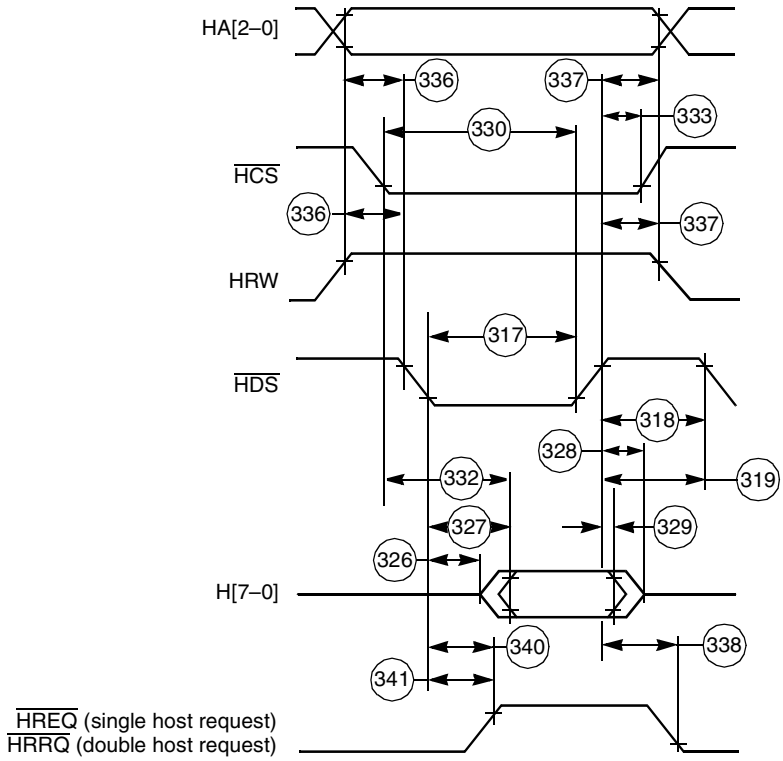


Figure 2-14. Read Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

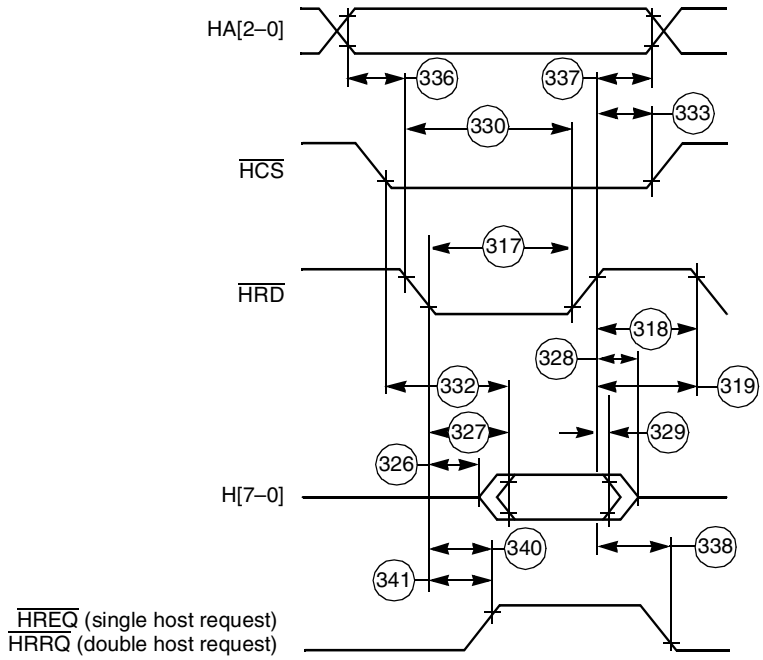


Figure 2-15. Read Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

2.4.7 SCI Timing

Table 2-11. SCI Timings

No.	Characteristics[1]	Symbol	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
400	Synchronous clock cycle	t_{SCC}[2]	$16 \times T_C$	80.0	—	72.8	—	66.7	—	58.0	—	ns
401	Clock low period		$t_{SCC}/2 - 10.0$	30.0	—	26.4	—	23.4	—	19.0	—	ns
402	Clock high period		$t_{SCC}/2 - 10.0$	30.0	—	26.4	—	23.4	—	19.0	—	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	5.5	—	3.5	—	1.76	—	–0.68	—	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 1.5 \times T_C$	13	—	11.5	—	10	—	9.04	—	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	47.5	—	45.5	—	43.8	—	41.32	—	ns
406	Input data not valid before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 5.5$	—	17.0	—	15.0	—	13.8	—	10.81	ns
407	Clock falling edge to output data valid (external clock)			—	32.0	—	32.0	—	32.0	—	32.0	ns
408	Output data hold after clock rising edge (external clock)		$T_C + 8.0$	13.0	—	12.6	—	12.2	—	11.64	—	ns
409	Input data setup time before clock rising edge (external clock)			0.0	—	0.0	—	0.0	—	0.0	—	ns
410	Input data hold time after clock rising edge (external clock)			9.0	—	9.0	—	9.0	—	9.0	—	ns
411	Asynchronous clock cycle	t_{ACC}[3]	$64 \times T_C$	320.0	—	291.2	—	266.9	—	232.0	—	ns
412	Clock low period		$t_{ACC}/2 - 10.0$	150.0	—	135.6	—	123.5	—	106.0	—	ns
413	Clock high period		$t_{ACC}/2 - 10.0$	150.0	—	135.6	—	123.5	—	106.0	—	ns
414	Output data setup to clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	130.0	—	115.6	—	103.5	—	86.0	—	ns
415	Output data hold after clock rising edge (internal clock)		$t_{ACC}/2 - 30.0$	130.0	—	115.6	—	103.5	—	86.0	—	ns

Notes:
1. $V_{CCQH} = 3.3\ V \pm 0.3\ V$, $V_{CCQL} = 1.6\ V \pm 0.1\ V$; $T_J = -40°C$ to $+100\ °C$, $C_L = 50\ pF$.
2. t_{SCC} = synchronous clock cycle time (for internal clock, t_{SCC} is determined by the SCI clock control register and T_C).
3. t_{ACC} = asynchronous clock cycle time; value given for 1X Clock mode (for internal clock, t_{ACC} is determined by the SCI clock control register and T_C).
4. In the timing diagrams that follow, the SCLK is drawn using the clock falling edge as a the first reference. Clock polarity is programmable in the SCI Control Register (SCR). Refer to the *DSP56321 Reference Manual* for details.

Packaging 3

This section includes diagrams of the DSP56321 package pin-outs and tables showing how the signals described in **Chapter 1** are allocated for the package. The DSP56321 is available in a 196-pin molded array plastic-ball grid array (MAP-BGA) package.

Table 3-1. Signal List by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	Not Connected (NC)	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors ($\overline{\text{TRST}}$, TMS, $\overline{\text{DE}}$).
- The following pins must be asserted during the power-up sequence: $\overline{\text{RESET}}$ and $\overline{\text{TRST}}$. A stable EXTAL signal should be supplied before deassertion of $\overline{\text{RESET}}$. If the V_{CC} reaches the required level before EXTAL is stable or other "required $\overline{\text{RESET}}$ duration" conditions are met (see **Table 2-7**), the device circuitry can be in an uninitialized state that may result in significant power consumption and heat-up. Designs should minimize this condition to the shortest possible duration.
- Ensure that during power-up, and throughout the DSP56321 operation, V_{CCQH} is always higher or equal to the V_{CCQL} voltage level.
- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- The Port A data bus (D[0–23]), HI08, ESSI0, ESSI1, SCI, and timers all use internal keepers to maintain the last output value even when the internal signal is tri-stated. Typically, no pull-up or pull-down resistors should be used with these signal lines. However, if the DSP is connected to a device that requires pull-up resistors (such as an MPC8260), the recommended resistor value is 10 KΩ or less. If more than one DSP must be connected in parallel to the other device, the pull-up resistor value requirement changes as follows:
  - 2 DSPs = 5 KΩ (mask sets 0K91M and 1K91M)/7 KΩ (mask set 0K93M) or less
  - 3 DSPs = 3 KΩ (mask sets 0K91M and 1K91M)/4 KΩ (mask set 0K93M) or less
  - 4 DSPs = 2 KΩ (mask sets 0K91M and 1K91M)/3 KΩ (mask set 0K93M) or less
  - 5 DSPs = 1.5 KΩ (mask sets 0K91M and 1K91M)/2 KΩ (mask set 0K93M) or less
  - 6 DSPs = 1 KΩ (mask sets 0K91M and 1K91M)/1.5 KΩ (mask set 0K93M) or less

Note: Refer to *EB610/D DSP56321/DSP56321T Power-Up Sequencing Guidelines* for detailed information about minimizing power consumption during startup.

4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

Equation 3: $I = C \times V \times f$

Where:

C	=	node/pin capacitance
V	=	voltage swing
f	=	frequency of node/pin toggle

Example 4-1. Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

Equation 4: $I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^{6} = 5.48\ mA$

The maximum internal current (I_{CCI}max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current (I_{CCItyp}) value reflects the average switching of the internal buses on typical operating conditions.

Perform the following steps for applications that require very low current consumption:

1. Set the EBD bit when you are not accessing external memory.
2. Minimize external memory accesses, and use internal memory accesses.
3. Minimize the number of pins that are switching.
4. Minimize the capacitive load on the pins.
5. Connect the unused inputs to pull-up or pull-down resistors.
6. Disable unused peripherals.
7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.

Equation 5: $/\ \text{MIPS} = I/\ \text{MHz} = (I_{typF2} - I_{typF1})/\ (\text{F2} - \text{F1})$

Where:

I_{typF2}	=	current at F2
I_{typF1}	=	current at F1
F2	=	high frequency (any specified operating frequency)
F1	=	low frequency (any specified operating frequency lower than F2)

Note: F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

4.4 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.

```
ioequ   ident   1,0

;---------------------------------------------------------------------------
;
;       EQUATES for I/O Port Programming
;
;---------------------------------------------------------------------------

;       Register Addresses

M_HDR EQU $FFFFC9                ; Host port GPIO data Register
M_HDDR EQU $FFFFC8               ; Host port GPIO direction Register
M_PCRC EQU $FFFFBF               ; Port C Control Register
M_PRRC EQU $FFFFBE               ; Port C Direction Register
M_PDRC EQU $FFFFBD               ; Port C GPIO Data Register
M_PCRD EQU $FFFFAF               ; Port D Control register
M_PRRD EQU $FFFFAE               ; Port D Direction Data Register
M_PDRD EQU $FFFFAD               ; Port D GPIO Data Register
M_PCRE EQU $FFFF9F               ; Port E Control register
M_PRRE EQU $FFFF9E               ; Port E Direction Register
M_PDRE EQU $FFFF9D               ; Port E Data Register
M_OGDB EQU $FFFFFC               ; OnCE GDB Register


;---------------------------------------------------------------------------
;
;       EQUATES for Host Interface
;
;---------------------------------------------------------------------------

;       Register Addresses

M_HCR EQU $FFFFC2                ; Host Control Register
M_HSR EQU $FFFFC3                ; Host Status Register
M_HPCR EQU $FFFFC4               ; Host Polarity Control Register
M_HBAR EQU $FFFFC5               ; Host Base Address Register
M_HRX EQU $FFFFC6                ; Host Receive Register
M_HTX EQU $FFFFC7                ; Host Transmit Register

;       HCR bits definition
M_HRIE EQU $0                    ; Host Receive interrupts Enable
M_HTIE EQU $1                    ; Host Transmit Interrupt Enable
M_HCIE EQU $2                    ; Host Command Interrupt Enable
M_HF2 EQU $3                     ; Host Flag 2
M_HF3 EQU $4                     ; Host Flag 3

;       HSR bits definition
M_HRDF EQU $0                    ; Host Receive Data Full
M_HTDE EQU $1                    ; Host Receive Data Empty
M_HCP EQU $2                     ; Host Command Pending
M_HF0 EQU $3                     ; Host Flag 0
M_HF1 EQU $4                     ; Host Flag 1


;       HPCR bits definition
M_HGEN EQU $0                    ; Host Port GPIO Enable
M_HA8EN EQU $1                   ; Host Address 8 Enable
M_HA9EN EQU $2                   ; Host Address 9 Enable
M_HCSEN EQU $3                   ; Host Chip Select Enable
M_HREN EQU $4                    ; Host Request Enable
M_HAEN EQU $5                    ; Host Acknowledge Enable
M_HEN EQU $6                     ; Host Enable
```

```
M_CD EQU $FFF                       ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                        ; Clock Out Divider
M_SCP EQU 13                        ; Clock Prescaler
M_RCM EQU 14                        ; Receive Clock Mode Source Bit
M_TCM EQU 15                        ; Transmit Clock Source Bit

;-------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;-------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                  ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                  ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                  ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                  ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                   ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                  ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                  ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                 ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                 ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                 ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                 ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                  ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                  ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                  ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                  ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                   ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                  ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                  ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                 ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                 ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                 ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                 ; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF                        ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                        ; Prescaler Range
M_DC EQU $1F000                     ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18                        ; Alignment Control (ALC)
M_WL EQU $380000                    ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22                       ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3                         ; Serial Output Flag Mask
M_OF0 EQU 0                         ; Serial Output Flag 0
M_OF1 EQU 1                         ; Serial Output Flag 1
M_SCD EQU $1C                       ; Serial Control Direction Mask
M_SCD0 EQU 2                        ; Serial Control 0 Direction
M_SCD1 EQU 3                        ; Serial Control 1 Direction
M_SCD2 EQU 4                        ; Serial Control 2 Direction
M_SCKD EQU 5                        ; Clock Source Direction
M_SHFD EQU 6                        ; Shift Direction
M_FSL EQU $180                      ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7                        ; Frame Sync Length 0
```

```
M_TLR0 EQU  $FFFF8E              ; TIMER0 Load Reg
M_TCPR0 EQU $FFFF8D              ; TIMER0 Compare Register
M_TCR0 EQU  $FFFF8C              ; TIMER0 Count Register

;       Register Addresses Of TIMER1

M_TCSR1 EQU $FFFF8B              ; TIMER1 Control/Status Register
M_TLR1 EQU  $FFFF8A              ; TIMER1 Load Reg
M_TCPR1 EQU $FFFF89              ; TIMER1 Compare Register
M_TCR1 EQU  $FFFF88              ; TIMER1 Count Register


;       Register Addresses Of TIMER2

M_TCSR2 EQU $FFFF87              ; TIMER2 Control/Status Register
M_TLR2 EQU  $FFFF86              ; TIMER2 Load Reg
M_TCPR2 EQU $FFFF85              ; TIMER2 Compare Register
M_TCR2 EQU  $FFFF84              ; TIMER2 Count Register
M_TPLR EQU  $FFFF83              ; TIMER Prescaler Load Register
M_TPCR EQU  $FFFF82              ; TIMER Prescalar Count Register


;       Timer Control/Status Register Bit Flags

M_TE EQU 0                       ; Timer Enable
M_TOIE EQU 1                     ; Timer Overflow Interrupt Enable
M_TCIE EQU 2                     ; Timer Compare Interrupt Enable
M_TC EQU $F0                     ; Timer Control Mask (TC0-TC3)
M_INV EQU 8                      ; Inverter Bit
M_TRM EQU 9                      ; Timer Restart Mode
M_DIR EQU 11                     ; Direction Bit
M_DI EQU 12                      ; Data Input
M_DO EQU 13                      ; Data Output
M_PCE EQU  15                    ; Prescaled Clock Enable
M_TOF EQU 20                     ; Timer Overflow Flag
M_TCF EQU 21                     ; Timer Compare Flag

;       Timer Prescaler Register Bit Flags

M_PS EQU  $600000                ; Prescaler Source Mask
M_PS0 EQU  21
M_PS1 EQU  22

;      Timer Control Bits
M_TC0 EQU 4                      ; Timer Control 0
M_TC1 EQU 5                      ; Timer Control 1
M_TC2 EQU 6                      ; Timer Control 2
M_TC3 EQU 7                      ; Timer Control 3


;---------------------------------------------------------------------------
;
;       EQUATES for Direct Memory Access (DMA)
;
;---------------------------------------------------------------------------

;       Register Addresses Of DMA
M_DSTR EQU FFFFF4                ; DMA Status Register
M_DOR0 EQU $FFFFF3               ; DMA Offset Register 0
M_DOR1 EQU $FFFFF2               ; DMA Offset Register 1
M_DOR2 EQU $FFFFF1               ; DMA Offset Register 2
M_DOR3 EQU $FFFFF0               ; DMA Offset Register 3
```