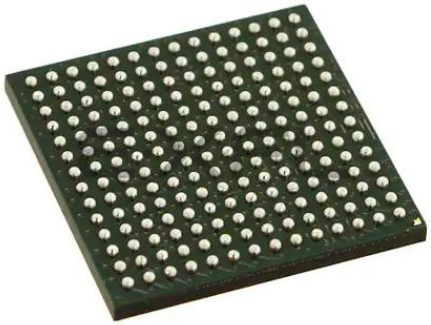

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed Point
Interface	Host Interface, SSI, SCI
Clock Rate	240MHz
Non-Volatile Memory	ROM (576B)
On-Chip RAM	576kB
Voltage - I/O	3.30V
Voltage - Core	1.60V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	196-BGA
Supplier Device Package	196-MAPBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spakdsp321vl240

Features

Table 1 lists the features of the DSP56321 device.

Table 1. DSP56321 Features

Feature	Description
High-Performance DSP56300 Core	• 275 million multiply-accumulates per second (MMACS) (550 MMACS using the EFCOP in filtering applications) with a 275 MHz clock at 1.6 V core and 3.3 V I/O • Object code compatible with the DSP56000 core with highly parallel instruction set • Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control • Program control unit (PCU) with position independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts • Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals • Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination • Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)

Enhanced Filter Coprocessor (EFCOP)	• Internal 24 × 24-bit filtering and echo-cancellation coprocessor that runs in parallel to the DSP core
	• Operation at the same frequency as the core (up to 275 MHz)
	• Support for a variety of filter modes, some of which are optimized for cellular base station applications:
	  • Real finite impulse response (FIR) with real taps
	  • Complex FIR with complex taps
	  • Complex FIR generating pure real or pure imaginary outputs alternately
	  • A 4-bit decimation factor in FIR filters, thus providing a decimation ratio up to 16
	  • Direct form 1 (DFI) Infinite Impulse Response (IIR) filter
	  • Direct form 2 (DFII) IIR filter
	  • Four scaling factors (1, 4, 8, 16) for IIR output
	  • Adaptive FIR filter with true least mean square (LMS) coefficient updates
	  • Adaptive FIR filter with delayed LMS coefficient updates

Internal Peripherals	• Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs • Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater) • Serial communications interface (SCI) with baud rate generator • Triple timer module • Up to 34 programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

Product Documentation

The documents listed in **Table 2** are required for a complete description of the DSP56321 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Table 2. DSP56321 Documentation

Name	Description	Order Number
DSP56321 Reference Manual	Detailed functional description of the DSP56321 memory configuration, operation, and register programming	DSP56321RM
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56321 product website

Table 1-7. External Bus Control Signals (Continued)

Signal Name	Type	State During Reset, Stop, or Wait	Signal Description
$\overline{TA}$	Input	Ignored Input	**Transfer Acknowledge**—If the DSP56321 is the bus master and there is no external bus activity, or the DSP56321 is not the bus master, the $\overline{TA}$ input is ignored. The $\overline{TA}$ input is a data transfer acknowledge (DTACK) function that can extend an external bus cycle indefinitely. Any number of wait states (1, 2. . .infinity) can be added to the wait states inserted by the bus control register (BCR) by keeping $\overline{TA}$ deasserted. In typical operation, $\overline{TA}$ is deasserted at the start of a bus cycle, is asserted to enable completion of the bus cycle, and is deasserted before the next bus cycle. The current bus cycle completes one clock period after $\overline{TA}$ is asserted synchronous to CLKOUT. The number of wait states is determined by the $\overline{TA}$ input or by the BCR, whichever is longer. The BCR can be used to set the minimum number of wait states in external bus cycles. To use the $\overline{TA}$ functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by $\overline{TA}$ deassertion; otherwise, improper operation may result.
$\overline{BR}$	Output	Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output (deasserted) • BRH = 1: Maintains last state (that is, if asserted, remains asserted)	**Bus Request**—Asserted when the DSP requests bus mastership. $\overline{BR}$ is deasserted when the DSP no longer needs the bus. $\overline{BR}$ may be asserted or deasserted independently of whether the DSP56321 is a bus master or a bus slave. Bus “parking” allows $\overline{BR}$ to be deasserted even though the DSP56321 is the bus master. (See the description of bus “parking” in the $\overline{BB}$ signal description.) The bus request hold (BRH) bit in the BCR allows $\overline{BR}$ to be asserted under software control even though the DSP does not need the bus. $\overline{BR}$ is typically sent to an external bus arbitrator that controls the priority, parking, and tenure of each master on the same external bus. $\overline{BR}$ is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, $\overline{BR}$ is deasserted and the arbitration is reset to the bus slave state.
$\overline{BG}$	Input	Ignored Input	**Bus Grant**—Asserted by an external bus arbitration circuit when the DSP56321 becomes the next bus master. When $\overline{BG}$ is asserted, the DSP56321 must wait until $\overline{BB}$ is deasserted before taking bus mastership. When $\overline{BG}$ is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution. To ensure proper operation, the user must set the asynchronous bus arbitration enable (ABE) bit (Bit 13) in the Operating Mode Register. When this bit is set, $\overline{BG}$ and $\overline{BB}$ are synchronized internally. This adds a required delay between the deassertion of an initial $\overline{BG}$ input and the assertion of a subsequent $\overline{BG}$ input.
$\overline{BB}$	Input/ Output	Ignored Input	**Bus Busy**—Indicates that the bus is active. Only after $\overline{BB}$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master may keep $\overline{BB}$ asserted after ceasing bus activity regardless of whether $\overline{BR}$ is asserted or deasserted. Called “bus parking,” this allows the current bus master to reuse the bus without rearbitration until another device requires the bus. $\overline{BB}$ is deasserted by an “active pull-up” method (that is, $\overline{BB}$ is driven high and then released and held high by an external pull-up resistor). **Notes:** **1.** See $\overline{BG}$ for additional information. **2.** $\overline{BB}$ requires an external pull-up resistor.

Table 1-12. Enhanced Serial Synchronous Interface 1 (Continued)

Signal Name	Type	State During Reset[1,2]	Signal Description
SCK1	Input/Output	Ignored Input	**Serial Clock**—Provides the serial bit rate clock for the ESSI. The SCK1 is a clock input or output used by both the transmitter and receiver in synchronous modes or by the transmitter in asynchronous modes. Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PD3	Input or Output		**Port D 3**—The default configuration following reset is GPIO input PD3. When configured as PD3, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SCK1 through the Port D Control Register.
SRD1	Input	Ignored Input	**Serial Receive Data**—Receives serial data and transfers the data to the ESSI Receive Shift Register. SRD1 is an input when data is being received.
PD4	Input or Output		**Port D 4**—The default configuration following reset is GPIO input PD4. When configured as PD4, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal SRD1 through the Port D Control Register.
STD1	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the Serial Transmit Shift Register. STD1 is an output when data is being transmitted.
PD5	Input or Output		**Port D 5**—The default configuration following reset is GPIO input PD5. When configured as PD5, signal direction is controlled through the Port D Direction Register. The signal can be configured as an ESSI signal STD1 through the Port D Control Register.

Notes: 1. In the Stop state, the signal maintains the last state as follows:
- If the last state is input, the signal is an ignored input.
- If the last state is output, these lines have weak keepers that maintain the last output state even if the drivers are tri-stated.

2. The Wait processing state does not affect the signal state.

1.9 Serial Communication Interface (SCI)

The SCI provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-13. Serial Communication Interface

Signal Name	Type	State During Reset[1,2]	Signal Description
RXD	Input	Ignored Input	**Serial Receive Data**—Receives byte-oriented serial data and transfers it to the SCI Receive Shift Register.
PE0	Input or Output		**Port E 0**—The default configuration following reset is GPIO input PE0. When configured as PE0, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal RXD through the Port E Control Register.
TXD	Output	Ignored Input	**Serial Transmit Data**—Transmits data from the SCI Transmit Data Register.
PE1	Input or Output		**Port E 1**—The default configuration following reset is GPIO input PE1. When configured as PE1, signal direction is controlled through the Port E Direction Register. The signal can be configured as an SCI signal TXD through the Port E Control Register.

1.11 JTAG and OnCE Interface

The DSP56300 family and in particular the DSP56321 support circuit-board test strategies based on the **IEEE® Std.** 1149.1™ test access port and boundary scan architecture, the industry standard developed under the sponsorship of the Test Technology Committee of IEEE and the JTAG. The OnCE module provides a means to interface nonintrusively with the DSP56300 core and its peripherals so that you can examine registers, memory, or on-chip peripherals. Functions of the OnCE module are provided through the JTAG TAP signals. For programming models, see the chapter on debugging support in the *DSP56300 Family Manual*.

Table 1-15. JTAG/OnCE Interface

Signal Name	Type	State During Reset	Signal Description
TCK	Input	Input	**Test Clock**—A test clock input signal to synchronize the JTAG test logic.
TDI	Input	Input	**Test Data Input**—A test data serial input signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.
TDO	Output	Tri-stated	**Test Data Output**—A test data serial output signal for test instructions and data. TDO is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCK.
TMS	Input	Input	**Test Mode Select**—Sequences the test controller's state machine. TMS is sampled on the rising edge of TCK and has an internal pull-up resistor.
$\overline{\text{TRST}}$	Input	Input	**Test Reset**—Initializes the test controller asynchronously. $\overline{\text{TRST}}$ has an internal pull-up resistor. $\overline{\text{TRST}}$ must be asserted during and after power-up (see EB610/D for details).
$\overline{\text{DE}}$	Input/ Output	Input	**Debug Event**—As an input, initiates Debug mode from an external command controller, and, as an open-drain output, acknowledges that the chip has entered Debug mode. As an input, $\overline{\text{DE}}$ causes the DSP56300 core to finish executing the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands to be entered from the debug serial input line. This signal is asserted as an output for three clock cycles when the chip enters Debug mode as a result of a debug request or as a result of meeting a breakpoint condition. The $\overline{\text{DE}}$ has an internal pull-up resistor. This signal is not a standard part of the JTAG TAP controller. The signal connects directly to the OnCE module to initiate debug mode directly or to provide a direct external indication that the chip has entered Debug mode. All other interface with the OnCE module must occur through the JTAG port.

Table 2-3. DC Electrical Characteristics[7]

Characteristics	Symbol	Min	Typ	Max	Unit
Internal supply current:					
• In Normal mode[3]	I_{CCI}				
— at 200 MHz		—	190	—	mA
— at 220 MHz		—	200	—	mA
— at 240 MHz		—	210	—	mA
— at 275 MHz		—	235	—	mA
• In Wait mode[4]	I_{CCW}	—	25	—	mA
• In Stop mode[5]	I_{CCS}	—	15	—	mA
Input capacitance[6]	C_{IN}	—	—	10	pF

Notes:
1. Power-up sequence: During power-up, and throughout the DSP56321 operation, V_{CCQH} voltage must always be higher or equal to V_{CCQL} voltage.
2. Refers to MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, MODC/$\overline{\text{IRQC}}$, and MODD/$\overline{\text{IRQD}}$ pins.
3. **Section 4.3** provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see **Appendix A**). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications.
4. To obtain these results, all inputs must be terminated (that is, not allowed to float).
5. To obtain these results, all inputs not disconnected at Stop mode must be terminated (that is, not allowed to float), and the DPLL and on-chip crystal oscillator must be disabled.
6. Periodically sampled and not 100 percent tested.
7. V_{CCQH} = 3.3 V ±0.3 V, V_{CQLC} = 1.6 V ±0.1 V; T_J = –40°C to +100 °C, C_L = 50 pF
8. This characteristic does not apply to XTAL.
9. Driving EXTAL to the low V_{IHX} or the high V_{ILX} value may cause additional power consumption (DC current). To minimize power consumption, the minimum V_{IHX} should be no lower than 0.9 × V_{CCQH} and the maximum V_{ILX} should be no higher than 0.1 × V_{CCQH}.

2.4 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a V_{IL} maximum of 0.3 V and a V_{IH} minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Notes 7 and 9 of the previous table. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal's transition. DSP56321 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.4 V and 2.4 V, respectively.

Note: Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 16 MHz and rated speed with the DPLL enabled.

2.4.1 Internal Clocks

Table 2-4. Internal Clocks

Characteristics	Symbol	Expression		
		Min	Typ	Max
Internal operating frequency	f			
• With DPLL disabled		—	Ef/2	—
• With DPLL enabled		—	(Ef × MF)/(PDF × DF)	—
Internal clock cycle time	T_C			
• With DPLL disabled		—	2 × ET_C	—
• With DPLL enabled		—	ET_C × PDF × DF/MF	—
Internal clock high period	T_H			
• With DPLL disabled		—	ET_C	—
• With DPLL enabled		0.49 × T_C	—	0.51 × T_C

Table 2-5. External Clock Operation (Continued)

No.	Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz	
			Min	Max	Min	Max	Min	Max	Min	Max
4	EXTAL cycle time[3] • With DPLL disabled • With DPLL enabled	ET_C	 5.0 ns 5.0 ns	 ∞ 62.5 ns	 4.55 ns 4.55 ns	 ∞ 62.5 ns	 4.17 ns 4.17 ns	 ∞ 62.5 ns	 3.64 ns 3.64 ns	 ∞ 62.5 ns
7	Instruction cycle time = $I_{CYC} = ET_C$ • With DPLL disabled • With DPLL enabled	I_{CYC}	 10 ns 5.0 ns	 ∞ 1.6 µs	 9.09 ns 4.55 ns	 ∞ 1.6 µs	 8.33 ns 4.17 ns	 ∞ 1.6 µs	 7.28 ns 3.64 ns	 ∞ 1.6 µs

Notes:
1. The rise and fall time of this external clock should be 2 ns maximum.
2. Refer to **Table 2-6** for a description of PDF and PDFR.
3. Measured at 50 percent of the input transition.
4. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

Note: If an externally-supplied square wave voltage source is used, disable the internal oscillator circuit after boot-up by setting XTLD (PCTL Register bit 2 = 1—see the *DSP56321 Reference Manual*). The external square wave source connects to EXTAL and XTAL is not used. **Figure 2-2** shows the EXTAL input signal.

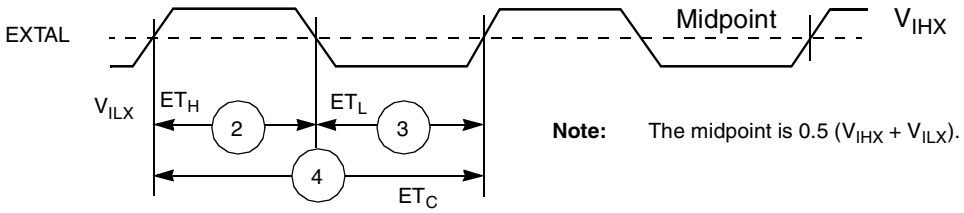


Figure 2-2. External Input Clock Timing

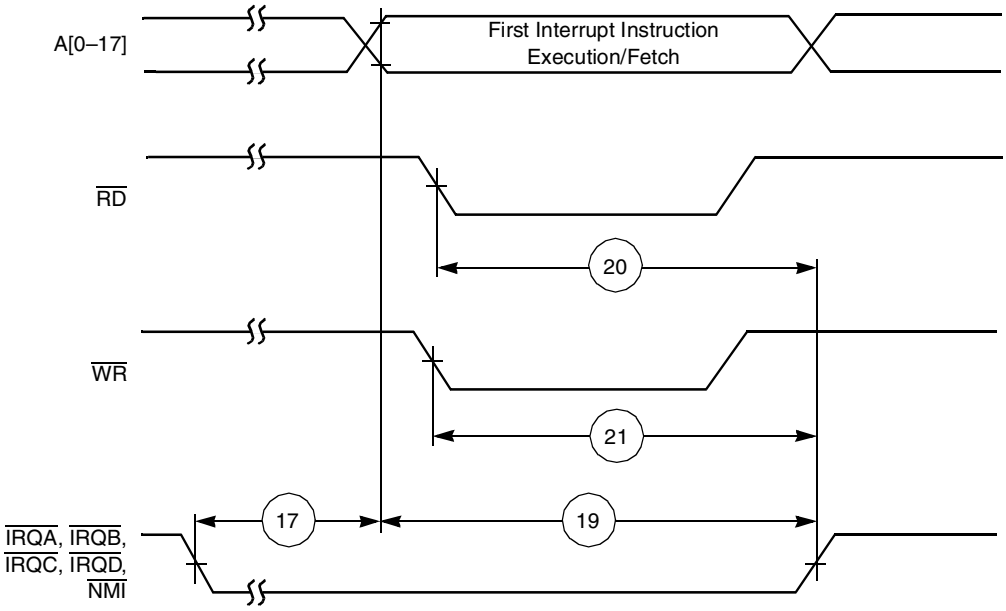
2.4.3 Clock Generator (CLKGEN) and Digital PLL (DPLL) Characteristics

Table 2-6. CLKGEN and DPLL Characteristics

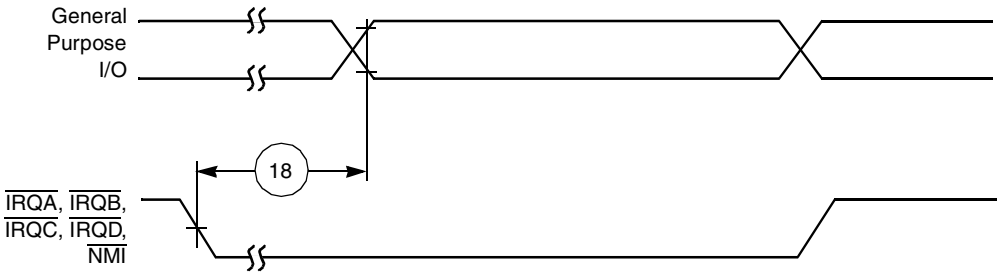
Characteristics	Symbol	200 MHz		220 MHz		240 MHz		275 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Predivision factor	PDF[1]	1	16	1	16	1	16	1	16	—
Predivider output clock frequency range	PDFR	16	32	16	32	16	32	16	32	MHz
Total multiplication factor[2]	MF	5	15	5	15	5	15	5	15	—
Multiplication factor integer part	MFI[1]	5	15	5	15	5	15	5	15	—
Multiplication factor numerator[3]	MFN	0	127	0	127	0	127	0	127	—
Multiplication factor denominator	MFD	1	128	1	128	1	128	1	128	—
Double clock frequency range	DDFR	160	400	160	440	160	480	160	550	MHz
Phase lock-in time[4]	DPLT	6.8[5]	150[6]	6.8[5]	150[6]	6.8[5]	150[6]	6.8[5]	150[6]	µs

Table 2-7. Reset, Stop, Mode Select, and Interrupt Timing[5] (CONTINUED)

No.	Characteristics	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
20	Delay from $\overline{RD}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7]	(WS + 3.25) × T_C – 10.94	—	Note 7	—	Note 7	—	Note 7	—	Note 7	ns
21	Delay from $\overline{WR}$ assertion to interrupt request deassertion for level sensitive fast interrupts[1, 6, 7] • SRAM WS = 3 • SRAM WS ≥ 4	 (WS + 3) × T_C – 10.94 (WS + 2.5) × T_C – 10.94	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 — —	 Note 7 Note 7	 ns ns
24	Duration for $\overline{IRQA}$ assertion to recover from Stop state		8.0	—	8.0	—	8.0	—	8.0	—	ns
25	Delay from $\overline{IRQA}$ assertion to fetch of first instruction (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL Bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop (PCTL Bit 1 = 1; Implies No Stop Delay)	 DPLT + (128K × T_C) DPLT + (23.75 ± 0.5) × T_C (10.0 ± 1.75) × T_C	 662.2 µs 6.9 41.25	 209.9 ms 188.8 58.8	 662.2 µs 6.9 37.5	 209.9 ms 188.8 53.3	 662.2 µs 6.9 34.4	 209.9 ms 188.8 49.0	 662.2 µs 6.9 30.0	 209.9 ms 188.8 43.0	 — µs ns
26	Duration of level sensitive $\overline{IRQA}$ assertion to ensure interrupt service (when exiting Stop)[2, 3] • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0) • DPLL is not active during Stop (PCTL bit 1 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1) • DPLL is active during Stop ((PCTL bit 1 = 0; implies no Stop delay)	 DPLT + (128 K × T_C) DPLT + (20.5 ± 0.5) × T_C 5.5 × T_C	 805.4 150.1 27.5	 — — —	 805.4 150.1 25	 — — —	 805.4 150.1 22.9	 — — —	 805.4 150.1 20.0	 — — —	 µs µs ns
27	Interrupt Request Rate • HI08, ESSI, SCI, Timer • DMA • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger) • $\overline{IRQ}$, $\overline{NMI}$ (level trigger)	 12T_C 8T_C 8T_C 12T_C	 — — — —	 60.0 40.0 40.0 60.0	 — — — —	 54.6 36.4 36.4 54.6	 — — — —	 50.0 33.4 33.4 50.0	 — — — —	 43.7 29.2 29.2 43.7	 ns ns ns ns
28	DMA Request Rate • Data read from HI08, ESSI, SCI • Data write to HI08, ESSI, SCI • Timer • $\overline{IRQ}$, $\overline{NMI}$ (edge trigger)	 6T_C 7T_C 2T_C 3T_C	 — — — —	 30.0 35.0 10.0 15.0	 — — — —	 27.3 31.9 9.1 13.7	 — — — —	 25.0 29.2 8.3 12.5	 — — — —	 21.84 25.48 7.28 10.92	 ns ns ns ns
29	Delay from $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{NMI}$ assertion to external memory (DMA source) access address out valid	4.25 × T_C + 2.0	23.25	—	21.34	—	19.72	—	17.45	—	ns



a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-4. External Fast Interrupt Timing

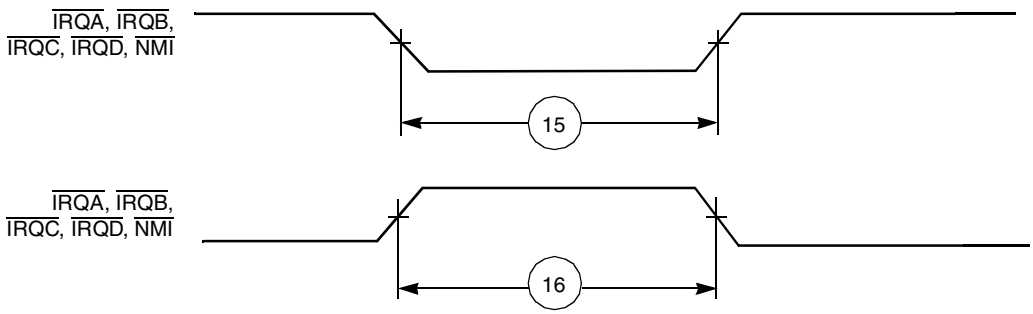


Figure 2-5. External Interrupt Timing (Negative Edge-Triggered)

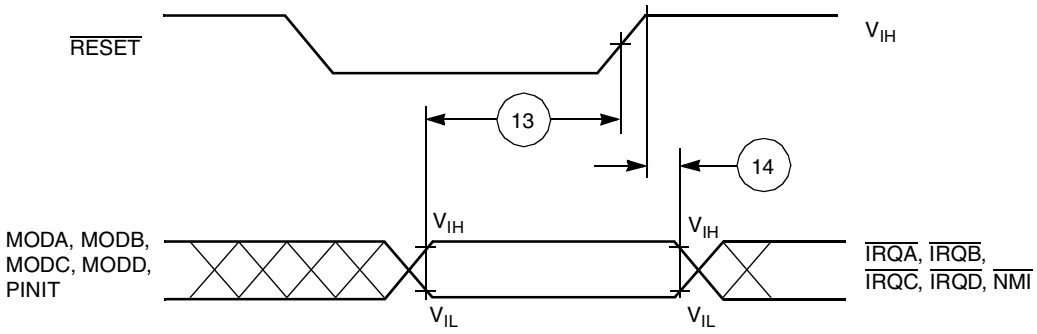


Figure 2-6. Operating Mode Select Timing

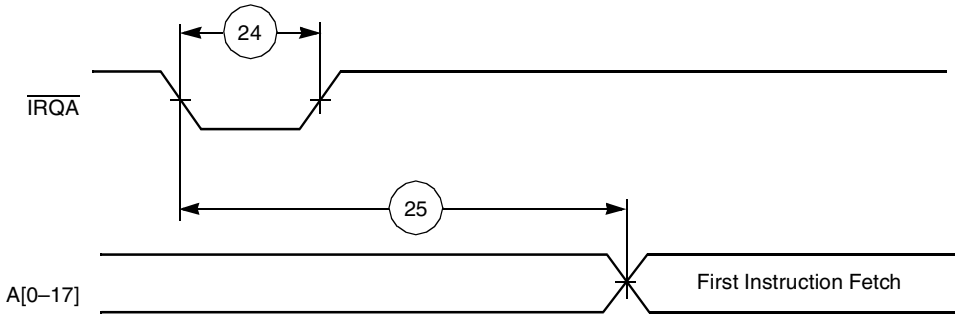


Figure 2-7. Recovery from Stop State Using IRQA

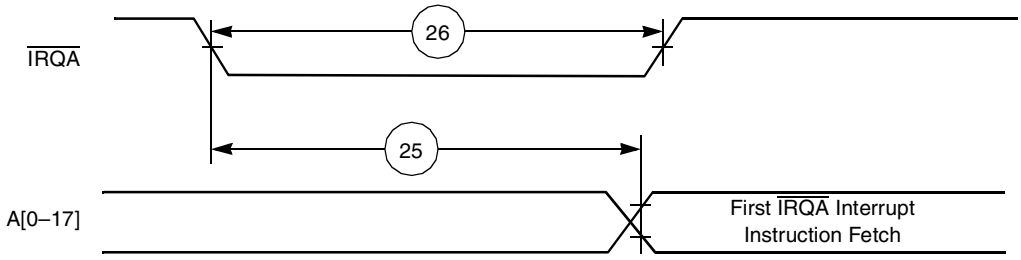


Figure 2-8. Recovery from Stop State Using IRQA Interrupt Service

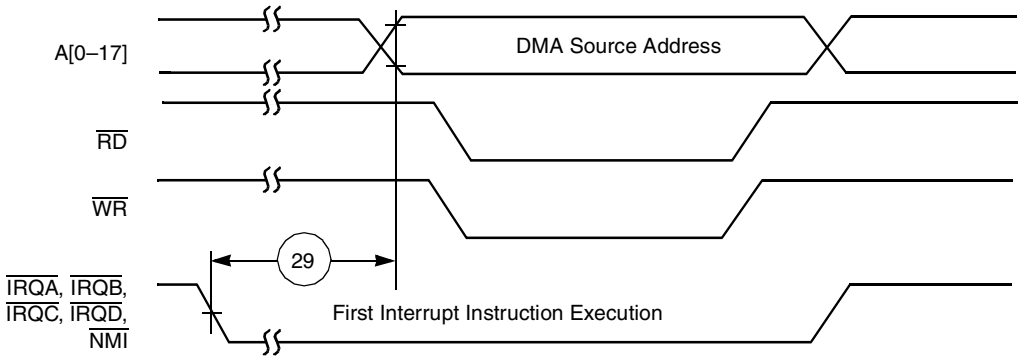


Figure 2-9. External Memory Access (DMA Source) Timing

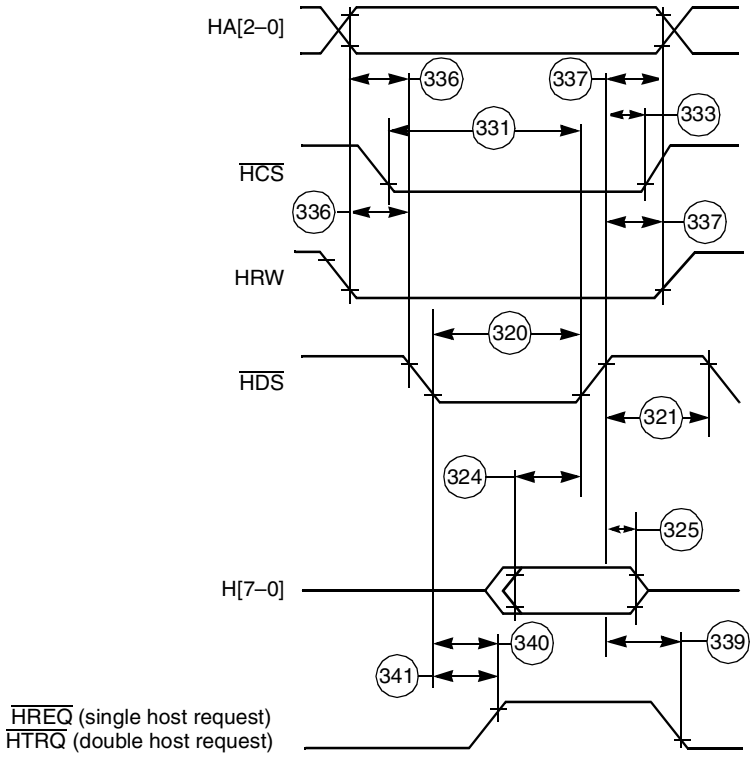


Figure 2-16. Write Timing Diagram, Non-Multiplexed Bus, Single Data Strobe

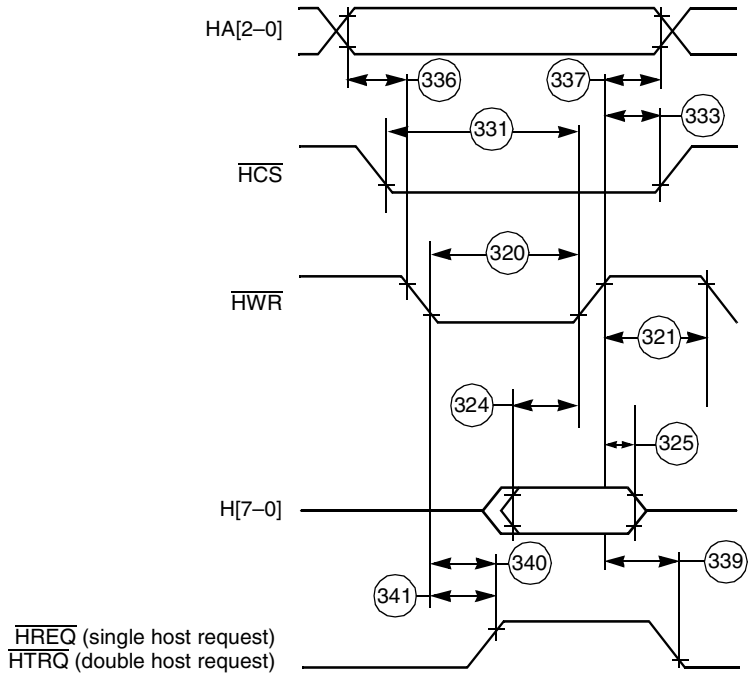


Figure 2-17. Write Timing Diagram, Non-Multiplexed Bus, Double Data Strobe

2.4.8 ESSI0/ESSI1 Timing

Table 2-12. ESSI Timings

No.	Characteristics[4, 6]	Symbol	Expression	200 MHz		220 MHz		240 MHz		275 MHz		Condition[5]	Unit
				Min	Max	Min	Max	Min	Max	Min	Max		
430	Clock cycle[1]	T_{ECCX} T_{ECCI}	$6 \times T_C$ $8 \times T_C$	30.0 40.0	— —	27.3 36.6	— —	25.0 33.3	— —	21.5 25.0	— —	x ck i ck	ns ns
431	Clock high period • For internal clock • For external clock		 $T_{ECCX}/2 - 3.7$ $T_{ECCI}/2 - 10.0$	 11.3 10.0	 — —	 9.9 8.2	 — —	 8.8 6.7	 — —	 7.21 2.5	 — —		 ns ns
432	Clock low period • For internal clock • For external clock		 $T_{ECCX}/2 - 3.7$ $T_{ECCI}/2 - 10.0$	 11.3 10.0	 — —	 9.9 8.2	 — —	 8.8 6.7	 — —	 7.21 2.5	 — —		 ns ns
433	RXC rising edge to FSR out (bit-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
434	RXC rising edge to FSR out (bit-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
435	RXC rising edge to FSR out (word-length-relative) high[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
436	RXC rising edge to FSR out (word-length-relative) low[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
437	RXC rising edge to FSR out (word-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
438	RXC rising edge to FSR out (word-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck	ns
440	Data in hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge[2]			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	5.0 10.0	— —	x ck i ck s	ns
445	Flags input hold time after RXC falling edge			3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	3.8 5.0	— —	x ck i ck s	ns
446	TXC rising edge to FST out (bit-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
447	TXC rising edge to FST out (bit-length) low			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
448	TXC rising edge to FST out (word-length-relative) high[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
449	TXC rising edge to FST out (word-length-relative) low[2]			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns
450	TXC rising edge to FST out (word-length) high			— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	— —	12.5 8.3	x ck i ck	ns

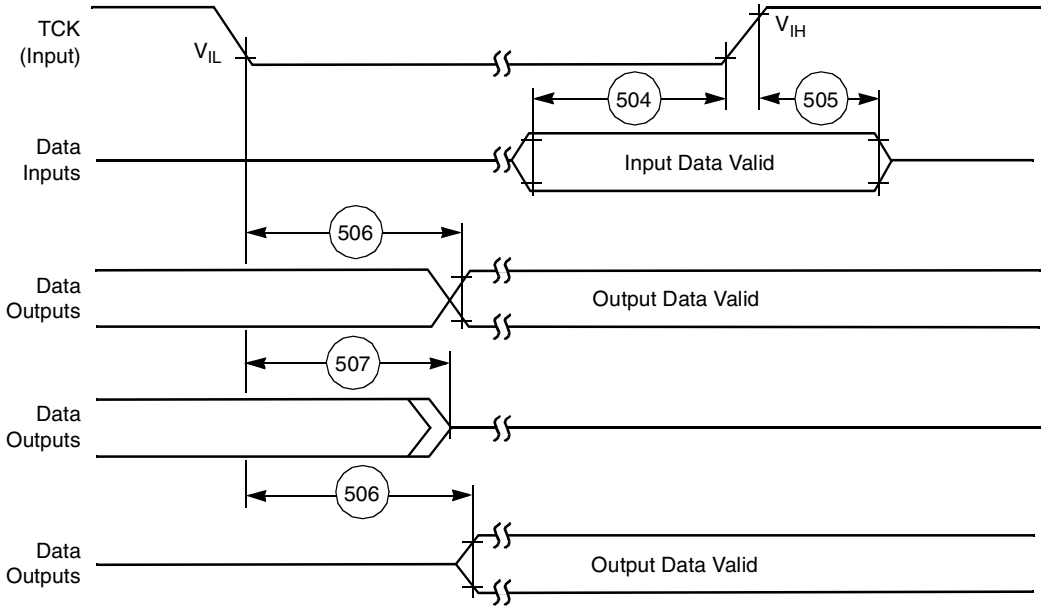


Figure 2-29. Boundary Scan (JTAG) Timing Diagram

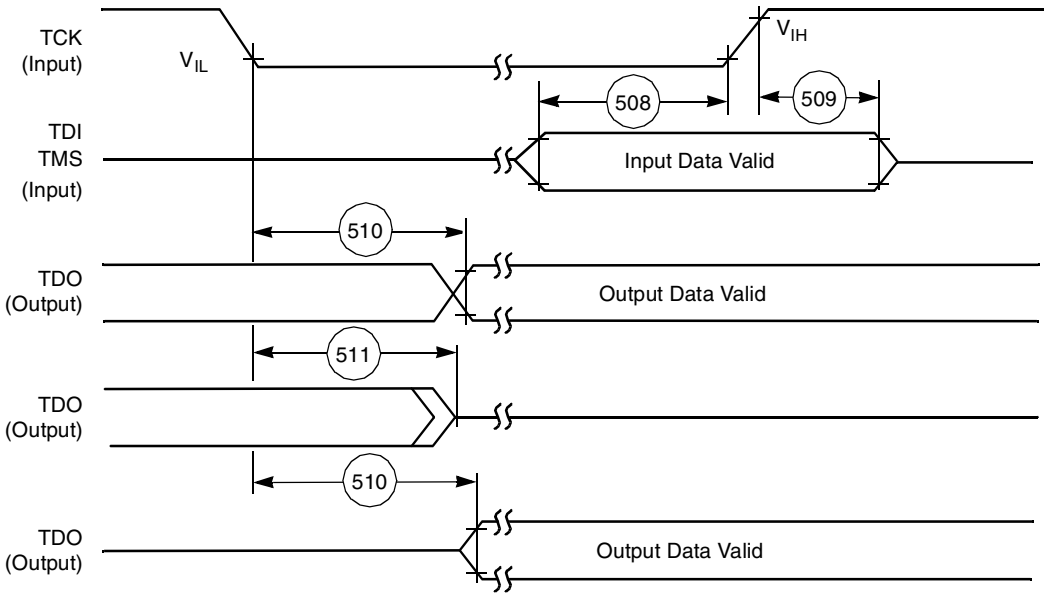


Figure 2-30. Test Access Port Timing Diagram

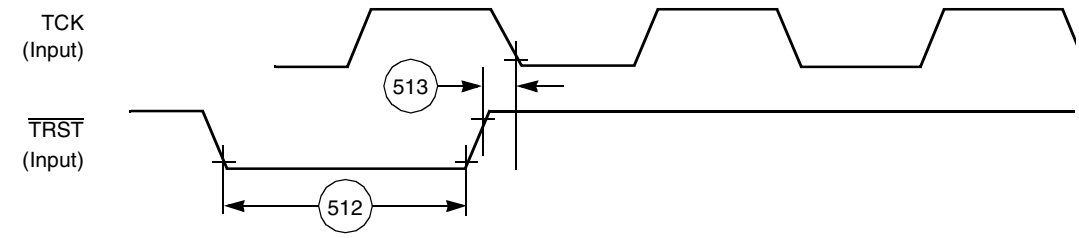


Figure 2-31. $\overline{\text{TRST}}$ Timing Diagram

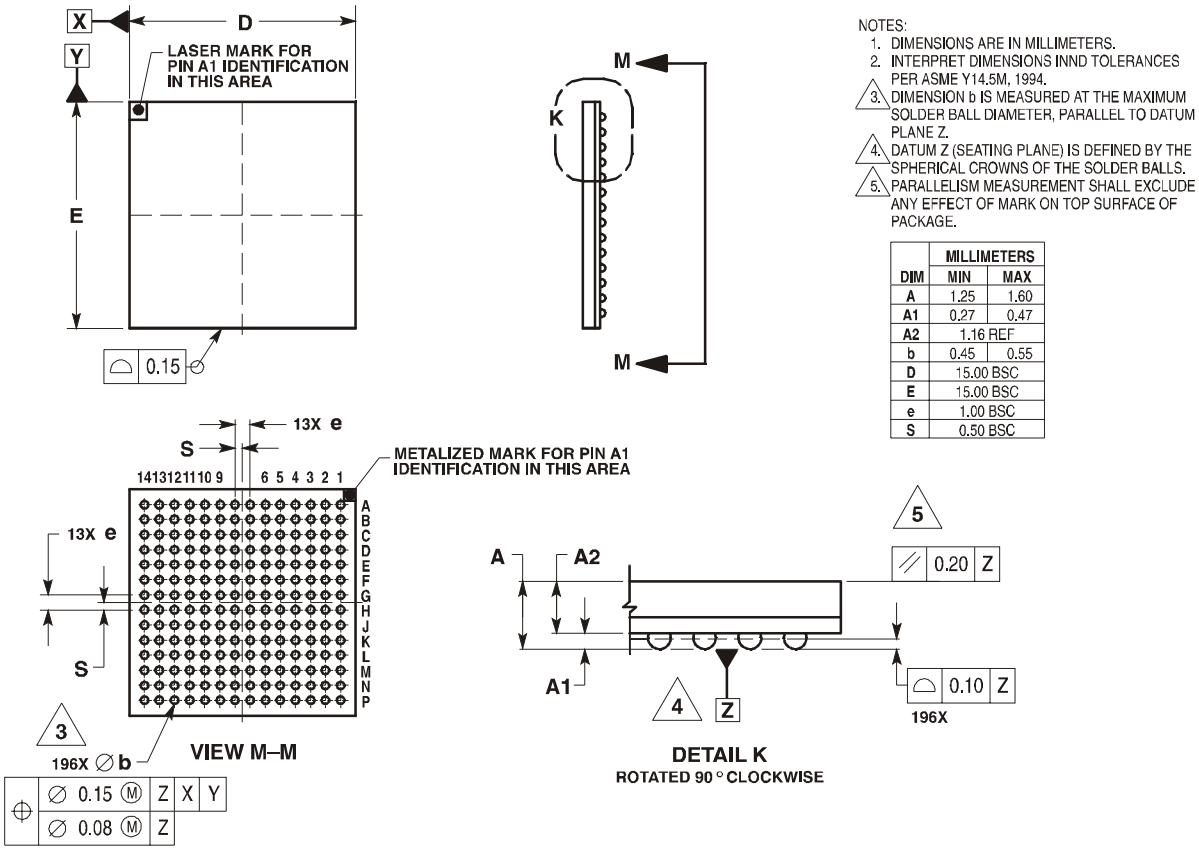
Table 3-1. Signal List by Ball Number

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	Not Connected (NC)	B12	D8	D9	GND
A2	SC11 or PD1	B13	D5	D10	GND
A3	TMS	B14	NC	D11	GND
A4	TDO	C1	SC02 or PC2	D12	D1
A5	MODB/$\overline{\text{IRQB}}$	C2	STD1 or PD5	D13	D2
A6	D23	C3	TCK	D14	V_{CCD}
A7	V_{CCD}	C4	MODA/$\overline{\text{IRQA}}$	E1	STD0 or PC5
A8	D19	C5	MODC/$\overline{\text{IRQC}}$	E2	V_{CCS}
A9	D16	C6	D22	E3	SRD0 or PC4
A10	D14	C7	V_{CCQL}	E4	GND
A11	D11	C8	D18	E5	GND
A12	D9	C9	V_{CCD}	E6	GND
A13	D7	C10	D12	E7	GND
A14	NC	C11	V_{CCD}	E8	GND
B1	SRD1 or PD4	C12	D6	E9	GND
B2	SC12 or PD2	C13	D3	E10	GND
B3	TDI	C14	D4	E11	GND
B4	$\overline{\text{TRST}}$	D1	PINIT/$\overline{\text{NMI}}$	E12	A17
B5	MODD/$\overline{\text{IRQD}}$	D2	SC01 or PC1	E13	A16
B6	D21	D3	$\overline{\text{DE}}$	E14	D0
B7	D20	D4	GND	F1	RXD or PE0
B8	D17	D5	GND	F2	SC10 or PD0
B9	D15	D6	GND	F3	SC00 or PC0
B10	D13	D7	GND	F4	GND
B11	D10	D8	GND	F5	GND

Table 3-2. Signal List by Signal Name (Continued)

Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.
TIO2	K3	V_{CCC}	P9	V_{CCQL}	C7
TMS	A3	V_{CCD}	A7	V_{CCQL}	G13
$\overline{TRST}$	B4	V_{CCD}	C9	V_{CCQL}	H2
TXD	G3	V_{CCD}	C11	V_{CCQL}	M6
V_{CCA}	H12	V_{CCD}	D14	V_{CCQL}	N9
V_{CCA}	K12	V_{CCH}	M4	V_{CCS}	E2
V_{CCA}	L12	V_{CCQH}	F12	V_{CCS}	K1
V_{CCC}	N12	V_{CCQH}	H1	$\overline{WR}$	M11
		V_{CCQH}	M7	XTAL	P8

3.2 MAP-BGA Package Mechanical Drawing



CASE 1128C–01
ISSUE O

DATE 07/28/98

Figure 3-3. DSP56321 Mechanical Information, 196-pin MAP-BGA Package

```
;
; Load the Y-data
;
       move   #INT_YDAT,r0
       move   #YDAT_START,r1
       do     #(YDAT_END-YDAT_START),YLOAD_LOOP
       move   p:(r1)+,x0
       move   x0,y:(r0)+
YLOAD_LOOP
;

       jmp    INT_PROG

PROG_START
       move   #$0,r0
       move   #$0,r4
       move   #$3f,m0
       move   #$3f,m4
;
       clr    a
       clr    b
       move   #$0,x0
       move   #$0,x1
       move   #$0,y0
       move   #$0,y1
       bset   #4,omr        ; ebd
;
sbr    dor    #60,_end
       mac    x0,y0,ax:(r0)+,x1   y:(r4)+,y1
       mac    x1,y1,ax:(r0)+,x0   y:(r4)+,y0
       add    a,b
       mac    x0,y0,ax:(r0)+,x1
       mac    x1,y1,a             y:(r4)+,y0
       move   b1,x:$ff
_end
       bra    sbr
       nop
       nop
       nop
       nop
PROG_END
       nop
       nop


XDAT_START
;      org    x:0
       dc     $262EB9
       dc     $86F2FE
       dc     $E56A5F
       dc     $616CAC
       dc     $8FFD75
       dc     $9210A
       dc     $A06D7B
       dc     $CEA798
       dc     $8DFBF1
       dc     $A063D6
       dc     $6C6657
       dc     $C2A544
       dc     $A3662D
       dc     $A4E762
       dc     $84F0F3
       dc     $E6F1B0
```

```
M_CD EQU $FFF                       ; Clock Divider Mask (CD0-CD11)
M_COD EQU 12                        ; Clock Out Divider
M_SCP EQU 13                        ; Clock Prescaler
M_RCM EQU 14                        ; Receive Clock Mode Source Bit
M_TCM EQU 15                        ; Transmit Clock Source Bit

;-------------------------------------------------------------------------
;
;       EQUATES for Synchronous Serial Interface (SSI)
;
;-------------------------------------------------------------------------

;
;       Register Addresses Of SSI0
M_TX00 EQU $FFFFBC                  ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB                  ; SSIO Transmit Data Register 1
M_TX02 EQU $FFFFBA                  ; SSIO Transmit Data Register 2
M_TSR0 EQU $FFFFB9                  ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8                   ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7                ; SSI0 Status Register
M_CRB0 EQU $FFFFB6                  ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5                  ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4                 ; SSI0 Transmit Slot Mask Register A
M_TSMB0 EQU $FFFFB3                 ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2                 ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1                 ; SSI0 Receive Slot Mask Register B

;       Register Addresses Of SSI1
M_TX10 EQU $FFFFAC                  ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB                  ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA                  ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9                  ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8                   ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7                ; SSI1 Status Register
M_CRB1 EQU $FFFFA6                  ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5                  ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4                 ; SSI1 Transmit Slot Mask Register A
M_TSMB1 EQU $FFFFA3                 ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2                 ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1                 ; SSI1 Receive Slot Mask Register B

;       SSI Control Register A Bit Flags

M_PM EQU $FF                        ; Prescale Modulus Select Mask (PM0-PM7)
M_PSR EQU 11                        ; Prescaler Range
M_DC EQU $1F000                     ; Frame Rate Divider Control Mask (DC0-DC7)
M_ALC EQU 18                        ; Alignment Control (ALC)
M_WL EQU $380000                    ; Word Length Control Mask (WL0-WL7)
M_SSC1 EQU 22                       ; Select SC1 as TR #0 drive enable (SSC1)

;       SSI Control Register B Bit Flags

M_OF EQU $3                         ; Serial Output Flag Mask
M_OF0 EQU 0                         ; Serial Output Flag 0
M_OF1 EQU 1                         ; Serial Output Flag 1
M_SCD EQU $1C                       ; Serial Control Direction Mask
M_SCD0 EQU 2                        ; Serial Control 0 Direction
M_SCD1 EQU 3                        ; Serial Control 1 Direction
M_SCD2 EQU 4                        ; Serial Control 2 Direction
M_SCKD EQU 5                        ; Clock Source Direction
M_SHFD EQU 6                        ; Shift Direction
M_FSL EQU $180                      ; Frame Sync Length Mask (FSL0-FSL1)
M_FSL0 EQU 7                        ; Frame Sync Length 0
```

```
;       Register Addresses Of DMA0

M_DSR0 EQU $FFFFEF               ; DMA0 Source Address Register
M_DDR0 EQU $FFFFEE               ; DMA0 Destination Address Register
M_DCO0 EQU $FFFFED               ; DMA0 Counter
M_DCR0 EQU $FFFFEC               ; DMA0 Control Register

;       Register Addresses Of DMA1

M_DSR1 EQU $FFFFEB               ; DMA1 Source Address Register
M_DDR1 EQU $FFFFEA               ; DMA1 Destination Address Register
M_DCO1 EQU $FFFFE9               ; DMA1 Counter
M_DCR1 EQU $FFFFE8               ; DMA1 Control Register

;       Register Addresses Of DMA2

M_DSR2 EQU $FFFFE7               ; DMA2 Source Address Register
M_DDR2 EQU $FFFFE6               ; DMA2 Destination Address Register
M_DCO2 EQU $FFFFE5               ; DMA2 Counter
M_DCR2 EQU $FFFFE4               ; DMA2 Control Register

;       Register Addresses Of DMA4

M_DSR3 EQU $FFFFE3               ; DMA3 Source Address Register
M_DDR3 EQU $FFFFE2               ; DMA3 Destination Address Register
M_DCO3 EQU $FFFFE1               ; DMA3 Counter
M_DCR3 EQU $FFFFE0               ; DMA3 Control Register

;       Register Addresses Of DMA4


M_DSR4 EQU $FFFFDF               ; DMA4 Source Address Register
M_DDR4 EQU $FFFFDE               ; DMA4 Destination Address Register
M_DCO4 EQU $FFFFDD               ; DMA4 Counter
M_DCR4 EQU $FFFFDC               ; DMA4 Control Register

;       Register Addresses Of DMA5

M_DSR5 EQU $FFFFDB               ; DMA5 Source Address Register
M_DDR5 EQU $FFFFDA               ; DMA5 Destination Address Register
M_DCO5 EQU $FFFFD9               ; DMA5 Counter
M_DCR5 EQU $FFFFD8               ; DMA5 Control Register

;      DMA Control Register

M_DSS EQU $3                     ; DMA Source Space Mask (DSS0-Dss1)
M_DSS0 EQU 0                     ; DMA Source Memory space 0
M_DSS1 EQU 1                     ; DMA Source Memory space 1
M_DDS EQU $C                     ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2                     ; DMA Destination Memory Space 0
M_DDS1 EQU 3                     ; DMA Destination Memory Space 1
M_DAM EQU $3f0                   ; DMA Address Mode Mask (DAM5-DAM0)
M_DAM0  EQU 4                    ; DMA Address Mode 0
M_DAM1  EQU 5                    ; DMA Address Mode 1
M_DAM2  EQU 6                    ; DMA Address Mode 2
M_DAM3  EQU 7                    ; DMA Address Mode 3
M_DAM4  EQU 8                    ; DMA Address Mode 4
M_DAM5  EQU 9                    ; DMA Address Mode 5
M_D3D EQU 10                     ; DMA Three Dimensional Mode
M_DRS EQU $F800                  ; DMA Request Source Mask (DRS0-DRS4)
M_DCON EQU 16                    ; DMA Continuous Mode
M_DPR EQU $60000                 ; DMA Channel Priority
```

```
M_Z EQU 2                           ; Zero
M_N EQU 3                           ; Negative
M_U EQU 4                           ; Unnormalized
M_E EQU 5                           ; Extension
M_L EQU 6                           ; Limit
M_S EQU 7                           ; Scaling Bit
M_I0 EQU 8                          ; Interupt Mask Bit 0
M_I1 EQU 9                          ; Interupt Mask Bit 1
M_S0 EQU 10                         ; Scaling Mode Bit 0
M_S1 EQU 11                         ; Scaling Mode Bit 1
M_SC EQU 13                         ; Sixteen_Bit Compatibility
M_DM EQU 14                         ; Double Precision Multiply
M_LF EQU 15                         ; DO-Loop Flag
M_FV EQU 16                         ; DO-Forever Flag
M_SA EQU 17                         ; Sixteen-Bit Arithmetic
M_CE EQU 19                         ; Instruction Cache Enable
M_SM EQU 20                         ; Arithmetic Saturation
M_RM EQU 21                         ; Rounding Mode
M_CP0 EQU 22                        ; bit 0 of priority bits in SR
M_CP1 EQU 23                        ; bit 1 of priority bits in SR

;       control and status bits in OMR
M_CDP EQU $300; mask for CORE-DMA priority bits in OMR
M_MA    equ0                        ; Operating Mode A
M_MB   equ1                         ; Operating Mode B
M_MC    equ2                        ; Operating Mode C
M_MD    equ3                        ; Operating Mode D
M_EBD EQU 4                         ; External Bus Disable bit in OMR
M_SD EQU 6                          ; Stop Delay
M_MS EQU 7                          ; Memory Switch bit in OMR
M_CDP0 EQU 8                        ; bit 0 of priority bits in OMR
M_CDP1 EQU 9                        ; bit 1 of priority bits in OMR
M_BEN   EQU 10                      ; Burst Enable
M_TAS  EQU 11                       ; TA Synchronize Select
M_BRT  EQU 12                       ; Bus Release Timing
M_ATE EQU 15                        ; Address Tracing Enable bit in OMR.
M_XYS EQU 16                        ; Stack Extension space select bit in OMR.
M_EUN EQU 17                        ; Extensed stack UNderflow flag in OMR.
M_EOV EQU 18                        ; Extended stack OVerflow flag in OMR.
M_WRP EQU 19                        ; Extended WRaP flag in OMR.
M_SEN EQU 20                        ; Stack Extension Enable bit in OMR.




;*************************************************************************
;
;     EQUATES for DSP56321 interrupts
;
;*************************************************************************

       page   132,55,0,0,0
       opt    mex

intequ  ident   1,0

       if     @DEF(I_VEC)
                                    ;leave user definition as is.
       else
I_VEC EQU $0
       endif
```