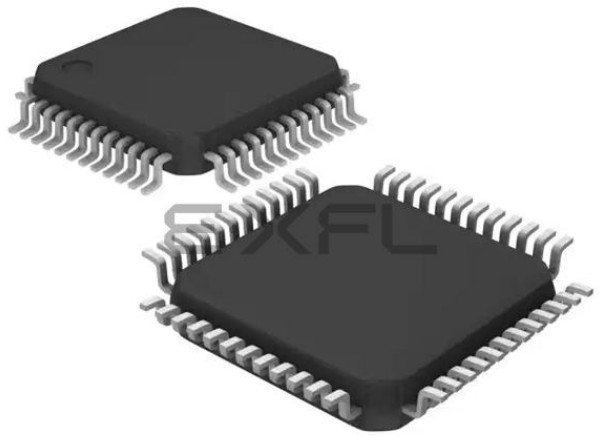


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano102lb1an

1 GENERAL DESCRIPTION

The Nano112 series ultra-low-power 32-bit microcontroller embeded with ARM® Cortex™-M0 core operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded Flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). The Nano112 series integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 12-bit SAR ADC, comparators and provides high performance connectivity peripheral interfaces such as UART, SPI, I^2C, GPIOs, and ISO-7816-3 for Smart card. The Nano112 series supports Brown-out Detector, Power-down mode with RTC turn on, RAM retention is less than 1.5 uA, Deep power down mode with RAM retention is less than 650 nA and fast wake-up via many peripheral interfaces.

The Nano112 series provides low voltage, low operating power consumption, low standby current, high integration peripherals, high-efficiency operation, fast wake-up function and the lowest cost 32-bit microcontrollers. The Nano112 series is suitable for a wide range of battery device applications such as:

- Wearable Device
- Smart Watch
- Wireless Gaming Control
- Hand-Held Medical Device
- RFID Reader
- Mobile Payment Smart Card Reader
- Security Alarm System
- Smart Home Appliance
- Wireless Thermostats
- Wireless Sensors Node Device (WSND)
- Wireless Auto Meter Reading (AMR)
- Portable Wireless Data Collector
- Smart Water, Gas, Heat Meters

The Nano112 series includes two product lines: Nano102 Base line and Nano112 LCD line.

The Nano102 Base line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates RTC, 8- channels 12-bit SAR ADC, 2xComparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I^2Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano102 Base line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

The Nano112 LCD line, an ultra-low-power 32-bit microcontroller embedded with ARM® Cortex™-M0 core, operates at low voltage range from 1.8V to 3.6V and runs up to 32 MHz frequency with 16/32 Kbytes embedded flash and 4/8 Kbytes embedded SRAM and 4 Kbytes Flash loader memory for In-System Programming (ISP). It integrates 4 COM x 36 SEG or 6 COM x 34 SEG LCD controller, RTC, 8-channels 12-bit SAR ADC, 2 x Comparators and provides high performance connectivity peripheral interfaces such as 2 x Low Power UARTs, 2 x SPIs, 2 x I^2Cs, GPIOs, and 2 x ISO-7816-3 for Smart card. The Nano112 LCD line supports Brown-out Detector, Power-down mode with RAM retention and fast wake-up via many peripheral interfaces.

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano102 Features – Base Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access
  - 16/32 Kbytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 5 channels: 4 PDMA channels and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

新唐科技 NUVOTON INTELLECTUAL PROPERTY

- Up to two sets of SPI controllers
- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up(SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Wake system up(address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 8-ch single-ended input from external pin (PA.0 ~ PA.7)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}.
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Only scan on enabled channels

- Threshold voltage detection (comparator function)
- Conversion started by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1℃ resolution
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

新唐科技 nuvoTon INTELLECTUAL PROPERTY

- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up (SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requestING the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave address with mask option)
  - Wake system up (address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 7-ch single-ended input from external pin (PA.0 ~ PA.6)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to

新唐科技 nuvoTon INTELLECTUAL PROPERTY

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

4.2.2 NuMicro™ Nano112 LCD Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	I/O	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10KHz / 12MHz / 16MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I²C											
NANO112LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112SB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112RB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112RC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112VC2AN	32K	8K	Configurable	4K	up to 80	4	4	2	2	2	4	8	√	√	4	4x36, 6x34	2	√	LQFP100	-40 to +85

LQFP48: 7x7mm
LQFP64: 7x7mm
LQFP64*: 10x10mm

新唐科技 NUVOTON INTELLECTUAL PROPERTY

4.4 Pin Description

4.4.1 NuMicro™ Nano102 Pin Description

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
1			PB.10	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SPI0_MOSI1	I/O	SPI0 2nd MOSI (Master Out, Slave In) pin
2			PB.11	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SPI0_MISO1	I/O	SPI0 2rd MISO (Master In, Slave Out) pin
			TM1	I/O	Timer1 external counter input or Timer1 toggle out
3	1	1	PB.12	I/O	General purpose digital I/O pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			FCLK0	O	Frequency Divider0 output pin
4	2	2	PB.13	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
5	3	3	PB.14	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI0_CLK	I/O	SPI0 serial clock pin
6	4	4	PB.15	I/O	General purpose digital I/O pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI0_SS0	I/O	SPI0 1st slave select pin
7	5		PC.0	I/O	General purpose digital I/O pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			I2C0_SCL	I/O	I2C0 clock pin
			PWM0_CH0	I/O	PWM0 Channel0 output
8	6		PC.1	I/O	General purpose digital I/O pin
			I2C0_SDA	I/O	I2C0 data I/O pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG12	**O**	LCD segment output 12 at 64-pin
			LCD_SEG5	**O**	LCD segment output 5 at 48-pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin (SC0_UART_RXD)
20	14	12	PC.7	**I/O**	General purpose digital I/O pin
			LCD_SEG15	**O**	LCD segment output 15 at 100-pin
			LCD_SEG11	**O**	LCD segment output 11 at 64-pin
			LCD_SEG4	**O**	LCD segment output 4 at 48-pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			SC0_PWR	**O**	SmartCard0 Power pin
21	15	13	PC.8	**I/O**	General purpose digital I/O pin
			LCD_SEG14	**O**	LCD segment output 14 at 100-pin
			LCD_SEG10	**O**	LCD segment output 10 at 64-pin
			LCD_SEG3	**O**	LCD segment output 3 at 48-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	**O**	SmartCard0 RST pin
22	16	14	PC.9	**I/O**	General purpose digital I/O pin
			LCD_SEG13	**O**	LCD segment output 13 at 100-pin
			LCD_SEG9	**O**	LCD segment output 9 at 64-pin
			LCD_SEG2	**O**	LCD segment output 2 at 48-pin
23			V_{DD}	**P**	Power supply for I/O ports and LDO source
24			V_{SS}	**G**	Ground for digital circuit
25			V_{SS}	**G**	Ground for digital circuit
26			PC.10	**I/O**	General purpose digital I/O pin
			LCD_SEG12	**O**	LCD segment output 12 at 100-pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
			SC1_CD	**I**	SmartCard1 card detect pin
27			PC.11	**I/O**	General purpose digital I/O pin
			LCD_SEG11	**O**	LCD segment output 11 at 100-pin
			I2C1_SDA	**I/O**	I^2C 1 data I/O pin
			SC1_PWR	**O**	SmartCard1 PWR pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
84			PA.8	**I/O**	General purpose digital I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
85			PA.9	**I/O**	General purpose digital I/O pin
			SC0_RST	**O**	SmartCard0 RST pin
86			PA.10	**I/O**	General purpose digital I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
87			PA.11	**I/O**	General purpose digital I/O pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			STADC	**I**	ADC external trigger input.
88	56	45	PA.12	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 48-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	**I/O**	I^2C 0 clock pin
			ACMP1_P	**AI**	Comparator1 P-end input
89	57	46	PA.13	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 48-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_N	**AI**	Comparator1 N-end input
90	58	47	PA.14	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			LCD_SEG31	**O**	LCD segment output 31 at 64-pin
			LCD_SEG17	**O**	LCD segment output 17 at 48-pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
91	59	48	PA.15	**I/O**	General purpose digital I/O pin
			LCD_SEG30	**O**	LCD segment output 30 at 64-pin
			LCD_SEG16	**O**	LCD segment output 16 at 48-pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

新唐科技 nuvoTon INTELLECTUAL PROPERTY

6.5 Clock Controller

6.5.1 Overview

The clock controller generates clocks for the whole chip, Iincluding system clocks (CPU clock, HCLKx, and PCLKx) and all peripheral module clocks. HCLKx means AHB bus clock for peripherals on AHB bus. PCLKx means APB bus clock for peripherals on APB bus. PCLKx can be the same as HCLKx or devided from HCLKx. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit PD_EN(PWRCTL[6]) and executes the WFI instruction. In the Power-down mode, clock controller turns off the external high frequency crystal, internal high frequency oscillator, and system clocks (CPU clock, HCLKx, and PCLKx) to reduce the power consumption.

The clock controller consists of 5 sources as listed below:

- 32768Hz external low speed crystal oscillator (LXT)
- 4~ 24 MHz external high speed crystal oscillator (HXT)
- 12/16 MHz internal high speed RC oscillator (HIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT or HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

6.5.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- High frequency crystal, internal high frequency oscillator, and system clocks will be turned off when chip is in Power-down mode.

新唐科技 nuvoTon INTELLECTUAL PROPERTY

6.10.2 Features

6.10.2.1 PWM Function:

- PWM controllers has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators
- Up to 4 PWM channels or 2 PWM paired channels
- Up to 16 bits PWM counter width
- PWM Interrupt request synchronous with PWM period
- Single-shot or Continuous mode
- Two Dead-Zone generators

6.10.2.2 Capture Function:

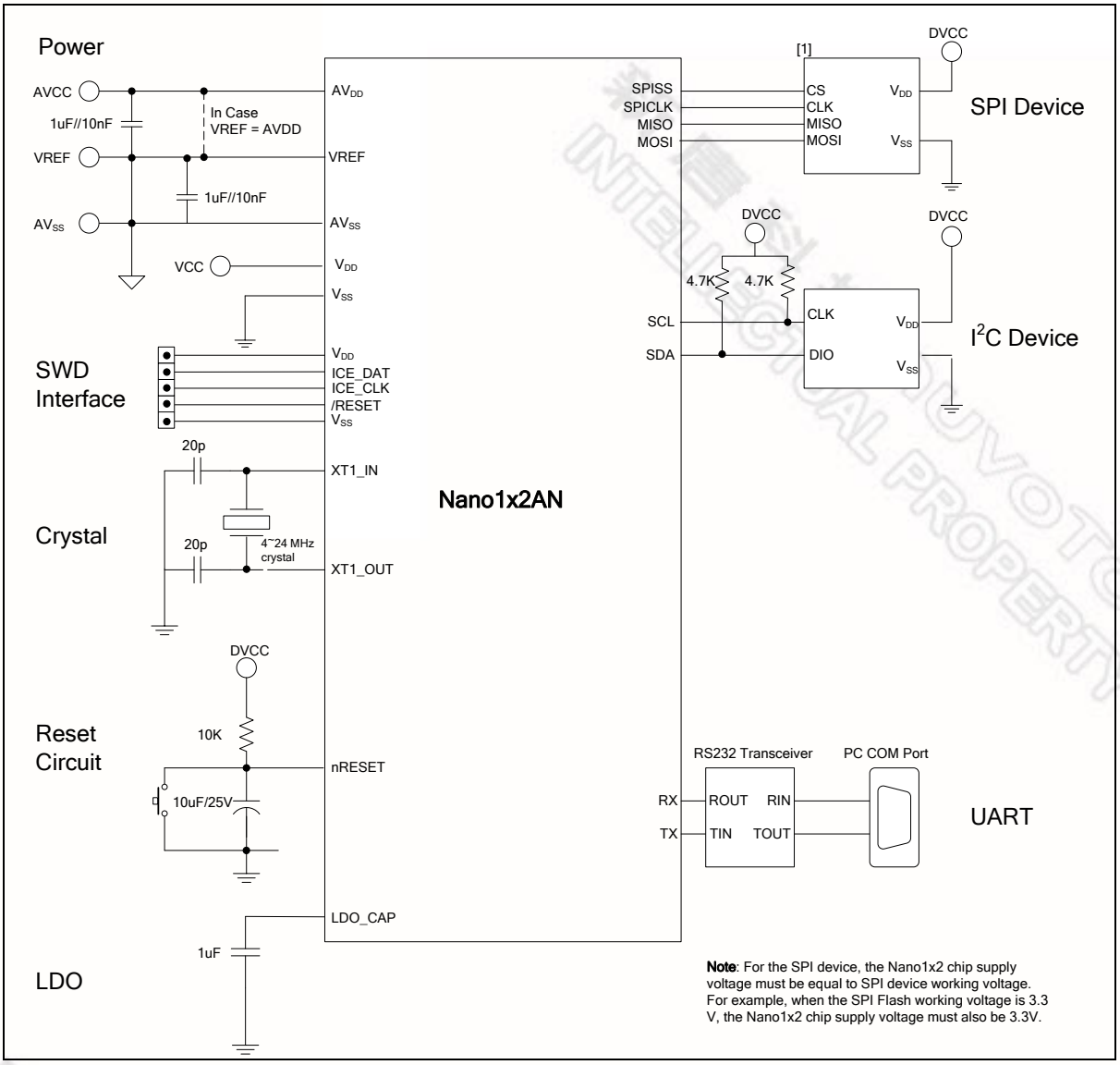
- Timing control logic shared with PWM timer.
- 4 Capture input channels shared with 4 PWM output channels.
- Each channel supports one rising latch register CRL (PWM_CRL0[15:0]), one falling latch register CFL (PWM_CFL0[15:0]) and Capture interrupt flag CAPIF0 (PWM_CAPINTSTS[0]).
- Four 16-bit counters for four capture channels or two 32-bit counter for two capture channels when cascade is enabled: when CH01CASKEN (PWM_CAPCTL[13]) is set, the original 16-bit counter of channel 1 will combine with channel 0's 16 bit counter for channel 0 input capture counting and so does CH23CASKEN(PWM_CAPCTL[29]) for channel 2, 3
- Supports PDMA transfer function for PWM channel 0, 2

新唐科技 NUVOTON INTELLECTUAL PROPERTY

- Supports multiple address recognition (Two slave addresses with mask option)
- Supports Power-down wake-up function
- Supports two-Level FIFO

新唐科技 NUVOTON INTELLECTUAL PROPERTY

7 APPLICATION CIRCUIT



新唐科技 NUVOTON INTELLECTUAL PROPERTY

9.2 Nano102/Nano112 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 32 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.8	-	3.6	V	V_{DD} =1.8V up to 32 MHz
Power Ground	V_{SS} AV_{SS}	-0.3	-		V	
LDO Output Voltage	V_{LDO1}	1.62	1.8	1.98	V	MCU operating in Run or Idle mode
		1.44	1.6	1.76	V	Set LDO_LEVEL(LDO_CTL[3:2]) = 0x1
	V_{LDO2}	1.49	1.66	1.83	V	MCU operating in Power-down mode
	C_{LDO}		1		uF	Connect to LDO_CAP pin
Analog Operating Voltage	AV_{DD}		V_{DD}		V	
Operating Current Normal Run Mode HCLK =32 MHz wkhile(1){}executed from flash V_{LDO1}=1.8 V	I_{DD5}		11.7		mA	V_{DD}: 3.3 V; HXT: 12 MHz; HIRC: X; PLL: V; All digital module: V
	I_{DD6}		5.8		mA	3.3 V; 12 MHz; X; V; X
	I_{DD7}		10.9		mA	1.8 V; 12 MHz; X; V; V
	I_{DD8}		5.6		mA	1.8 V; 12 MHz; X; V; X
Operating Current Normal Run Mode HCLK =32 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD9}		3.9		mA	3.3 V; 12 MHz; X; X; V
	I_{DD10}		1.9		mA	3.3 V; 12 MHz; X; X; X
	I_{DD11}		3.8		mA	1.8 V; 12 MHz; X; X; V
	I_{DD12}		1.9		mA	1.8 V; 12 MHz; ; ;

新唐科技 NUVOTON INTELLECTUAL PROPERTY

9.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F_{HRC}	11.88	12	12.12	MHz	25°C, VDD = 3.3V
		11.76	12	12.24	MHz	-40°C ~ +85°C, VDD = 1.8V~3.6V
		11.88	12	12.12	MHz	-40°C ~ +85 °C, VDD = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]=”10”
Operating current	I_{HRC}		250		μA	

Note: Internal oscillator operation voltage comes from LDO.

9.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	kHz	25°C, VDD = 3V
		5	10	15	kHz	-40°C ~+85 °C, VDD = 1.8V~3.6V
Operating current	I_{LRC}		0.3		μA	VDD = 3V

Note: Internal oscillator operation voltage comes from LDO.

9.4 Analog Characteristics

9.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8		3.6	V	$AV_{DD} = V_{DD}$
Operating current (AV_{DD} current) (Enable ADC and disable all	I_{ADC32}		120		μA	$AV_{DD} = V_{DD}$ = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 32 MHz

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
other analog modules)	I_{ADC2}		30		μA	AV_{DD} = V_{DD} = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 2 MHz
Resolution	R_{ADC}			12	Bit	
Reference voltage	V_{REF}	1.8		A_{VDD}	V	
Reference input current (Avg.)	I_{REF}			1	μA	
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	1			μS	
Conversion Rate	F_{SPS}			1.5M	Hz	V_{DD} = 3V
Integral Non-Linearity Error	INL		±1		LSB	V_{REF} is external Vref pin
Differential Non-Linearity	DNL		±0.8		LSB	V_{REF} is external Vref pin
Gain error	E_G		±2		LSB	V_{REF} is external Vref pin
Offset error	E_{OFFSET}		±1.5		LSB	V_{REF} is external Vref pin
Absolute error	E_{ABS}		-	±6	LSB	V_{REF} is external Vref pin
ADC Clock frequency	F_{ADC}	0.25		32	MHz	
Clock cycle	AD_{CYC}	20			Cycle	
Internal Capacitance	C_{IN}	-	5	-	pF	
Monotonic	-	Guaranteed			-	

9.4.2 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	-
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Quiescent Current	-	1		μA	AV_{DD} = 3V
V_{BOD}	Brown-out Voltage 25℃	2.4	2.5	2.6	V	BODCTL[2] = 1
		1.9	2.0	2.1	V	BODCTL[1] = 1
		1.6	1.7	1.8	V	BODCTL[0] = 1

新唐科技 NUVOTON INTELLECTUAL PROPERTY

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.