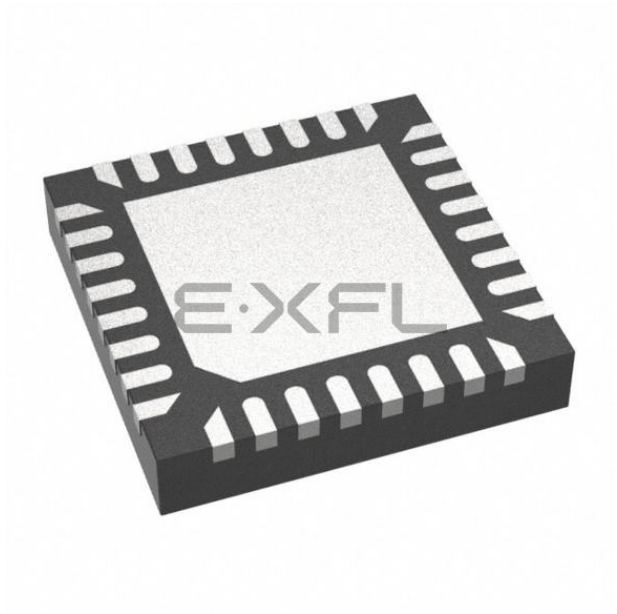
Nuvoton Technology Corporation - NANO102ZC2AN Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	33-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano102zc2an

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out

2.2 Nano112 Features – LCD Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access.
  - 16/32 Kbytes application program memory (APROM)
  - 4 Kbytes In System Programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 5 channels: 4 PDMA channels, and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC
    - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
      - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$

- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(10x10) / 64-pin(7x7) / 48-pin(7x7)

QEI	Quadrature Encoder Interface
SDIO	Secure Digital Input/Output
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4.3.2.3 NuMicro™ Nano112 LQFP 48-pin

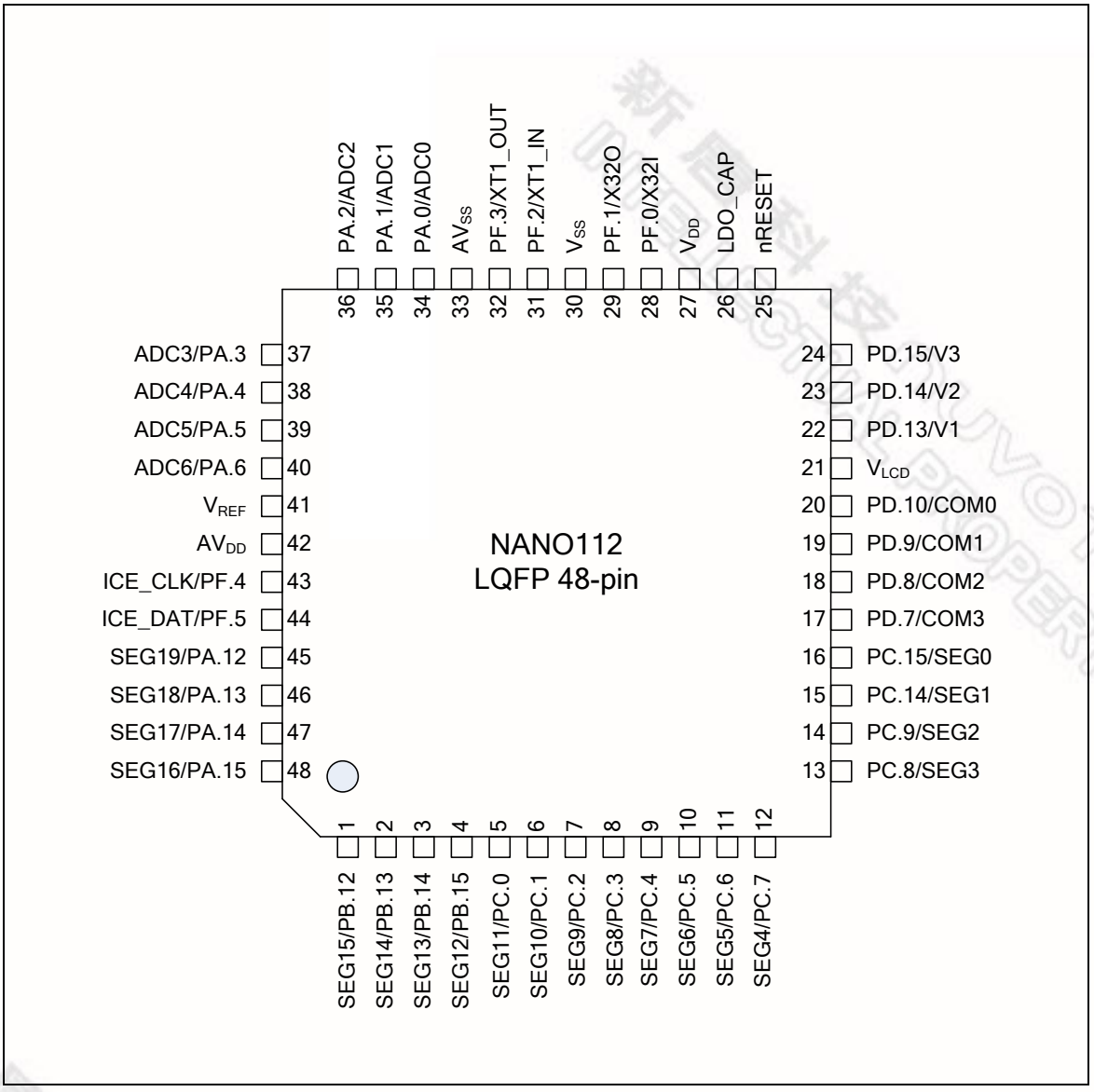


Figure 4-7 NuMicro™ Nano112 LQFP 48-pin Diagram

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			PWM0_CH1	I/O	PWM0 Channel1 output
9	7		PC.2	I/O	General purpose digital I/O pin
			I2C1_SCL	O	I^2C1 clock pin
			PWM0_CH2	I/O	PWM0 Channel2 output
10	8		PC.3	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output
11	9	5	PC.4	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
12	10		PC.5	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
13	11	6	PC.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SC0_DAT	I/O	SmartCard0 DATA pin (SC0_UART_RXD)
14	12	7	PC.7	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_PWR	O	SmartCard0 Power pin
15	13	8	PC.8	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	O	SmartCard0 RST pin
16	14		PC.9	I/O	General purpose digital I/O pin
		9	PC.10	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I^2C1 clock pin
			SC1_CD	I	SmartCard1 card detect
		10	PC.11	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C 1 data I/O pin
			SC1_PWR	O	SmartCard1 PWR pin
		11	PC.12	I/O	General purpose digital I/O pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG12	**O**	LCD segment output 12 at 64-pin
			LCD_SEG5	**O**	LCD segment output 5 at 48-pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin (SC0_UART_RXD)
20	14	12	PC.7	**I/O**	General purpose digital I/O pin
			LCD_SEG15	**O**	LCD segment output 15 at 100-pin
			LCD_SEG11	**O**	LCD segment output 11 at 64-pin
			LCD_SEG4	**O**	LCD segment output 4 at 48-pin
			UART1_RXD	**I**	UART1 Data receiver input pin
			SC0_PWR	**O**	SmartCard0 Power pin
21	15	13	PC.8	**I/O**	General purpose digital I/O pin
			LCD_SEG14	**O**	LCD segment output 14 at 100-pin
			LCD_SEG10	**O**	LCD segment output 10 at 64-pin
			LCD_SEG3	**O**	LCD segment output 3 at 48-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	**O**	SmartCard0 RST pin
22	16	14	PC.9	**I/O**	General purpose digital I/O pin
			LCD_SEG13	**O**	LCD segment output 13 at 100-pin
			LCD_SEG9	**O**	LCD segment output 9 at 64-pin
			LCD_SEG2	**O**	LCD segment output 2 at 48-pin
23			V_{DD}	**P**	Power supply for I/O ports and LDO source
24			V_{SS}	**G**	Ground for digital circuit
25			V_{SS}	**G**	Ground for digital circuit
26			PC.10	**I/O**	General purpose digital I/O pin
			LCD_SEG12	**O**	LCD segment output 12 at 100-pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
			SC1_CD	**I**	SmartCard1 card detect pin
27			PC.11	**I/O**	General purpose digital I/O pin
			LCD_SEG11	**O**	LCD segment output 11 at 100-pin
			I2C1_SDA	**I/O**	I^2C 1 data I/O pin
			SC1_PWR	**O**	SmartCard1 PWR pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			TC0	**I**	Timer0 capture input
44	31		PD.12	**I/O**	General purpose digital I/O pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 100-pin
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			TM1	**I/O**	Timer1 external counter input
			FCLK0	**O**	Frequency Divider0 output pin
45					NC
46	32	21	V_{LCD}	**P**	LCD power supply pin
47					NC
48	33	22	PD.13	**I/O**	General purpose digital I/O pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 100-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 64-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 48-pin
			INT1	**I**	External interrupt 1 input pin
49	34	23	PD.14	**I/O**	General purpose digital I/O pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 100-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 64-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 48-pin
50	35	24	PD.15	**I/O**	General purpose digital I/O pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 100-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 64-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 48-pin

6.5 Clock Controller

6.5.1 Overview

The clock controller generates clocks for the whole chip, Iincluding system clocks (CPU clock, HCLKx, and PCLKx) and all peripheral module clocks. HCLKx means AHB bus clock for peripherals on AHB bus. PCLKx means APB bus clock for peripherals on APB bus. PCLKx can be the same as HCLKx or devided from HCLKx. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a 4-bit clock divider. The chip will not enter power-down mode until CPU sets the power down enable bit PD_EN(PWRCTL[6]) and executes the WFI instruction. In the Power-down mode, clock controller turns off the external high frequency crystal, internal high frequency oscillator, and system clocks (CPU clock, HCLKx, and PCLKx) to reduce the power consumption.

The clock controller consists of 5 sources as listed below:

- 32768Hz external low speed crystal oscillator (LXT)
- 4~ 24 MHz external high speed crystal oscillator (HXT)
- 12/16 MHz internal high speed RC oscillator (HIRC)
- One programmable PLL FOUT (PLL source can be selected from HXT or HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

6.5.2 Features

- Generates clocks for system clocks and all peripheral module clocks.
- Each peripheral module clock can be turned on/off.
- High frequency crystal, internal high frequency oscillator, and system clocks will be turned off when chip is in Power-down mode.

6.6 Flash Memory Controller (FMC)

6.6.1 Overview

This chip is equipped with 16/32 Kbytes on-chip embedded flash memory for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides Data Flash Region, the Data Flash is shared with original program memory and its start address is configurable and defined by user in Config1. The Data Flash size is defined by user application request.

6.6.2 Features

- 16/32 Kbytes application program memory (APROM)
- 4 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable Data Flash start address and memory size with 512 bytes page erase unit
- 512 bytes system program memory (SPROM)
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.7 General Purpose I/O Controller

6.7.1 Overview

The NuMicro Nano112™ series have up to 80 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 80 pins are arranged in 6 ports named with GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, and open-drain mode. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for V_{DD} from 1.8 V to 3.6 V.

6.7.2 Features

- Three I/O modes:
  - Schmitt trigger Input-only with high impendence
  - Push-pull output
  - Open-drain output
- I/O pin configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the pin wake-up function

6.16 I²C

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up to 1 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte.

A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.

The controller's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C controller handles byte transfers autonomously. Pull up resistor is needed for I²C operation as these are open drain pins.

The I²C controller is equipped with two slave address registers. The contents of the registers are irrelevant when I²C is in Master mode. In the Slave mode, the seven most significant bits must be loaded with the user's own slave address. The I²C hardware will react if the contents of I2CADDR are matched with the received slave address.

This controller supports the "General Call (GC)" function. If the GCALL (I2CSADDR[0]) bit is set this controller will respond to General Call address (00H). Clear GC bit to disable general call function. When GCALL bit is set and the I²C is in Slave mode, it can receive the general call address which is equal to 00H after master sends general call address to the I²C bus, then it will follow status of GC mode. If it is in Master mode, the ACK bit must be cleared when it sends general call address of 00H to the I²C bus.

The I²C-bus controller supports multiple address recognition with two address mask register. When the bit in the address mask register is set to one, it means the received corresponding address bit is don't-care. If the bit is set to 0, that means the received corresponding register bit should be exact the same as address register.

6.16.2 Features

- Supports two I2C channels and both of them can acts as Master or Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- One built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clock divider allows versatile rate control
- Supports 7-bit addressing mode

6.18 LCD Display Driver

6.18.1 Overview

The LCD driver can directly drive a LCD glass by creating the ac segment and common voltage signals automatically. It can support static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty LCD glass with up to 3 segments with 6 COM (segment 0 is used as LCD_COM4 and segment 1 is used as LCD_COM5) or 36 segments with 4 COM (LCD_COM0 ~ LCD_COM3).

A built-in charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage. The LCD driver would generate voltage higher than the threshold voltage in older to darken a segment and a voltage lower than threshold to make a segment clear. However, the LCD display segment will degrade if the applied voltage has a DC-component. To avoid this, the generated waveform by LCD driver are arranged such that average voltage of each segment is 0 and the RMS(root-mean-square) voltage applied on a LCD segment lower than the segment threshold making LCD clear and RMS voltage higher than the segment threshold making LCD dark.

6.18.2 Features

- Supports Segment/Com:
  - 108 dots (6x18) or 80 dots (4x20) in LQFP48 package
  - 108 dots (6x18) or 80 dots (4x20) or 132 dots (6x 22) or 96 dots (4x24) or 180 dots (6x30) or 128 dots (4x32) in LQFP64 package
  - 204 dots (6x34) or 144 dots (4x36) in LQFP100 package
- Common 0-5 multiplexing functions with GPI/O pins
- Segment 0-35 multiplexing function with GPI/O pins
- Supports Static,1/2 bias and 1/3 bias voltage
- Six display modes: Static,1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty or 1/6 duty Selectable LCD frequency by frequency divider
- Configurable frame frequency
- Internal Charge pump, adjustable contrast adjustment
- Embedded LCD bias reference ladder (R-Type, 200/300/400 kΩ resisters)
- Configurable Charge pump frequency
- Blinking capability
- Supports R/C/Ext_C-type method
- LCD frame interrupt

6.19 Analog to Digital Converter (ADC)

6.19.1 Overview

The Nano112 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 external input channels and 4 internal channels. The A/D converter supports three operation modes: Single, Single-cycle Scan and Continuous Scan mode, and can be started by software, external STADC(PA.11) pin, timer event start and PWM trigger.

Note that the I/O pins used as ADC analog input pins must configure the Pin Function (PA_L_MFP) to ADC input and off digital function (GPIOA_OFFD) should be turned on before ADC function is enabled.

6.19.2 Features

- Analog input voltage range: 0~V_{REF} (Max to AV_{DD})
- Selectable 12-bits, 10-bits, 8-bits and 6-bits resolution
- Supports sampling time settings for channel 0~7 individually (ADCCHSAMP0 register) and channel 14~17 share the same one sampling time setting (ADCCHSAMP1 register)
- Supports two power-down modes:
  - Power-down mode
  - Standby mode
- Up to 8 external analog input channels (channel0 ~ channel7), and 4 internal channels (channel14~channel17) converting four voltage sources (internal band-gap voltage, internal temperature sensor output, AV_{DD}, and AV_{SS}).
- Maximum ADC clock frequency is 32 MHz and each conversion is 19 clocks+ sampling time depending on the input resistance (Rin).
- Three operating modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger
  - Selects one from four timer events (TMR0, TMR1, TMR2 and TMR3) that enable ADC and transfer AD results by PDMA
- Conversion results held in data registers for each channel
- Supports digital comparator: Conversion result can be compared with a specified value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting.
- Supports Calibration and load Calibration words capability.

9.2 Nano102/Nano112 DC Electrical Characteristics

(VDD-VSS=3.3V, TA = 25°C, FOSC = 32 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	1.8	-	3.6	V	V_{DD} =1.8V up to 32 MHz
Power Ground	V_{SS} AV_{SS}	-0.3	-		V	
LDO Output Voltage	V_{LDO1}	1.62	1.8	1.98	V	MCU operating in Run or Idle mode
		1.44	1.6	1.76	V	Set LDO_LEVEL(LDO_CTL[3:2]) = 0x1
	V_{LDO2}	1.49	1.66	1.83	V	MCU operating in Power-down mode
	C_{LDO}		1		uF	Connect to LDO_CAP pin
Analog Operating Voltage	AV_{DD}		V_{DD}		V	
Operating Current Normal Run Mode HCLK =32 MHz wkhile(1){}executed from flash V_{LDO1}=1.8 V	I_{DD5}		11.7		mA	V_{DD}: 3.3 V; HXT: 12 MHz; HIRC: X; PLL: V; All digital module: V
	I_{DD6}		5.8		mA	3.3 V; 12 MHz; X; V; X
	I_{DD7}		10.9		mA	1.8 V; 12 MHz; X; V; V
	I_{DD8}		5.6		mA	1.8 V; 12 MHz; X; V; X
Operating Current Normal Run Mode HCLK =32 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD9}		3.9		mA	3.3 V; 12 MHz; X; X; V
	I_{DD10}		1.9		mA	3.3 V; 12 MHz; X; X; X
	I_{DD11}		3.8		mA	1.8 V; 12 MHz; X; X; V
	I_{DD12}		1.9		mA	1.8 V; 12 MHz; ; ;

9.3.4 Internal 12 MHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{HRC}		1.8		V	
Calibrated Internal Oscillator Frequency	F_{HRC}	11.88	12	12.12	MHz	25°C, VDD = 3.3V
		11.76	12	12.24	MHz	-40°C ~ +85°C, VDD = 1.8V~3.6V
		11.88	12	12.12	MHz	-40°C ~ +85 °C, VDD = 1.8V~3.6V Enable 32.768K crystal oscillator and set TRIM_SEL[1:0]=”10”
Operating current	I_{HRC}		250		μA	

Note: Internal oscillator operation voltage comes from LDO.

9.3.5 Internal 10 kHz Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Supply voltage[1]	V_{LRC}		1.8		V	
Center Frequency	F_{LRC}	7	10	13	kHz	25°C, VDD = 3V
		5	10	15	kHz	-40°C ~+85 °C, VDD = 1.8V~3.6V
Operating current	I_{LRC}		0.3		μA	VDD = 3V

Note: Internal oscillator operation voltage comes from LDO.

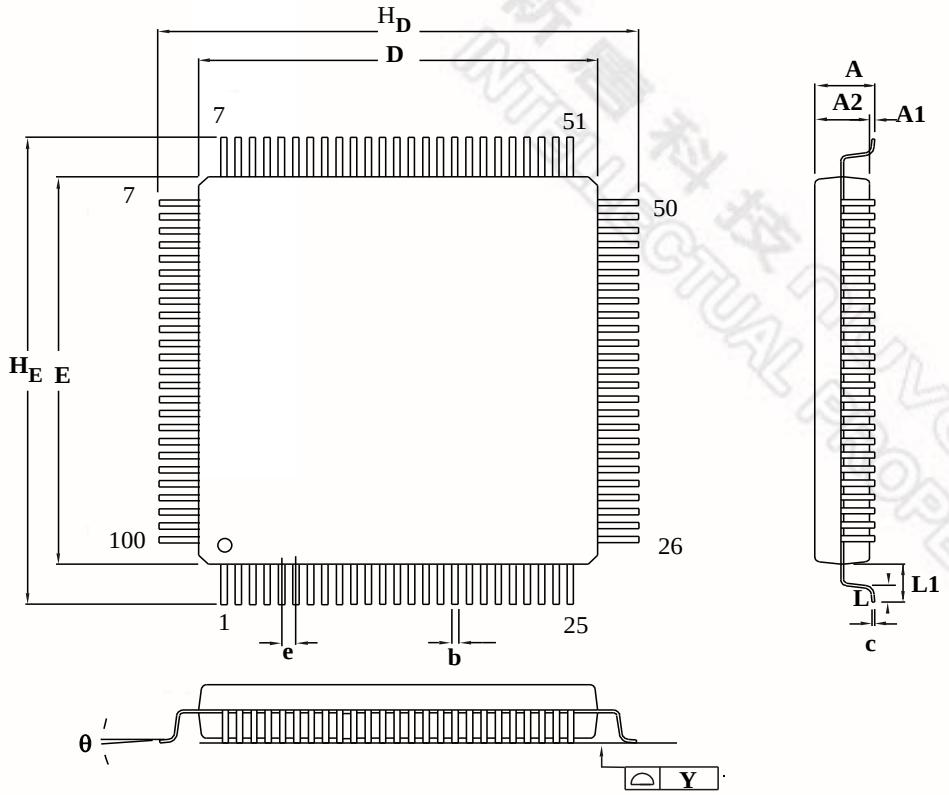
9.4 Analog Characteristics

9.4.1 12-bit ADC

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8		3.6	V	$AV_{DD} = V_{DD}$
Operating current (AV_{DD} current) (Enable ADC and disable all	I_{ADC32}		120		μA	$AV_{DD} = V_{DD}$ = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 32 MHz

10 PACKAGE DIMENSIONS

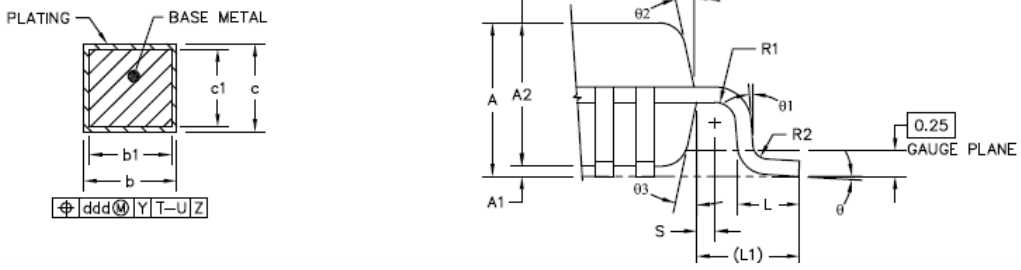
10.1 100L LQFP (14x14x1.4 mm footprint 2.0 mm)



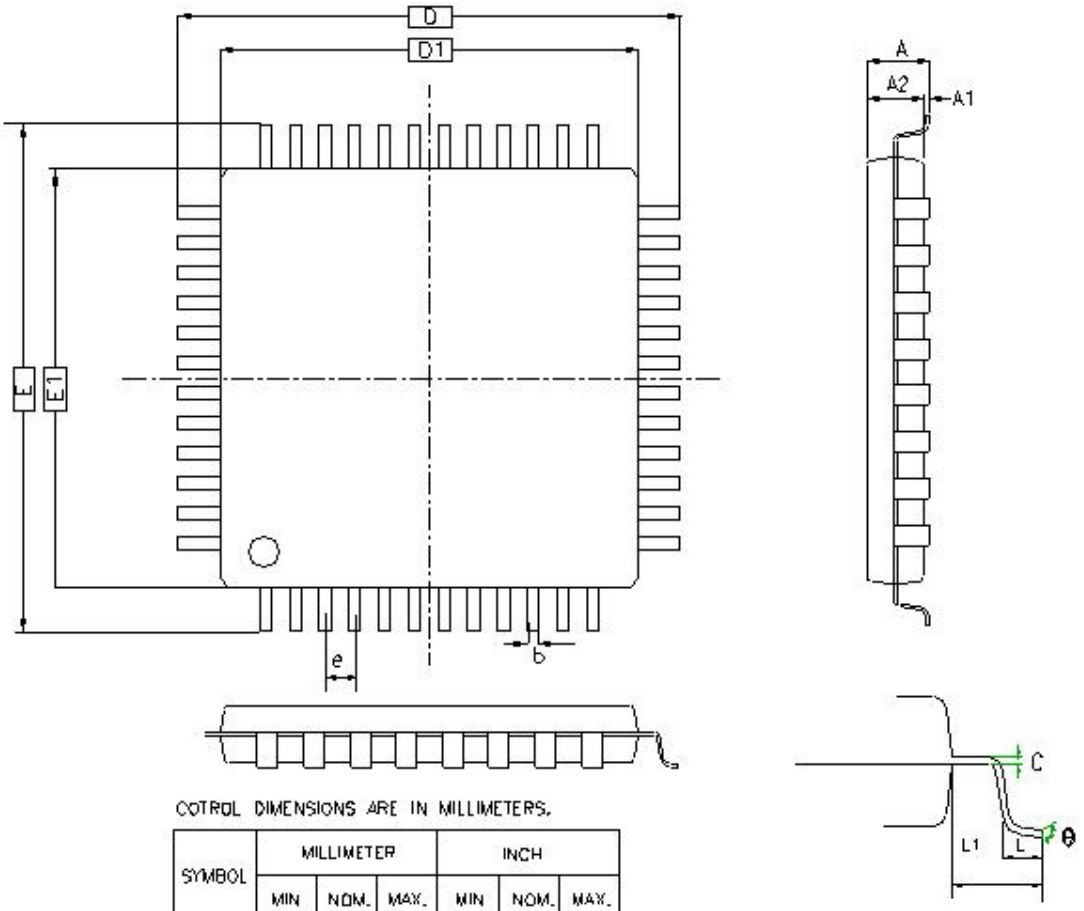
Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



10.4 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

11 REVISION HISTORY

Date	Revision	Description
2014.03.28	1.00	1. Initial release
2014.05.08	1.01	1. Modified some typos and format.
2014.09.02	1.02	1. Modified the pin description for LCD_Vx in section 4.4. 2. Modified all PWM1 group to PWM0 group in section 6.10. 3. Modified “PWM1 channel 2 and 3” to “PWM0 channel 2 and 3” in section 6.10. 4. Modified some typos and format.
2015.01.15	1.03	1. Updated ADC channel number in NANO102 feature list in Chapter 2. 2. Corrected typo in NANO102 64-pin sequence in section 4.4. 3. Updated all power related pins from “VDD, VSS, AVDD, AVSS, VTEMP and VLCD” to “V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, V_{TEMP} and V_{LCD}” in the Datashhet.