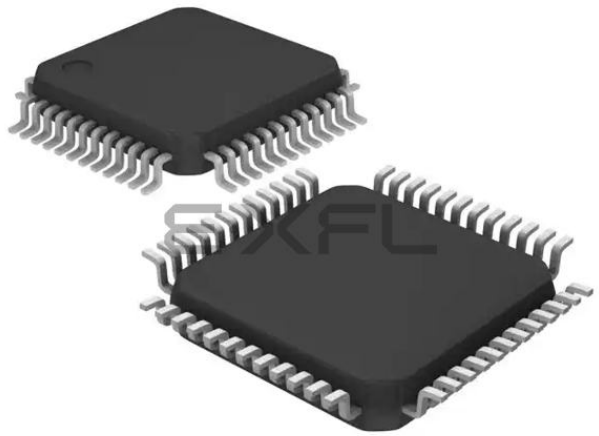
Nuvoton Technology Corporation - NANO112LB1AN Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112lb1an

Table of Contents

Product Line	UART	SPI	I^2C	ADC	ACMP	RTC	SC	Timer	LCD
Nano102	●	●	●	●	●	●	●	●	
Nano112	●	●	●	●	●	●	●	●	●

Table 1-1 Connectivity Support Table

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano102 Features – Base Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access
  - 16/32 Kbytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 5 channels: 4 PDMA channels and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out

- Threshold voltage detection (comparator function)
- Conversion started by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1℃ resolution
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is as the master, and 1 slave/device select line when SPI controller is as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up (SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C devices
  - Master/Slave up to 1Mbit/s
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requestING the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allow versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave address with mask option)
  - Wake system up (address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 7-ch single-ended input from external pin (PA.0 ~ PA.6)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Single scan/single cycle scan/continuous scan
  - Each channel with individual result register
  - Only scan on enabled channels
  - Threshold voltage detection (comparator function)
  - Conversion start by software programming or external input
  - Supports PDMA mode
  - Supports up to four timer time-out events (TMR0, TMR1, TMR2, and TMR3) to

- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(10x10) / 64-pin(7x7) / 48-pin(7x7)

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro™ Nano102/112 Series Selection Code

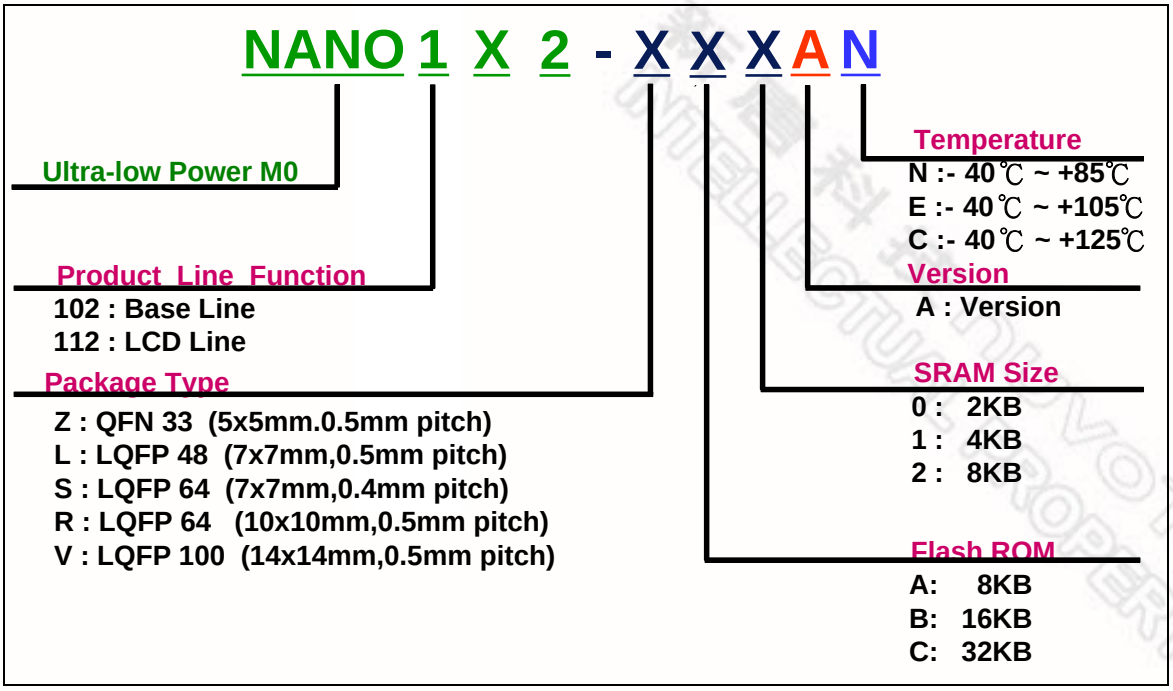

Figure 4-1 NuMicro™ Nano112 Series Selection Code

4.2 NuMicro™ Nano112 Products Selection Guide

4.2.1 NuMicro™ Nano102 Base Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	I/O	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10 kHz / 12 MHz / 16 MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I²C											
NANO102ZB1AN	16K	4K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102ZC2AN	32K	8K	Configurable	4K	up to 27	4	3	2	2	2	4	2	√	√	4	-	1	√	QFN33	-40 to +85
NANO102LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP48	-40 to +85
NANO102SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	-	2	√	LQFP64*	-40 to +85

QFN33: 5x5mm
LQFP48: 7x7mm
LQFP64*: 7x7mm

4.3.1.2 NuMicro™ Nano102 LQFP 48-pin

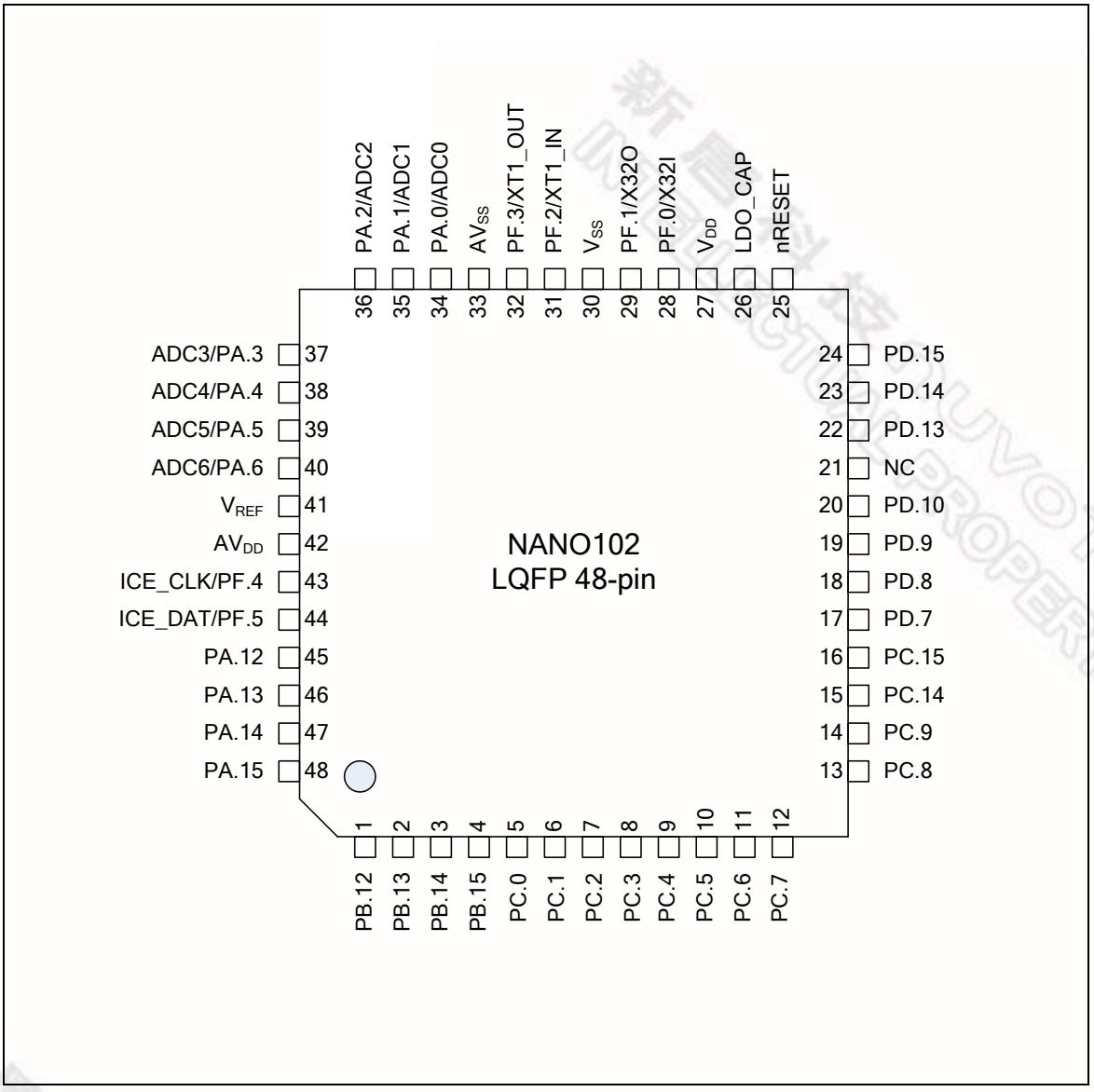

Figure 4-3 NuMicro™ Nano102 LQFP 48-pin Diagram

4.3.2.2 NuMicro™ Nano112 LQFP 64-pin

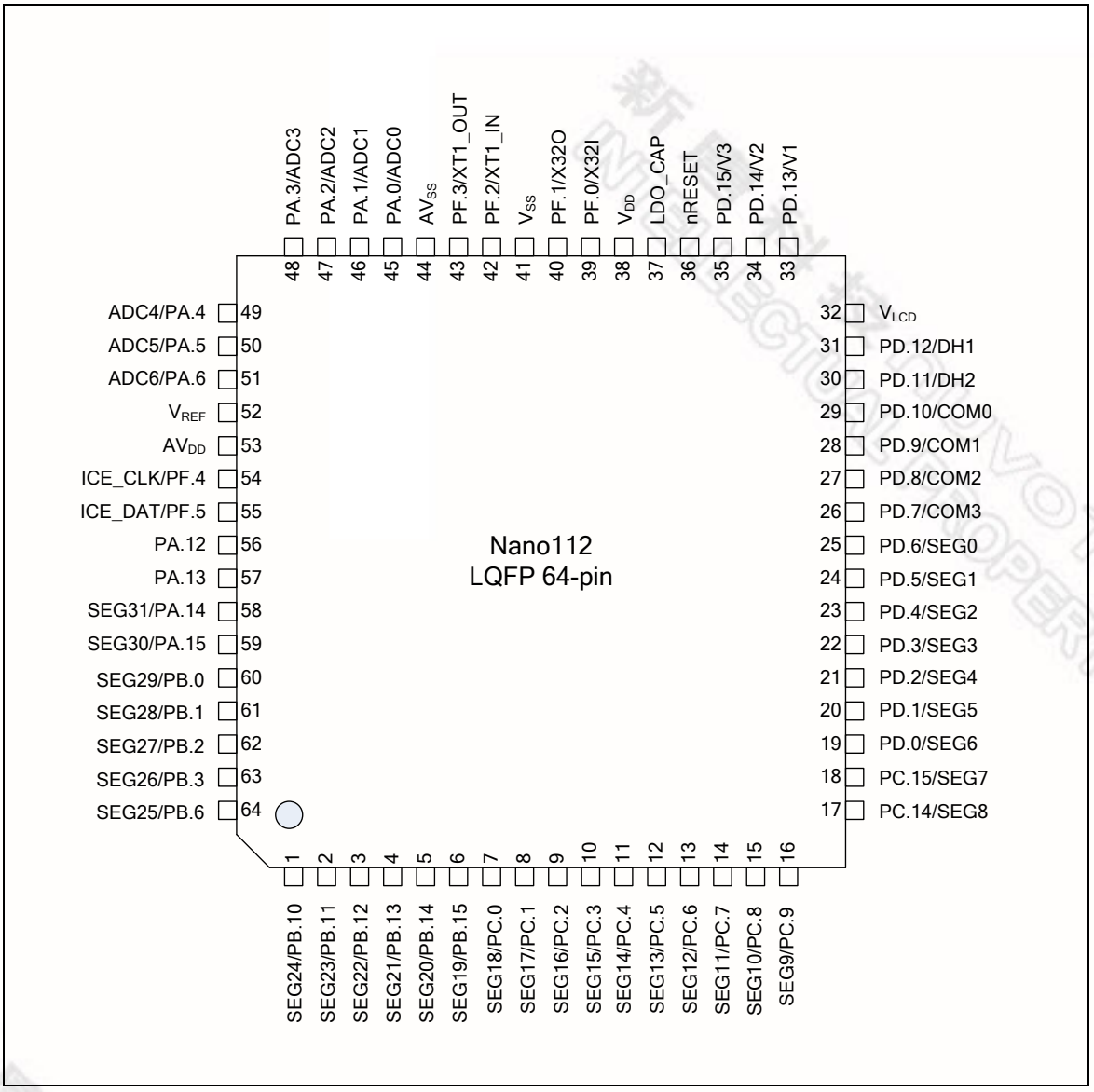

Figure 4-6 NuMicro™ Nano112 LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG26	O	LCD segment output 26 at 100-pin
			LCD_SEG22	O	LCD segment output 22 at 64-pin
			LCD_SEG15	O	LCD segment output 15 at 48-pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			FCLK0	O	Frequency Divider0 output pin
9	4	2	PB.13	I/O	General purpose digital I/O pin
			LCD_SEG25	O	LCD segment output 25 at 100-pin
			LCD_SEG21	O	LCD segment output 21 at 64-pin
			LCD_SEG14	O	LCD segment output 14 at 48-pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
10	5	3	PB.14	I/O	General purpose digital I/O pin
			LCD_SEG24	O	LCD segment output 24 at 100-pin
			LCD_SEG20	O	LCD segment output 20 at 64-pin
			LCD_SEG13	O	LCD segment output 13 at 48-pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI0_CLK	I/O	SPI0 serial clock pin
11			NC		
12	6	4	PB.15	I/O	General purpose digital I/O pin
			LCD_SEG23	O	LCD segment output 23 at 100-pin
			LCD_SEG19	O	LCD segment output 19 at 64-pin
			LCD_SEG12	O	LCD segment output 12 at 48-pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI0_SS0	I/O	SPI0 1st slave select pin
13	7	5	PC.0	I/O	General purpose digital I/O pin
			LCD_SEG22	O	LCD segment output 24 at 100-pin
			LCD_SEG18	O	LCD segment output 18 at 64-pin
			LCD_SEG11	O	LCD segment output 11 at 48-pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			I2C0_SCL	I/O	I^2C0 clock pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			TC0	**I**	Timer0 capture input
44	31		PD.12	**I/O**	General purpose digital I/O pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 100-pin
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			TM1	**I/O**	Timer1 external counter input
			FCLK0	**O**	Frequency Divider0 output pin
45					NC
46	32	21	V_{LCD}	**P**	LCD power supply pin
47					NC
48	33	22	PD.13	**I/O**	General purpose digital I/O pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 100-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 64-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 48-pin
			INT1	**I**	External interrupt 1 input pin
49	34	23	PD.14	**I/O**	General purpose digital I/O pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 100-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 64-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 48-pin
50	35	24	PD.15	**I/O**	General purpose digital I/O pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 100-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 64-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 48-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
51	35	25	nRESET		External reset input: low active. Setting this pin low will reset chip to initial state. With internal pull-up.
52	37	26	LDO_CAP	**P**	LDO capacitor pin
53	38	27	V_{DD}	**P**	Power supply for I/O ports and LDO source
54	38	28	PF.0	**I/O**	General purpose digital I/O pin
			X32I	**I**	External 32.768 kHz crystal input pin(default)
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
55	40	29	PF.1	**I/O**	General purpose digital I/O pin
			X32O	**O**	External 32.768 kHz crystal output pin(default)
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
56			V_{SS_PLL}	**G**	Ground for PLL
57	41	30	V_{SS}	**G**	Ground for digital circuit
58			V_{SS}	**G**	Ground for digital circuit
59	42	31	PF.2	**I/O**	General purpose digital I/O pin
			XT1_IN	**AI**	External 4~24 MHz crystal input pin(default)
			UART1_RXD	**I**	UART1 Data receiver input pin
			TC3	**I**	Timer3 capture input
			INT1	**I**	External interrupt1 input pin
60	43	32	PF.3	**I/O**	General purpose digital I/O pin
			XT1_OUT	**AO**	External 4~24 MHz crystal output pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			TC2	**I**	Timer 2 capture input
			INT0	**I**	External interrupt0 input pin
61					NC
62			PE.0	**I/O**	General purpose digital I/O pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
63			PE.1	**I/O**	General purpose digital I/O pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
64			PE.2	**I/O**	General purpose digital I/O pin

5 BLOCK DIAGRAM

5.1 Nano102 Block Diagram

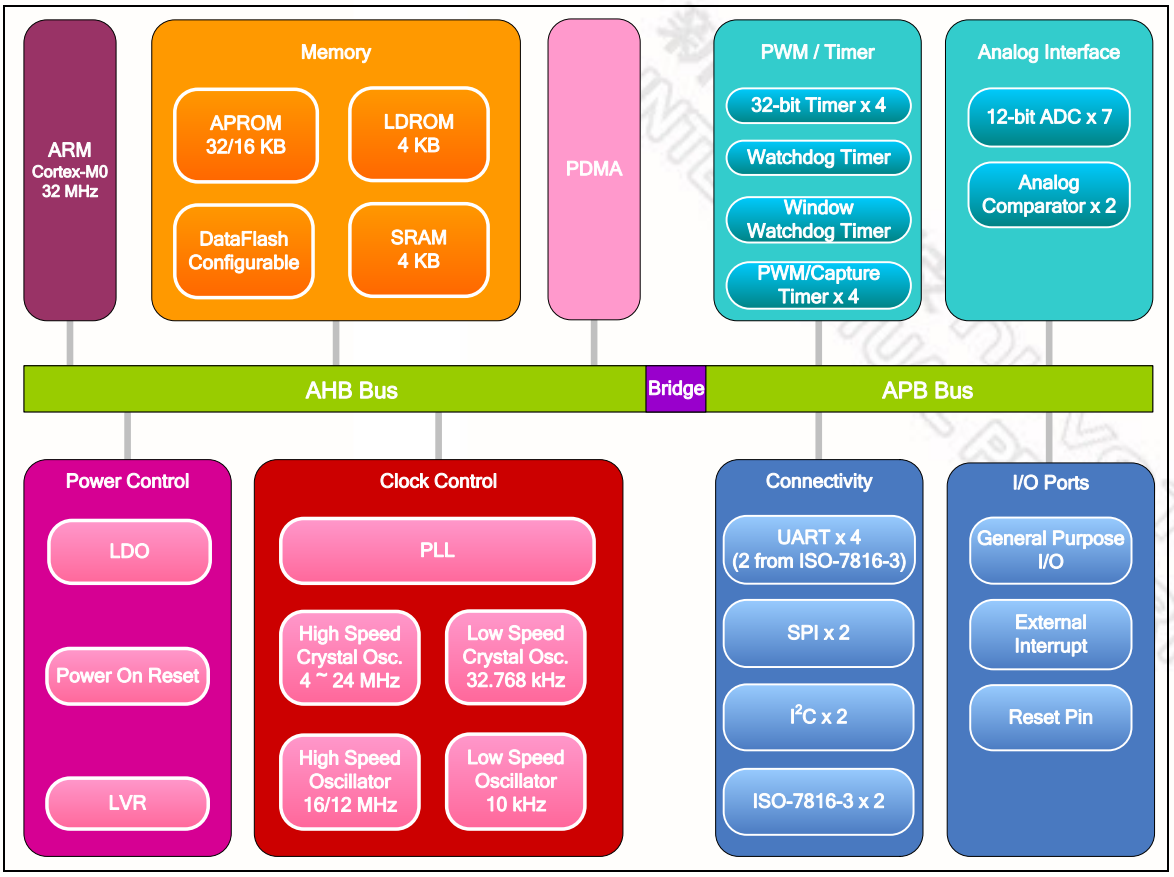

Figure 5-1 NuMicro™ Nano102 Block Diagram

- Supports multiple address recognition (Two slave addresses with mask option)
- Supports Power-down wake-up function
- Supports two-Level FIFO

8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU clock	Current
Nano102/112 series	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.89mA 157uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	800uA 67uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.65mA 137uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	560uA 46uA/MHz
	RTC + LCD Mode: (RAM retention) (Power down with LXT and LCD enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC and LCD circuit. Without panel loading Set LDO output = 1.6V Only for Nano112 LCD series	InternL C-Type (With internal Charge pump)	3.3V	Stop	9.5uA
		InternL R-Type (With internal resistor ladder) 200kΩ			8.3uA
		InternL R-Type (With internal resistor ladder) 300kΩ			6.4uA
		InternL R-Type (With internal resistor ladder) 400kΩ			5.5uA
		External C-Type (With 0.1uF cap. ladder)			2.5uA
		External R-type (With 1MΩ resister ladder)			3.7uA
	RTC Mode: (RAM retention) (Power down with LXT enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC circuit Set LDO output = 1.6V		3.3V	Stop	1.5uA
	Power Down Mode: (RAM retention) CPU and all clocks stop Set LDO output = 1.6V		3.3V	Stop	0.65uA
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from wake-up event to first CPU core valid clock)		3.3V	12 MHz	6us
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from interrupt event to interrupt service routine first instruction)		3.3V	12 MHz	7us

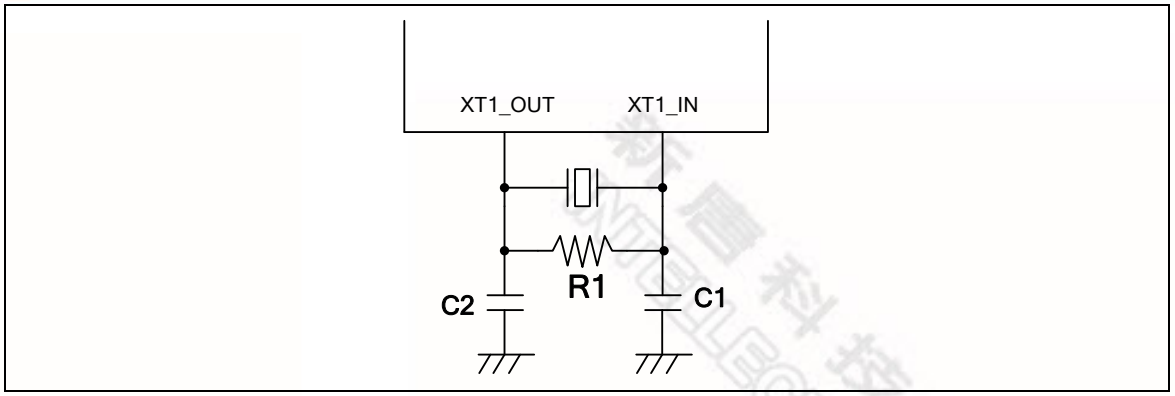

Figure 9-1 Typical Crystal Application Circuit

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1		μA	VDD = 3.0V

9.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

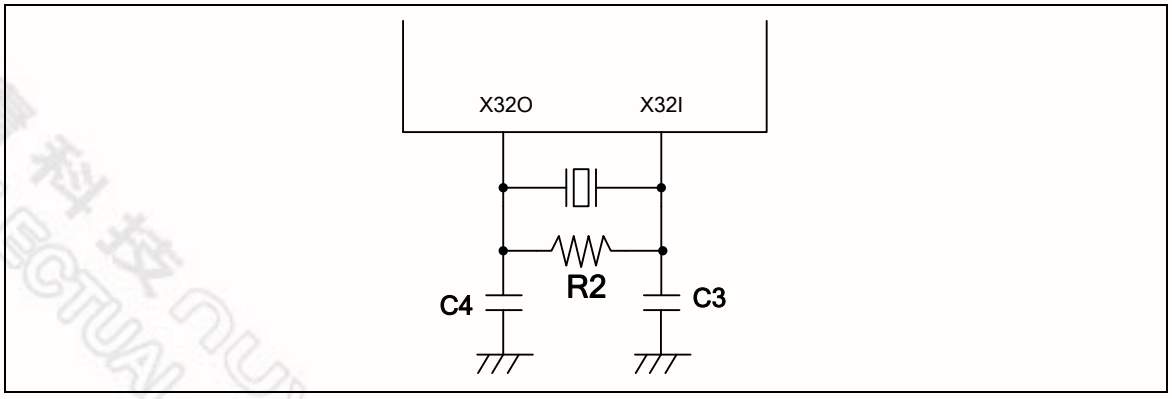

Figure 9-2 Typical Crystal Application Circuit

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
	$I_{LCDintR}$		8.3		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 200KΩ resistor ladder)
			6.4		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 300KΩ resistor ladder)
			5.5		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal R type with internal 400KΩ resistor ladder)
	$I_{LCDextR}$		3.7		μA	V_{DD} = 3V, frame rate = 64Hz Without loading (external R type with external 1MΩ resistor ladder)

9.4.6 Internal Voltage Reference

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	AV_{DD}	1.8	-	3.6	V	
1.5V voltage reference	V_{REF1}	1.44	1.5	1.56	V	AV_{DD} ≥ 1.8V (-40°C ~85°C)
1.8V voltage reference	V_{REF2}	1.69	1.8	1.87	V	AV_{DD} ≥ 2.0V (-40°C ~85°C)
2.5V voltage reference	V_{REF3}	2.35	2.5	2.60	V	AV_{DD} ≥ 2.8V (-40°C ~85°C)
Stable Time	T_{REFTAB}	-	1	-	ms	
Operating current	I_{VREF}	-	30	-	μA	AV_{DD} = 3V

9.4.7 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	1.8		3.6	V	
T_A	Temperature	-40	25	85	℃	-
I_{CMP}	Operation Current	-	40		μA	AV_{DD} = 3 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-

V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain	40	70	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{DIFF} = 100mV
V_{HYS}	Hysteresis	-	±10	-	mV	
T_{STB}	Stable time	-	-	1	µs	

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	