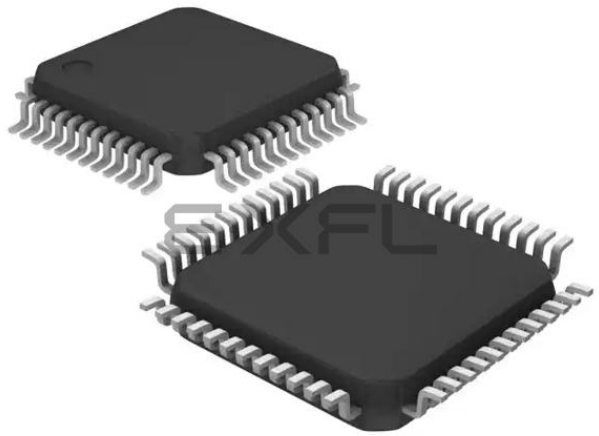


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112lc2an

LIST OF TABLES

- Wake system up from Power-down mode

- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output

- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports One-shot and Continuous mode
  - Supports Capture interrupt

- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control.
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system (CTSn, received data or RS-485 address matched) up from Power-down mode

- SPI

- Threshold voltage detection (comparator function)
- Conversion started by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1℃ resolution
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

- CRC-8: $X^8 + X^2 + X + 1$
- CRC-16: $X^{16} + X^{15} + X^2 + 1$
- CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, P.0(X32I), PF.1(X32O)
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible

4.3.1.2 NuMicro™ Nano102 LQFP 48-pin

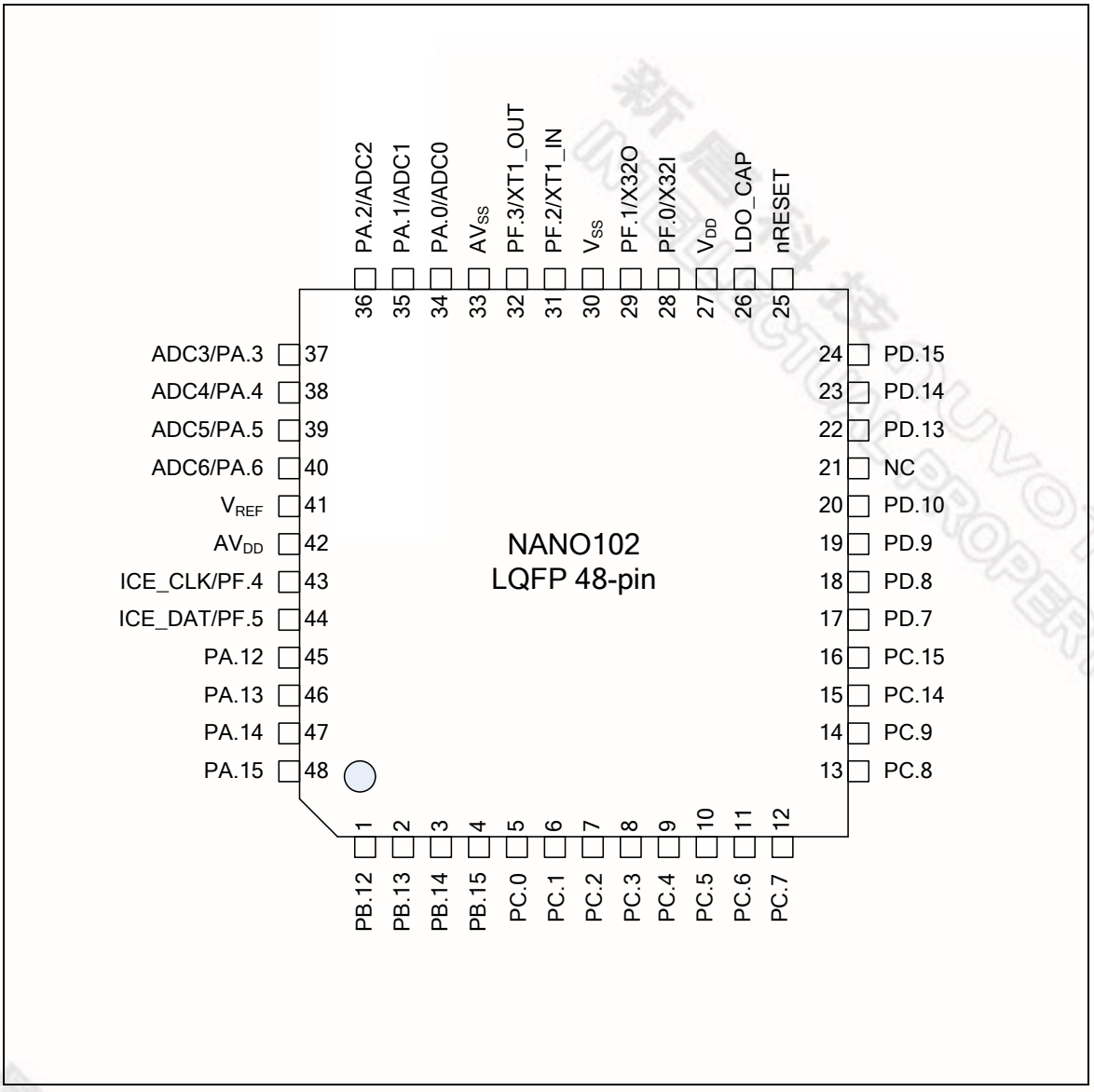


Figure 4-3 NuMicro™ Nano102 LQFP 48-pin Diagram

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			I2C1_SDA	I/O	I^2C1 data I/O pin
			TC3	I	Timer3 capture input
			ACMP1_OUT	O	Comparator1 output
60			PB.0	I/O	General purpose digital I/O pin
			UART0_TXD	O	UART0 Data transmitter output pin(This pin could modulate with PWM0 output)
			FCLK1	O	Frequency Divider1 output pin
61			PB.1	I/O	General purpose digital I/O pin
			UART0_RXD	I	UART0 Data receiver input pin
			TC2	I	Timer 2 capture input
			INT1	I	External interrupt1 input pin
62			PB.2	I/O	General purpose digital I/O pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI1_MOSI1	I/O	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	I/O	I^2C0 clock pin
			TM3	I/O	Timer3 external counter input or Timer3 toggle out.
63			PB.3	I/O	General purpose digital I/O pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI1_MISO1	I/O	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	I/O	I^2C0 data I/O pin
			TM2	I/O	Timer2 external counter input or Timer2 toggle out.
64			PB.6	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_SS1	I/O	SPI1 2nd slave select pin
			FCLK0	O	Frequency Divider0 output pin

Note: Pin Type: I = Digital Input, O = Digital Output; AI = Analog Input; AO = Analog Output; P = Power Pin; AP = Analog Power.

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
28			PC.12	I/O	General purpose digital I/O pin
			LCD_SEG10	O	LCD segment output 10 at 100-pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)
29			PC.13	I/O	General purpose digital I/O pin
			LCD_SEG9	O	LCD segment output 9 at 100-pin
			SC1_DAT	I/O	SmartCard1 DATA pin (SC1_UART_RXD)
30	17	15	PC.14	I/O	General purpose digital I/O pin
			LCD_SEG8	O	LCD segment output 8 at 100-pin
			LCD_SEG8	O	LCD segment output 8 at 64-pin
			LCD_SEG1	O	LCD segment output 1 at 48-pin
			SC1_CD	I	SmartCard1 card detect
31	18	16	PC.15	I/O	General purpose digital I/O pin
			LCD_SEG7	O	LCD segment output 7 at 100-pin
			LCD_SEG7	O	LCD segment output 7 at 64-pin
			LCD_SEG0	O	LCD segment output 0 at 48-pin
			SC1_PWR	O	SmartCard1 PWR pin
32	19		PD.0	I/O	General purpose digital I/O pin
			LCD_SEG6	O	LCD segment output 6 at 100-pin
			LCD_SEG6	O	LCD segment output 6 at 64-pin
33	20		PD.1	I/O	General purpose digital I/O pin
			LCD_SEG5	O	LCD segment output 5 at 100-pin
			LCD_SEG5	O	LCD segment output 5 at 64-pin
34	21		PD.2	I/O	General purpose digital I/O pin
			LCD_SEG4	O	LCD segment output 4 at 100-pin
			LCD_SEG4	O	LCD segment output 4 at 64-pin
35	22		PD.3	I/O	General purpose digital I/O pin
			LCD_SEG3	O	LCD segment output 3 at 100-pin
			LCD_SEG3	O	LCD segment output 3 at 64-pin
36	23		PD.4	I/O	General purpose digital I/O pin
			LCD_SEG2	O	LCD segment output 2 at 100-pin
			LCD_SEG2	O	LCD segment output 2 at 64-pin
			SC1_RST	O	SmartCard1 RST pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			TC0	**I**	Timer0 capture input
44	31		PD.12	**I/O**	General purpose digital I/O pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 100-pin
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			TM1	**I/O**	Timer1 external counter input
			FCLK0	**O**	Frequency Divider0 output pin
45					NC
46	32	21	V_{LCD}	**P**	LCD power supply pin
47					NC
48	33	22	PD.13	**I/O**	General purpose digital I/O pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 100-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 64-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 48-pin
			INT1	**I**	External interrupt 1 input pin
49	34	23	PD.14	**I/O**	General purpose digital I/O pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 100-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 64-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 48-pin
50	35	24	PD.15	**I/O**	General purpose digital I/O pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 100-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 64-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 48-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
76	49	38	PA.4	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_CD	**I**	SmartCard0 card detect pin
			ACMP0_P0	**AI**	Comparator0 P-end input0
			AD4	**AI**	ADC analog input4
77	50	39	PA.5	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
			ACMP0_N	**AI**	Comparator0 N-end input0
			AD5	**AI**	ADC analog input5
78	51	40	PA.6	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_RST	**O**	SmartCard0 RST pin
			ACMP0_OUT	**O**	Comparator0 output
			AD6	**AI**	ADC analog input6
79			PA.7	**I/O**	General purpose digital I/O pin
			SC1_CD	**I**	SmartCard1 card detect
			AD7	**AI**	ADC analog input7
80	52	41	V_{REF}	**A**	ADC/Comparator reference voltage
81	53	42	AV_{DD}	**P**	Power supply for ADC and comparators
82	54	43	PF.4	**I/O**	General purpose digital I/O pin
			ICE_CLK	**I**	Serial Wired Debugger Clock pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			PWM0_CH2	**O**	PWM0 Channel2 output
			TC1	**I**	Timer1 capture input
			FCLK1	**O**	Frequency Divider1 output pin
83	55	44	PF.5	**I/O**	General purpose digital I/O pin
			ICE_DAT	**I/O**	Serial Wired Debugger Data pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			PWM0_CH3	**I/O**	PWM0 Channel3 output
			TC0	**I**	Timer0 capture input

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
84			PA.8	**I/O**	General purpose digital I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
85			PA.9	**I/O**	General purpose digital I/O pin
			SC0_RST	**O**	SmartCard0 RST pin
86			PA.10	**I/O**	General purpose digital I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
87			PA.11	**I/O**	General purpose digital I/O pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			STADC	**I**	ADC external trigger input.
88	56	45	PA.12	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 48-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	**I/O**	I^2C 0 clock pin
			ACMP1_P	**AI**	Comparator1 P-end input
89	57	46	PA.13	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 48-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_N	**AI**	Comparator1 N-end input
90	58	47	PA.14	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			LCD_SEG31	**O**	LCD segment output 31 at 64-pin
			LCD_SEG17	**O**	LCD segment output 17 at 48-pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
91	59	48	PA.15	**I/O**	General purpose digital I/O pin
			LCD_SEG30	**O**	LCD segment output 30 at 64-pin
			LCD_SEG16	**O**	LCD segment output 16 at 48-pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin

5 BLOCK DIAGRAM

5.1 Nano102 Block Diagram

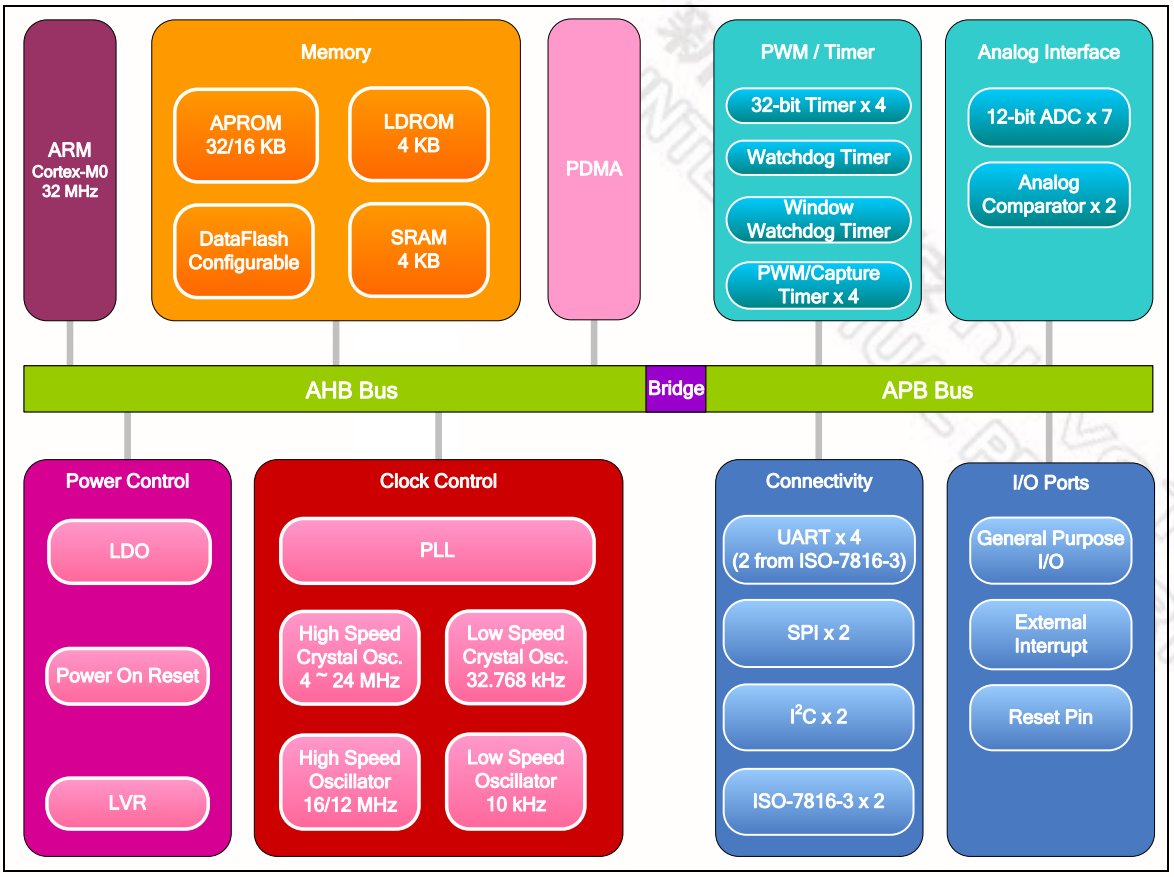


Figure 5-1 NuMicro™ Nano102 Block Diagram

6.4 System Manager

6.4.1 Overview

System manager mainly controls the power modes, wake-up sources, system resets, scalable LDO and system memory map. It also provides information about product ID, chip reset, IP reset, and multi-function pin control.

6.4.2 Features

- Power modes and wake-up sources
- System Power Architecture
- System resets
- Scalable LDO
- System Memory Map
- System manager registers for :
  - Part Number ID
  - Chip and IP reset
  - Multi-functional pin control

6.8 DMA Controller

6.8.1 Overview

The NuMicro™ NANO112 series DMA contains four-channel peripheral direct memory access (PDMA) controller and a cyclic redundancy check (CRC) generator.

The PDMA that transfers data to and from memory or transfer data to and from peripherals. For PDMA channel (PDMA CH1~CH4), there is one-word buffer as transfer buffer between the Peripherals APB devices and Memory. User can stop the PDMA operation by disable PDMACEN (PDMA_CSRx[0]). User can polling TD_IS (PDMA_ISRx[1]) or enable BLKD_IE (PDMA_IERx[1]) and wait interrupt to check PDMA transfer complete . The DMA controller can increase source or destination address, fixed or wrap around them as well.

The DMA controller contains a cyclic redundancy check (CRC) generator that can perform CRC calculation with programmable polynomial settings. The CRC engine supports CPU mode and DMA transfer mode.

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- Up to two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8 bit timers for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limitation function.
- Supports hardware activation sequence process.
- Supports hardware warm reset sequence process.
- Supports hardware deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Full duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGTR register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation

- Supports multiple address recognition (Two slave addresses with mask option)
- Supports Power-down wake-up function
- Supports two-Level FIFO

6.19 Analog to Digital Converter (ADC)

6.19.1 Overview

The Nano112 series contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 external input channels and 4 internal channels. The A/D converter supports three operation modes: Single, Single-cycle Scan and Continuous Scan mode, and can be started by software, external STADC(PA.11) pin, timer event start and PWM trigger.

Note that the I/O pins used as ADC analog input pins must configure the Pin Function (PA_L_MFP) to ADC input and off digital function (GPIOA_OFFD) should be turned on before ADC function is enabled.

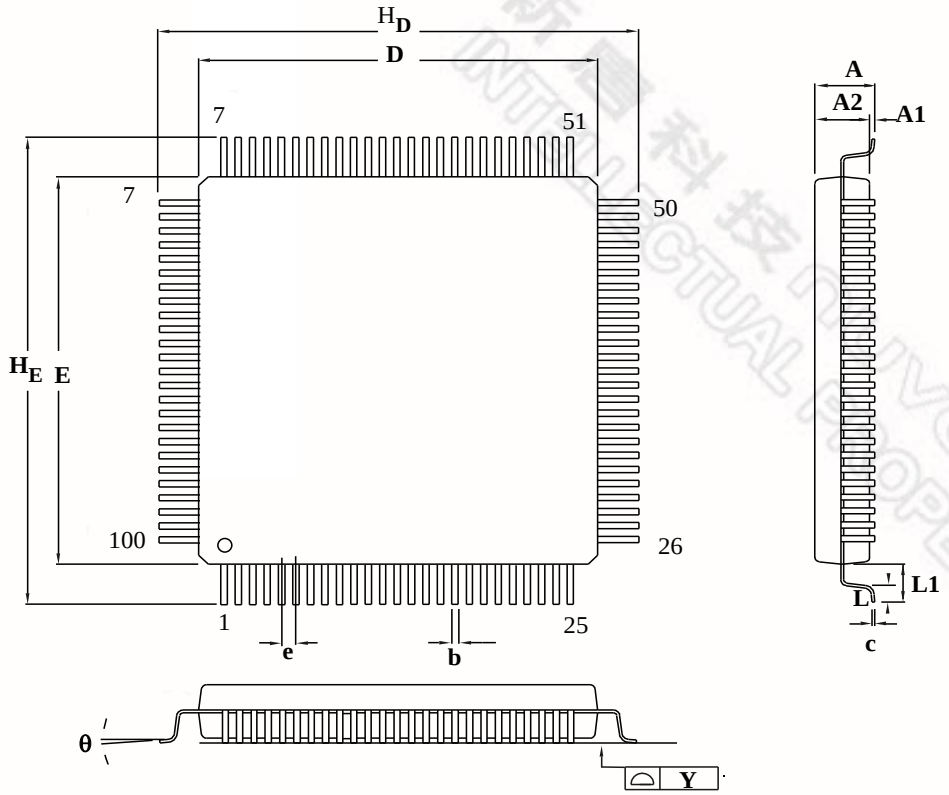
6.19.2 Features

- Analog input voltage range: 0~V_{REF} (Max to AV_{DD})
- Selectable 12-bits, 10-bits, 8-bits and 6-bits resolution
- Supports sampling time settings for channel 0~7 individually (ADCCHSAMP0 register) and channel 14~17 share the same one sampling time setting (ADCCHSAMP1 register)
- Supports two power-down modes:
  - Power-down mode
  - Standby mode
- Up to 8 external analog input channels (channel0 ~ channel7), and 4 internal channels (channel14~channel17) converting four voltage sources (internal band-gap voltage, internal temperature sensor output, AV_{DD}, and AV_{SS}).
- Maximum ADC clock frequency is 32 MHz and each conversion is 19 clocks+ sampling time depending on the input resistance (Rin).
- Three operating modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle Scan mode: A/D conversion is performed one cycle on all specified channels with the sequence from the lowest numbered channel to the highest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software write 1 to ADST bit
  - External pin STADC
  - PWM trigger
  - Selects one from four timer events (TMR0, TMR1, TMR2 and TMR3) that enable ADC and transfer AD results by PDMA
- Conversion results held in data registers for each channel
- Supports digital comparator: Conversion result can be compared with a specified value and user can select whether to generate an interrupt when conversion result is equal to the compare register setting.
- Supports Calibration and load Calibration words capability.

Operating Current Normal Run Mode HCLK =16 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD131}		5.8		mA	3.3 V	X	16 MHz	X	V
	I_{DD141}		2.3		mA	3.3 V	X	16 MHz	X	X
	I_{DD151}		5.7		mA	1.8 V	X	16 MHz	X	V
	I_{DD161}		2.3		mA	1.8 V	X	16 MHz	X	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD132}		4.0		mA	3.3 V	X	12 MHz	X	V
	I_{DD142}		1.7		mA	3.3 V	X	12 MHz	X	X
	I_{DD152}		4.0		mA	1.8 V	X	12 MHz	X	V
	I_{DD162}		1.7		mA	1.8 V	X	12 MHz	X	X
Operating Current Normal Run Mode HCLK =12 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD13}		3.8		mA	3.3 V	12 MHz	X	X	V
	I_{DD14}		1.9		mA	3.3 V	12 MHz	X	X	X
	I_{DD15}		3.8		mA	1.8 V	12 MHz	X	X	V
	I_{DD16}		1.9		mA	1.8 V	12 MHz	X	X	X
Operating Current Normal Run Mode xHCLK =4 MHz while(1){}executed from flash V_{LDO1}=1.6 V	I_{DD17}		1.3		mA	3.3 V	4 MHz	X	X	V
	I_{DD18}		0.7		mA	3.3 V	4 MHz	X	X	X
	I_{DD19}		1.3		mA	1.8 V	4 MHz	X	X	V
	I_{DD20}		0.7		mA	1.8 V	4 MHz	X	X	X
Operating Current Normal Run Mode HCLK =32.768 kHz wkhile(1){}executed from flash V_{LDO1}=1.6 V	I_{DD21}		99		uA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						3.3 V	32.768	X	X	V
	I_{DD22}		93		uA	3.3 V	32.768	X	X	X
	I_{DD23}		95		uA	1.8 V	32.768	X	X	V
	I_{DD24}		89		uA	1.8 V	32.768	X	X	X
Operating Current kNormal Run Mode HCLK =32 kHz wkhile(1){}executed from flash V_{LDO1}=1.6 V	I_{DD25}		91		uA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						3.3 V	X	10	X	V
	I_{DD26}		90		uA	3.3 V	X	10	X	X
	I_{DD27}		87		uA	1.8 V	X	10	X	V
	I_{DD28}		85		uA	1.8 V	X	10	X	X
Operating Current Idle Mode HCLK =32 MHz V_{LDO1}=1.8 V	I_{IDLE5}		8.4		mA	V_{DD}	HXT	HIRC	PLL	All digital module
						3.3 V	12 MHz	X	V	V
	I_{IDLE6}		2.6		mA	3.3 V	12 MHz	X	V	X
	I_{IDLE7}		8.0		mA	1.8 V	12 MHz	X	V	V
	I_{IDLE8}		2.5		mA	1.8 V	12 MHz	X	V	X

10 PACKAGE DIMENSIONS

10.1 100L LQFP (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.