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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112rb1an

Product Line	UART	SPI	I^2C	ADC	ACMP	RTC	SC	Timer	LCD
Nano102	●	●	●	●	●	●	●	●	
Nano112	●	●	●	●	●	●	●	●	●

Table 1-1 Connectivity Support Table

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out

- Wake system up from Power-down mode

- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible
  - Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output

- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports One-shot and Continuous mode
  - Supports Capture interrupt

- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control.
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system (CTSn, received data or RS-485 address matched) up from Power-down mode

- SPI

- Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output
- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports Capture interrupt
- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up (CTS, received data or RS-485 address matched) from Power-down mode
- SPI
  - Up to two sets of SPI controller
  - Master up to 32 MHz, and Slave up to 16 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12/16 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NTC	Negative Temperature Coefficient
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PTC	Positive Temperature Coefficient
PT1000	Thermal Resistance
PWM	Pulse Width Modulation

4.3.2.2 NuMicro™ Nano112 LQFP 64-pin

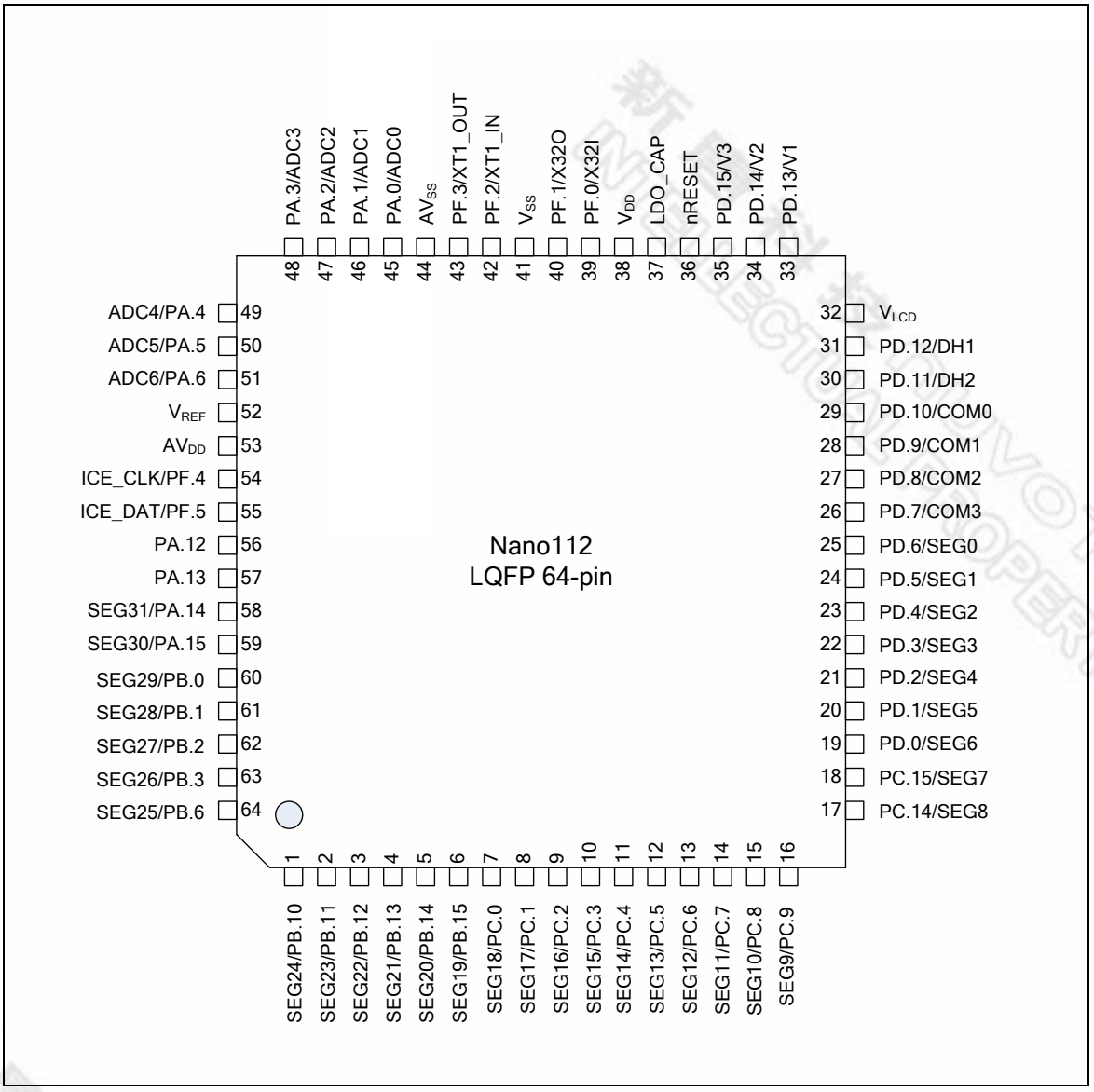

Figure 4-6 NuMicro™ Nano112 LQFP 64-pin Diagram

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
51	35	25	nRESET		External reset input: low active. Setting this pin low will reset chip to initial state. With internal pull-up.
52	37	26	LDO_CAP	**P**	LDO capacitor pin
53	38	27	V_{DD}	**P**	Power supply for I/O ports and LDO source
54	38	28	PF.0	**I/O**	General purpose digital I/O pin
			X32I	**I**	External 32.768 kHz crystal input pin(default)
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
55	40	29	PF.1	**I/O**	General purpose digital I/O pin
			X32O	**O**	External 32.768 kHz crystal output pin(default)
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
56			V_{SS_PLL}	**G**	Ground for PLL
57	41	30	V_{SS}	**G**	Ground for digital circuit
58			V_{SS}	**G**	Ground for digital circuit
59	42	31	PF.2	**I/O**	General purpose digital I/O pin
			XT1_IN	**AI**	External 4~24 MHz crystal input pin(default)
			UART1_RXD	**I**	UART1 Data receiver input pin
			TC3	**I**	Timer3 capture input
			INT1	**I**	External interrupt1 input pin
60	43	32	PF.3	**I/O**	General purpose digital I/O pin
			XT1_OUT	**AO**	External 4~24 MHz crystal output pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			TC2	**I**	Timer 2 capture input
			INT0	**I**	External interrupt0 input pin
61					NC
62			PE.0	**I/O**	General purpose digital I/O pin
			SPI0_MOSI0	**I/O**	SPI0 1st MOSI (Master Out, Slave In) pin
63			PE.1	**I/O**	General purpose digital I/O pin
			SPI0_MISO0	**I/O**	SPI0 1st MISO (Master In, Slave Out) pin
64			PE.2	**I/O**	General purpose digital I/O pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
76	49	38	PA.4	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_CD	**I**	SmartCard0 card detect pin
			ACMP0_P0	**AI**	Comparator0 P-end input0
			AD4	**AI**	ADC analog input4
77	50	39	PA.5	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SPI1_SS0	**I/O**	SPI1 1st slave select pin
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
			ACMP0_N	**AI**	Comparator0 N-end input0
			AD5	**AI**	ADC analog input5
78	51	40	PA.6	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			SC0_RST	**O**	SmartCard0 RST pin
			ACMP0_OUT	**O**	Comparator0 output
			AD6	**AI**	ADC analog input6
79			PA.7	**I/O**	General purpose digital I/O pin
			SC1_CD	**I**	SmartCard1 card detect
			AD7	**AI**	ADC analog input7
80	52	41	V_{REF}	**A**	ADC/Comparator reference voltage
81	53	42	AV_{DD}	**P**	Power supply for ADC and comparators
82	54	43	PF.4	**I/O**	General purpose digital I/O pin
			ICE_CLK	**I**	Serial Wired Debugger Clock pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			PWM0_CH2	**O**	PWM0 Channel2 output
			TC1	**I**	Timer1 capture input
			FCLK1	**O**	Frequency Divider1 output pin
83	55	44	PF.5	**I/O**	General purpose digital I/O pin
			ICE_DAT	**I/O**	Serial Wired Debugger Data pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			PWM0_CH3	**I/O**	PWM0 Channel3 output
			TC0	**I**	Timer0 capture input

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
84			PA.8	**I/O**	General purpose digital I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
85			PA.9	**I/O**	General purpose digital I/O pin
			SC0_RST	**O**	SmartCard0 RST pin
86			PA.10	**I/O**	General purpose digital I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
87			PA.11	**I/O**	General purpose digital I/O pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			STADC	**I**	ADC external trigger input.
88	56	45	PA.12	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 48-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	**I/O**	I^2C 0 clock pin
			ACMP1_P	**AI**	Comparator1 P-end input
89	57	46	PA.13	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 48-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_N	**AI**	Comparator1 N-end input
90	58	47	PA.14	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			LCD_SEG31	**O**	LCD segment output 31 at 64-pin
			LCD_SEG17	**O**	LCD segment output 17 at 48-pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
91	59	48	PA.15	**I/O**	General purpose digital I/O pin
			LCD_SEG30	**O**	LCD segment output 30 at 64-pin
			LCD_SEG16	**O**	LCD segment output 16 at 48-pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			UART1_RXD	**I**	UART1 Data receiver input pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
100	64		PB.6	**I/O**	General purpose digital I/O pin
			LCD_SEG34	**O**	LCD segment output 34 at 100-pin
			LCD_SEG25	**O**	LCD segment output 25 at 64-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_SS1	**I/O**	SPI1 2nd slave select pin
			FCLK0	**O**	Frequency Divider0 output pin

Note: Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power.

5 BLOCK DIAGRAM

5.1 Nano102 Block Diagram

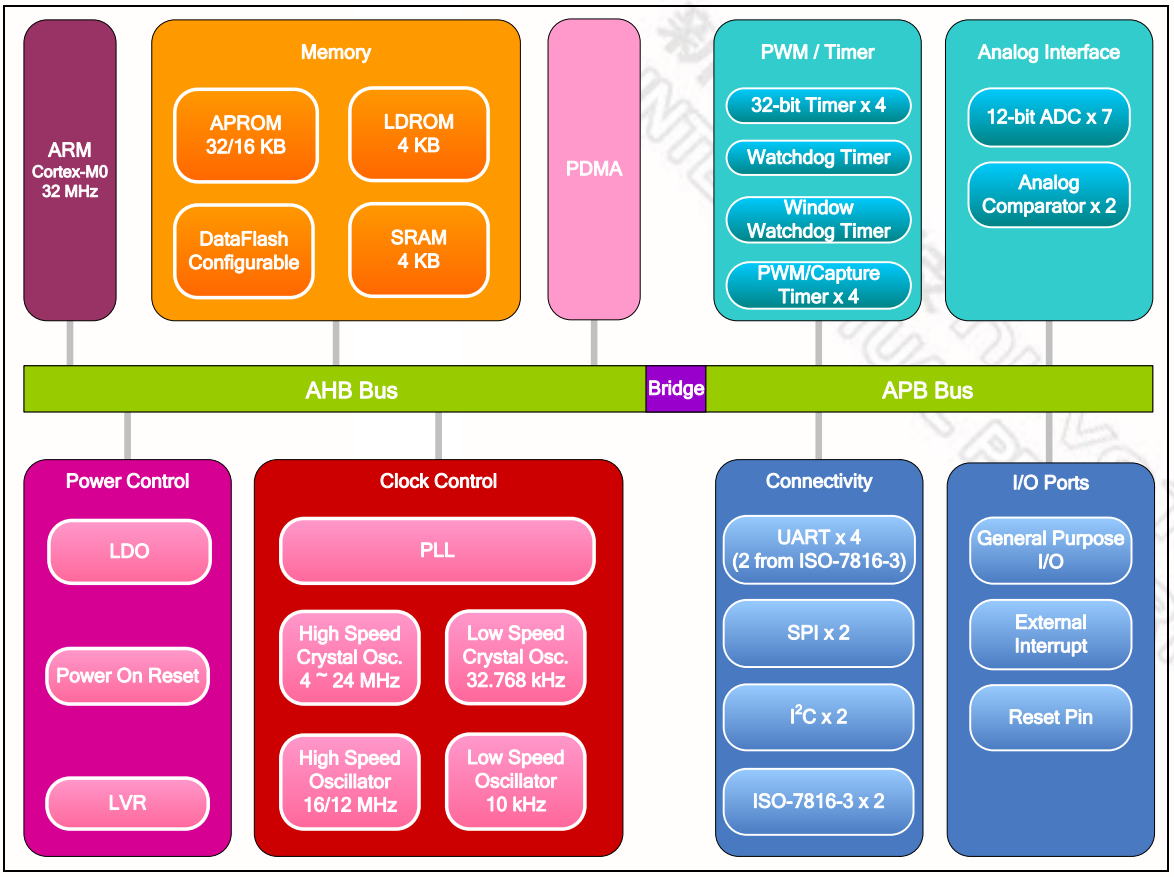

Figure 5-1 NuMicro™ Nano102 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex™-M0 Core

The Cortex™-M0 processor is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The processor can execute Thumb code and is compatible with other Cortex™-M profile processor. The profile supports two modes –Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The following figure shows the functional controller of processor.

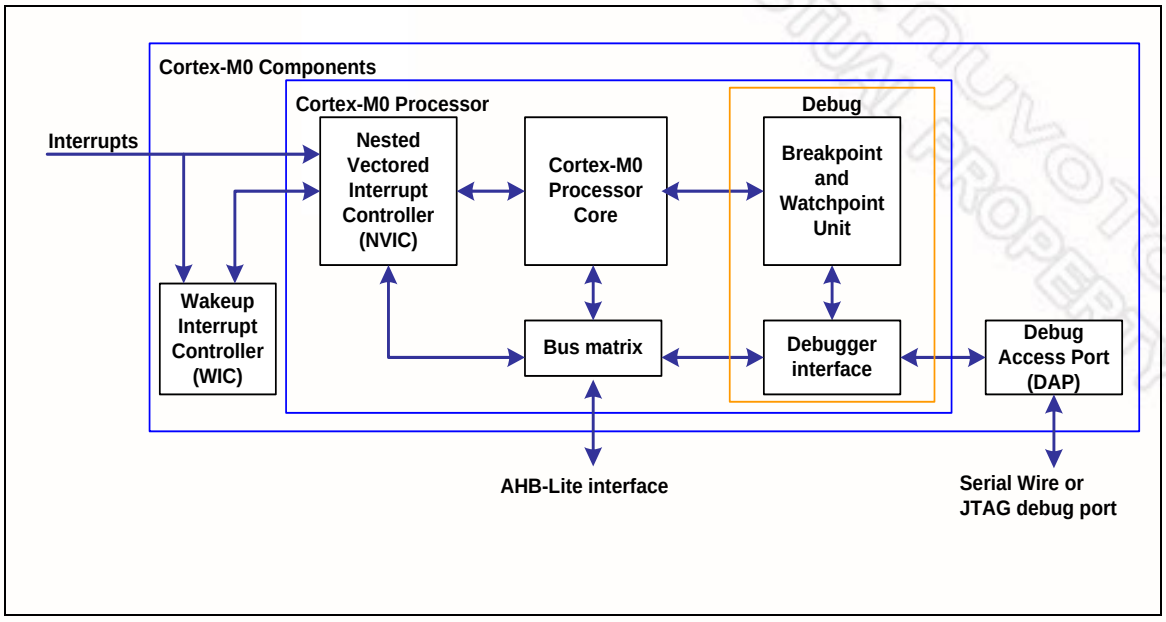

Figure 6-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - ARMv6-M Thumb® instruction set
  - Thumb-2 technology
  - ARMv6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARMv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature

6.4 System Manager

6.4.1 Overview

System manager mainly controls the power modes, wake-up sources, system resets, scalable LDO and system memory map. It also provides information about product ID, chip reset, IP reset, and multi-function pin control.

6.4.2 Features

- Power modes and wake-up sources
- System Power Architecture
- System resets
- Scalable LDO
- System Memory Map
- System manager registers for :
  - Part Number ID
  - Chip and IP reset
  - Multi-functional pin control

6.7 General Purpose I/O Controller

6.7.1 Overview

The NuMicro Nano112™ series have up to 80 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 80 pins are arranged in 6 ports named with GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, and open-drain mode. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for V_{DD} from 1.8 V to 3.6 V.

6.7.2 Features

- Three I/O modes:
  - Schmitt trigger Input-only with high impendence
  - Push-pull output
  - Open-drain output
- I/O pin configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the pin wake-up function

6.14 UART Controller

6.14.1 Overview

The UART Controller provides up to two channels of Universal Asynchronous Receiver/Transmitter (UART) modules and performs Normal Speed UART, and supports flow control function. The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU.

The UART controller also supports IrDA (SIR), LIN Master/Slave and RS-485 function modes.

There are four conditions to wake-up the system and it also supports PWM channel source selection to modulate the PWM and the UART transmitter.

6.14.2 Features

- Full duplex, asynchronous communications.
- Separate receiving / transmitting 16 bytes entry FIFO for data payloads.
- Supports hardware auto-flow control/flow control function (CTSn, RTSn) and programmable (CTSn, RTSn) flow control trigger level.
- Supports programmable baud rate generator.
- Supports auto-baud rate detect and baud rate compensation function.
- Supports programmable receiver buffer trigger level.
- Supports incoming data or CTSn or received FIFO is equal to the RFITL or RS-485 AAD mode address matched to wake-up function.
- Supports 9 bit receiver buffer time-out detection function.
- All UART Controller can be served by the PDMA.
- Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting DLY (UART_TMCTL[23:16]) register.
- Supports IrDA SIR function mode
- Supports LIN function mode.
- Supports RS-485 function mode.
- Supports PWM modulation

6.18 LCD Display Driver

6.18.1 Overview

The LCD driver can directly drive a LCD glass by creating the ac segment and common voltage signals automatically. It can support static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty LCD glass with up to 3 segments with 6 COM (segment 0 is used as LCD_COM4 and segment 1 is used as LCD_COM5) or 36 segments with 4 COM (LCD_COM0 ~ LCD_COM3).

A built-in charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage. The LCD driver would generate voltage higher than the threshold voltage in older to darken a segment and a voltage lower than threshold to make a segment clear. However, the LCD display segment will degrade if the applied voltage has a DC-component. To avoid this, the generated waveform by LCD driver are arranged such that average voltage of each segment is 0 and the RMS(root-mean-square) voltage applied on a LCD segment lower than the segment threshold making LCD clear and RMS voltage higher than the segment threshold making LCD dark.

6.18.2 Features

- Supports Segment/Com:
  - 108 dots (6x18) or 80 dots (4x20) in LQFP48 package
  - 108 dots (6x18) or 80 dots (4x20) or 132 dots (6x 22) or 96 dots (4x24) or 180 dots (6x30) or 128 dots (4x32) in LQFP64 package
  - 204 dots (6x34) or 144 dots (4x36) in LQFP100 package
- Common 0-5 multiplexing functions with GPI/O pins
- Segment 0-35 multiplexing function with GPI/O pins
- Supports Static,1/2 bias and 1/3 bias voltage
- Six display modes: Static,1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty or 1/6 duty Selectable LCD frequency by frequency divider
- Configurable frame frequency
- Internal Charge pump, adjustable contrast adjustment
- Embedded LCD bias reference ladder (R-Type, 200/300/400 kΩ resisters)
- Configurable Charge pump frequency
- Blinking capability
- Supports R/C/Ext_C-type method
- LCD frame interrupt

8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU clock	Current
Nano102/112 series	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.89mA 157uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	800uA 67uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.65mA 137uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	560uA 46uA/MHz
	RTC + LCD Mode: (RAM retention) (Power down with LXT and LCD enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC and LCD circuit. Without panel loading Set LDO output = 1.6V Only for Nano112 LCD series	InternL C-Type (With internal Charge pump)	3.3V	Stop	9.5uA
		InternL R-Type (With internal resistor ladder) 200kΩ			8.3uA
		InternL R-Type (With internal resistor ladder) 300kΩ			6.4uA
		InternL R-Type (With internal resistor ladder) 400kΩ			5.5uA
		External C-Type (With 0.1uF cap. ladder)			2.5uA
		External R-type (With 1MΩ resister ladder)			3.7uA
	RTC Mode: (RAM retention) (Power down with LXT enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC circuit Set LDO output = 1.6V		3.3V	Stop	1.5uA
	Power Down Mode: (RAM retention) CPU and all clocks stop Set LDO output = 1.6V		3.3V	Stop	0.65uA
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from wake-up event to first CPU core valid clock)		3.3V	12 MHz	6us
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from interrupt event to interrupt service routine first instruction)		3.3V	12 MHz	7us

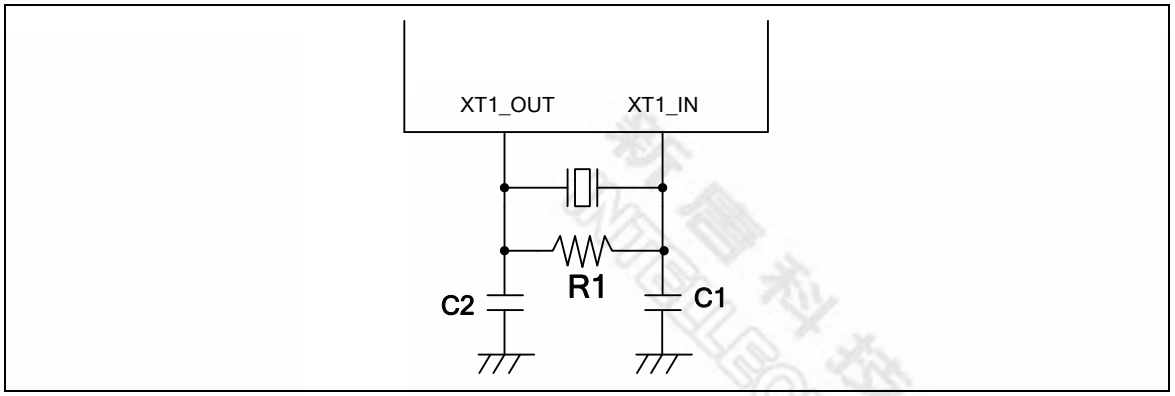

Figure 9-1 Typical Crystal Application Circuit

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1		μA	VDD = 3.0V

9.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

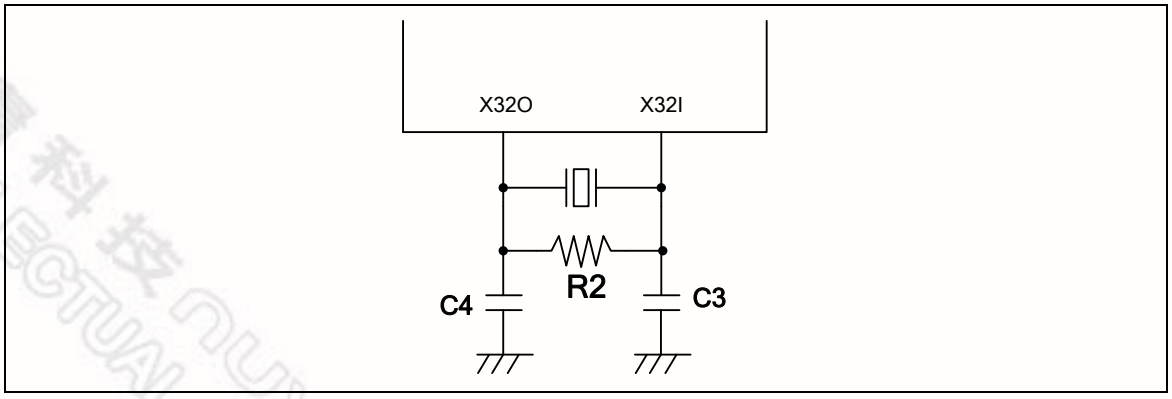

Figure 9-2 Typical Crystal Application Circuit

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
other analog modules)	I_{ADC2}		30		μA	AV_{DD} = V_{DD} = 3.0V ADC_VREF = AV_{DD} ADC Clock Rate = 2 MHz
Resolution	R_{ADC}			12	Bit	
Reference voltage	V_{REF}	1.8		A_{VDD}	V	
Reference input current (Avg.)	I_{REF}			1	μA	
ADC input voltage	V_{IN}	0		V_{REF}	V	
Conversion time	T_{CONV}	1			μS	
Conversion Rate	F_{SPS}			1.5M	Hz	V_{DD} = 3V
Integral Non-Linearity Error	INL		±1		LSB	V_{REF} is external Vref pin
Differential Non-Linearity	DNL		±0.8		LSB	V_{REF} is external Vref pin
Gain error	E_G		±2		LSB	V_{REF} is external Vref pin
Offset error	E_{OFFSET}		±1.5		LSB	V_{REF} is external Vref pin
Absolute error	E_{ABS}		-	±6	LSB	V_{REF} is external Vref pin
ADC Clock frequency	F_{ADC}	0.25		32	MHz	
Clock cycle	AD_{CYC}	20			Cycle	
Internal Capacitance	C_{IN}	-	5	-	pF	
Monotonic	-	Guaranteed			-	

9.4.2 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	-
T_A	Temperature	-40	25	85	℃	-
I_{BOD}	Quiescent Current	-	1		μA	AV_{DD} = 3V
V_{BOD}	Brown-out Voltage 25℃	2.4	2.5	2.6	V	BODCTL[2] = 1
		1.9	2.0	2.1	V	BODCTL[1] = 1
		1.6	1.7	1.8	V	BODCTL[0] = 1