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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112rc2an

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- Up to two sets of SPI controllers
- Master up to 32 MHz, and Slave up to 16 MHz
- Supports SPI/MICROWIRE Master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 4 to 32 bits
- MSB or LSB first data transfer
- RX and TX on both rising or falling edge of serial clock independently
- Two slave/device select lines when SPI controller is used as the master, and 1 slave/device select line when SPI controller is used as the slave
- Supports byte suspend mode in 32-bit transmission
- Supports two channel PDMA requests, one for transmit and another for receive
- Supports three wire mode, no slave select signal, bi-direction interface
- Wake system up(SPI clock toggle) from Power-down mode

- I^2C
  - Up to two sets of I^2C device
  - Master/Slave up to 1 Mbit/s
  - Bi-directional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
  - Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows
  - Programmable clocks allowing for versatile rate control
  - Supports 7-bit addressing mode
  - Supports multiple address recognition (four slave addresses with mask option)
  - Wake system up(address match) from Power-down mode
- ADC
  - 12-bit SAR ADC up to 1Msps conversion rate
  - Up to 8-ch single-ended input from external pin (PA.0 ~ PA.7)
  - Four internal channels from internal reference voltage (Int_V_{REF}), Temperature sensor, AV_{DD}, and AV_{SS}.
  - Supports three reference voltage sources from V_{REF} pin, internal reference voltage (Int_V_{REF}), and AV_{DD}.
  - Supports Single Scan, Single Cycle Scan, and Continuous Scan mode
  - Each channel with individual result register
  - Only scan on enabled channels

2.2 Nano112 Features – LCD Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access.
  - 16/32 Kbytes application program memory (APROM)
  - 4 Kbytes In System Programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA : Supports 5 channels: 4 PDMA channels, and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC
    - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
      - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$

- CRC-8: $X^8 + X^2 + X + 1$
- CRC-16: $X^{16} + X^{15} + X^2 + 1$
- CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, P.0(X32I), PF.1(X32O)
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible

enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full-duplex)
- ACMP
  - Suuports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- LCD
  - LCD driver for up to 4 COM x 36 SEG or 6 COM x 34 SEG
  - Supports Static,1/2 bias and 1/3 bias voltage
  - Six display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
  - Selectable LCD frequency by frequency divider
  - Configurable frame frequency
  - Internal Charge pump, adjustable contrast adjustment
  - Configurable Charge pump frequency
  - Blinking capability
  - Supports R-type/C-type/External C-type method
  - Configurable internal R-ladder resistor value (200K/300K/400K)
  - LCD frame interrupt
- One built-in temperature sensor with 1℃ resolution

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			PWM0_CH1	I/O	PWM0 Channel1 output
9	7		PC.2	I/O	General purpose digital I/O pin
			I2C1_SCL	O	I^2C1 clock pin
			PWM0_CH2	I/O	PWM0 Channel2 output
10	8		PC.3	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output
11	9	5	PC.4	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
12	10		PC.5	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
13	11	6	PC.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SC0_DAT	I/O	SmartCard0 DATA pin (SC0_UART_RXD)
14	12	7	PC.7	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_PWR	O	SmartCard0 Power pin
15	13	8	PC.8	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	O	SmartCard0 RST pin
16	14		PC.9	I/O	General purpose digital I/O pin
		9	PC.10	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I^2C1 clock pin
			SC1_CD	I	SmartCard1 card detect
		10	PC.11	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C 1 data I/O pin
			SC1_PWR	O	SmartCard1 PWR pin
		11	PC.12	I/O	General purpose digital I/O pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			AD0	AI	ADC analog input0
46	35		PA.1	I/O	General purpose digital I/O pin
			AD1	AI	ADC analog input1
			ACMP0_P3	AI	Comparator0 P-end input3
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
47	36		PA.2	I/O	General purpose digital I/O pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
			AD2	AI	ADC analog input2
			ACMP0_P2	AI	Comparator0 P-end input2
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
48	37		PA.3	I/O	General purpose digital I/O pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			INT1	I	External interrupt 1
			AD3	AI	ADC analog input3
			ACMP0_P1	AI	Comparator0 P-end input1
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
49	38	25	PA.4	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
			AD4	AI	ADC analog input4
			ACMP0_P0	AI	Comparator0 P-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
50	39	26	PA.5	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			SC0_PWR	O	SmartCard0 Power pin
			AD5	AI	ADC analog input5
			ACMP0_N	AI	Comparator0 N-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
51	40		PA.6	I/O	General purpose digital I/O pin
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
			SC0_RST	O	SmartCard0 RST pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

5.2 Nano112 Block Diagram

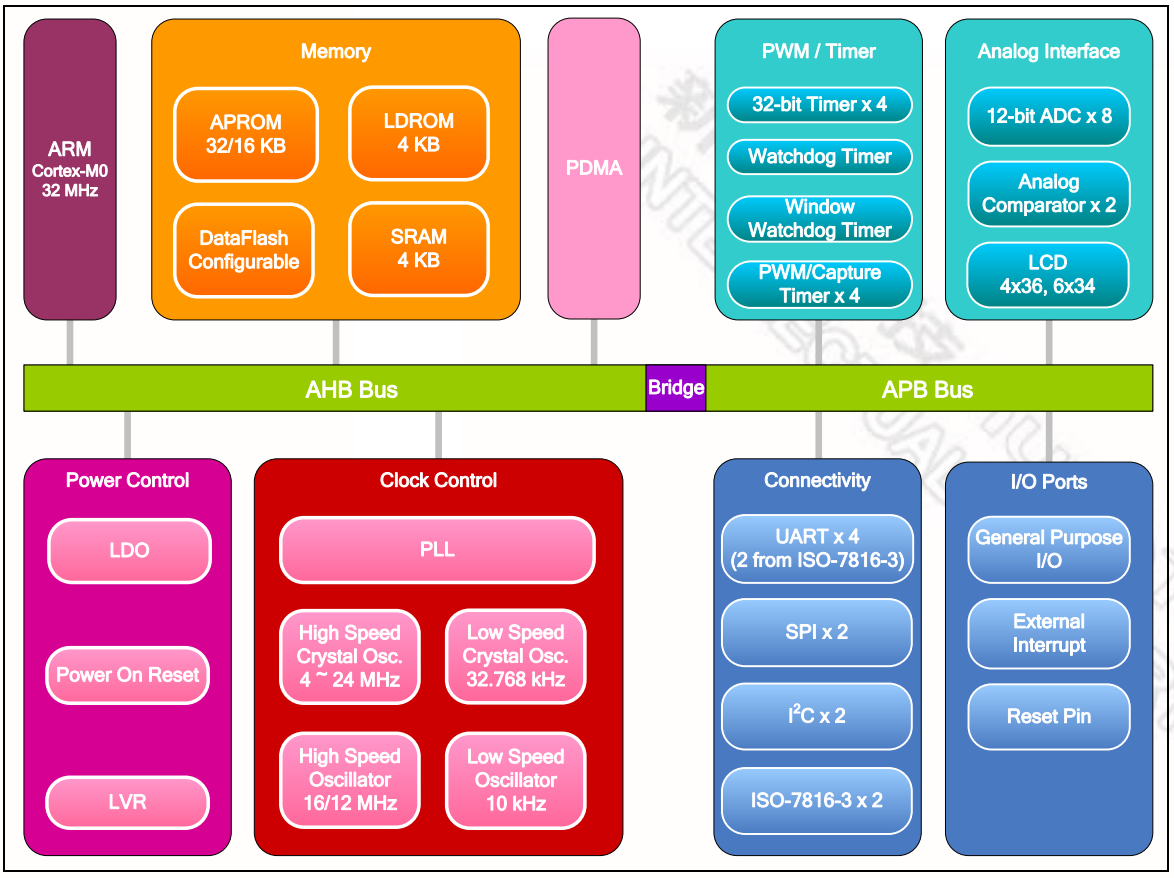

Figure 5-2 NuMicro™ Nano112 Block Diagram

- NVIC:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.10 Pulse Width Modulation (PWM)

6.10.1 Overview

This chip has one PWM controller, which includes 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators.

Each of the two PWM outputs, (CH0, CH1), (CH2, CH3), share the same 8-bit prescaler, clock divider providing 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16). Each PWM output has independent 16-bit PWM counter which has two counting modes for PWM period control. The PWM counter operates as down counting in edge-aligned mode and up-down counting in center-aligned mode only. Each PWM output also has a 16-bit comparator for PWM duty control. Each dead-zone generator has two outputs. The first dead-zone generator output is CH0 and CH1, and for the second dead-zone generator, the output is CH2 and CH3. The PWM controller total provide four independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter in edge-aligned mode (or up-down counter in center-aligned mode) reaches 0. PWM interrupt will be asserted when both PWM interrupt source and its corresponding enable bit are active. Each PWM output can be configured as one-shot mode to produce only one PWM cycle signal or continuous mode to output PWM waveform continuously.

When DZEN01(PWM_CTL[4]) is set, CH0 and CH1 perform complementary PWM paired function; the paired PWM timing, period, duty and dead-time are determined by PWM channel 0 timer and Dead-zone generator 0. Similarly, When DZEN23(PWM_CTL[5]) is set the complementary PWM pair of (CH2, CH3) is controlled by PWM channel 2.

To prevent PWM driving output pin with unsteady waveform, the 16-bit period down counter and 16-bit comparator are implemented with double buffer. When user writes data to counter/comparator buffer registers the updated value will be loaded into the 16-bit down counter/ comparator at the time down counter reaching 0. The double buffering feature avoids glitch at PWM outputs.

When the 16-bit period down counter reaches 0, the interrupt request is generated. If PWM output is set as continuous mode, when the down counter reaches 0, it is reloaded with CN of PWM_DUTYy(y=0~3) Register automatically then start decreases, repeatedly. If the PWM output is set as one-shot mode, the down counter will stop and generate one interrupt request when it reaches 0.

The value of PWM counter comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

The alternate feature of the PWM is digital input capture function. If capture function is enabled the PWM output pin is switched as capture input pin. The capture channel 0 and PWM CH0 share one timer; and the capture channel 1 and PWM CH1 share one timer, and etc. Therefore user must set up the PWM timer before enabling capture feature. After capture feature of channel 0 is enabled, the capture always latches PWM CH0 timer value to Capture Rising Latch Register CRL (PWM_CRL0[15:0]) when input channel has a rising transition and latches PWM CH0 timer value to Capture Falling Latch Register CFL (PWM_CFL0[15:0]) when input channel has a falling transition. Capture channel 0 interrupt is programmable by setting CRL_IE0(PWM_CAPINTEN[0]) for rising transition or CFL_IE0 (PWM_CAPINTEN[1]) for falling transition. Whenever Capture rising event latched for channel 0, the PWM CH0 timer will be reload at this moment if the corresponding reload enable bit CAPRELOADREN0 (PWM_CAPCTL[6]) is set.

The maximum captured frequency that PWM can capture is dominated by the capture interrupt latency. When capture interrupt occurs, software will do at least three steps, they are: Read PWMINTSTS to tell it from interrupt source and Read PWM_CRLy/PWM_CFLy(y=0~3) to get capture value and finally write 1 to clear PWM_INTSTS. If interrupt latency will take time T0 to finish, the capture signal mustn't transient during this interval. In this case, the maximum capture frequency will be 1/T0.

6.15 Smart Card Host Interface (SC)

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO-7816-3 T = 0, T = 1 compliant.
- EMV2000 compliant
- Up to two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads.
- Programmable transmission clock frequency.
- Programmable receiver buffer trigger level.
- Programmable guard time selection (11 ETU ~ 267 ETU).
- A 24-bit and two 8 bit timers for Answer to Request (ATR) and waiting times processing.
- Supports auto inverse convention function.
- Supports transmitter and receiver error retry and error number limitation function.
- Supports hardware activation sequence process.
- Supports hardware warm reset sequence process.
- Supports hardware deactivation sequence process.
- Supports hardware auto deactivation sequence when detected the card removal.
- Supports UART mode
  - Full duplex, asynchronous communications.
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads.
  - Supports programmable baud rate generator for each channel.
  - Supports programmable receiver buffer trigger level.
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SC_EGTR register.
  - Programmable even, odd or no parity bit generation and detection.
  - Programmable stop bit, 1 or 2 stop bit generation

6.18 LCD Display Driver

6.18.1 Overview

The LCD driver can directly drive a LCD glass by creating the ac segment and common voltage signals automatically. It can support static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty LCD glass with up to 3 segments with 6 COM (segment 0 is used as LCD_COM4 and segment 1 is used as LCD_COM5) or 36 segments with 4 COM (LCD_COM0 ~ LCD_COM3).

A built-in charge pump function can be enabled to provide the LCD glass with higher voltage than the system voltage. The LCD driver would generate voltage higher than the threshold voltage in older to darken a segment and a voltage lower than threshold to make a segment clear. However, the LCD display segment will degrade if the applied voltage has a DC-component. To avoid this, the generated waveform by LCD driver are arranged such that average voltage of each segment is 0 and the RMS(root-mean-square) voltage applied on a LCD segment lower than the segment threshold making LCD clear and RMS voltage higher than the segment threshold making LCD dark.

6.18.2 Features

- Supports Segment/Com:
  - 108 dots (6x18) or 80 dots (4x20) in LQFP48 package
  - 108 dots (6x18) or 80 dots (4x20) or 132 dots (6x 22) or 96 dots (4x24) or 180 dots (6x30) or 128 dots (4x32) in LQFP64 package
  - 204 dots (6x34) or 144 dots (4x36) in LQFP100 package
- Common 0-5 multiplexing functions with GPI/O pins
- Segment 0-35 multiplexing function with GPI/O pins
- Supports Static,1/2 bias and 1/3 bias voltage
- Six display modes: Static,1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty or 1/6 duty Selectable LCD frequency by frequency divider
- Configurable frame frequency
- Internal Charge pump, adjustable contrast adjustment
- Embedded LCD bias reference ladder (R-Type, 200/300/400 kΩ resisters)
- Configurable Charge pump frequency
- Blinking capability
- Supports R/C/Ext_C-type method
- LCD frame interrupt

6.20 Analog Comparator Controller (ACMP)

6.20.1 Overview

The Nano112 series contains two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes. The comparator ACMP0 can be used as normal comparator or it can emulate ADC function. The comparator ACMP1 can be used as normal comparator only.

6.20.2 Features

- Analog input voltage range: 0 ~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Comparator ACMP0 supports
  - 4 positive sources(ACMP0_Px)
    - PA.1, PA.2, PA.3, or PA.4
  - 4 negative sources
    - PA.5 (ACMP0_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP1 supports
  - 1 positive source
    - PA.12(ACMP1_P)
  - 4 negative sources
    - PA.13(ACMP1_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP0 supports three operation modes:
  - Normal Comparator mode
  - Single Slope ADC mode: Resistance measurement (e.g. PTC, NTC, PT1000)
    - Supports to measure 7 channels resistor
  - Sigma-Delta ADC mode
    - Supports up to 4 channel voltage input from ACMP0_Px

Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	I_{IDLE9}		2.8		mA	3.3 V	12 MHz	X	X	V
	I_{IDLE10}		0.8		mA	3.3 V	12 MHz	X	X	X
	I_{IDLE11}		2.8		mA	1.8 V	12 MHz	X	X	V
	I_{IDLE12}		0.8		mA	1.8 V	12 MHz	X	X	X

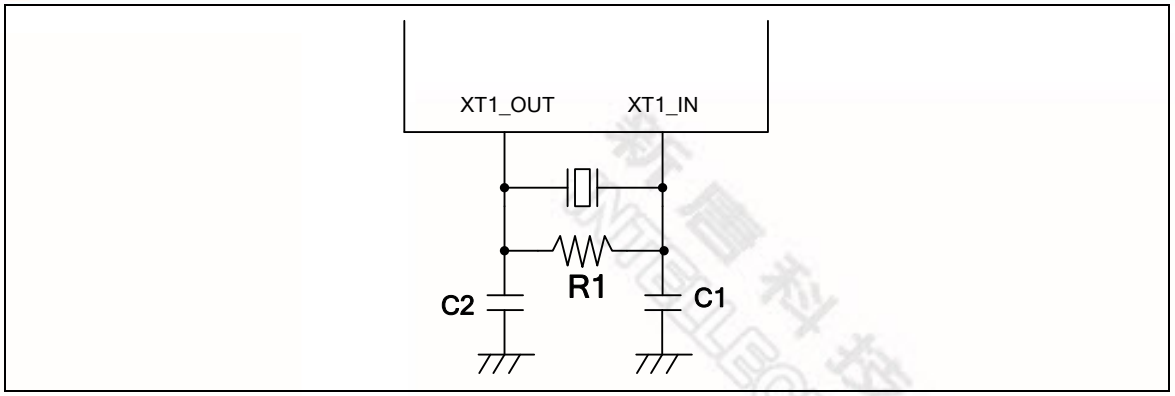

Figure 9-1 Typical Crystal Application Circuit

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1		μA	VDD = 3.0V

9.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

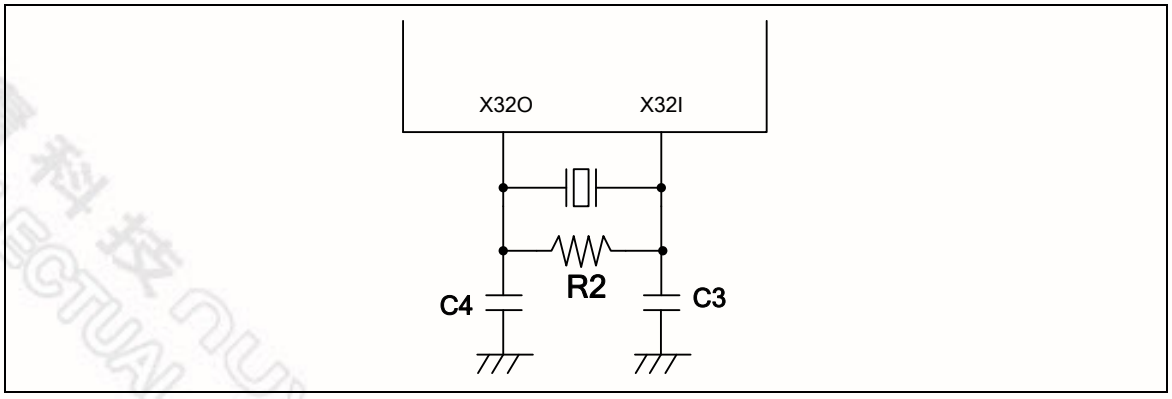

Figure 9-2 Typical Crystal Application Circuit

9.4.3 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Reset Voltage		1.6		V	-

9.4.4 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION (supply voltage = 3V)
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40		+85	^oC	
Operating current	I_{TEMP}	-	5	-	μA	
Gain	V_{TG}	-1.76	-1.68	-1.60	mV/^oC	
Offset	V_{TO}	735	745	755	mV	Tempeature at 0 ^oC

Note: Internal operation voltage comes form LDO.

9.4.5 LCD

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{DD}	1.8	-	3.6	V	
VLCD voltage	V_{LCD34}	-	3.4	-	V	CPUMP_VOL_SET=111, no loading
VLCD voltage	V_{LCD33}	-	3.3	-	V	CPUMP_VOL_SET=110, no loading
VLCD voltage	V_{LCD32}	-	3.2	-	V	CPUMP_VOL_SET=101, no loading
VLCD voltage	V_{LCD31}	-	3.1	-	V	CPUMP_VOL_SET=100, no loading
VLCD voltage	V_{LCD30}	-	3.0	-	V	CPUMP_VOL_SET=011, no loading
VLCD voltage	V_{LCD29}	-	2.9	-	V	CPUMP_VOL_SET=010, no loading
VLCD voltage	V_{LCD28}	-	2.8	-	V	CPUMP_VOL_SET=001, no loading
VLCD voltage	V_{LCD27}	-	2.7	-	V	CPUMP_VOL_SET=000, no loading
Operating current (Include 32.768 KHz crystal OSC and RTC operating)	I_{LCDint}	-	9.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal C type, with 0.1uF)
	I_{LCDext}	I_{LCDint}	2.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (external C type with 0.1uF)

11 REVISION HISTORY

Date	Revision	Description
2014.03.28	1.00	1. Initial release
2014.05.08	1.01	1. Modified some typos and format.
2014.09.02	1.02	1. Modified the pin description for LCD_Vx in section 4.4. 2. Modified all PWM1 group to PWM0 group in section 6.10. 3. Modified “PWM1 channel 2 and 3” to “PWM0 channel 2 and 3” in section 6.10. 4. Modified some typos and format.
2015.01.15	1.03	1. Updated ADC channel number in NANO102 feature list in Chapter 2. 2. Corrected typo in NANO102 64-pin sequence in section 4.4. 3. Updated all power related pins from “VDD, VSS, AVDD, AVSS, VTEMP and VLCD” to “V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, V_{TEMP} and V_{LCD}” in the Datashhet.

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