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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112sb1an

LIST OF TABLES

Product Line	UART	SPI	I^2C	ADC	ACMP	RTC	SC	Timer	LCD
Nano102	●	●	●	●	●	●	●	●	
Nano112	●	●	●	●	●	●	●	●	●

Table 1-1 Connectivity Support Table

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, PF.0(X32I), PF.1(X32O).
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-counting timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out

- Threshold voltage detection (comparator function)
- Conversion started by software programming or external input
- Supports PDMA mode
- Supports up to four timer time-out events (TMR0, TMR1, TMR2 and TMR3) to enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive/transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full–duplex)
- ACMP
  - Supports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- One built-in temperature sensor with 1℃ resolution
- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin(7x7) / 48-pin(7x7)/ QFN33-pin(5x5)

- CRC-8: $X^8 + X^2 + X + 1$
- CRC-16: $X^{16} + X^{15} + X^2 + 1$
- CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

- Clock Control
  - Flexible selection for different applications
  - Built-in 12/16 MHz OSC, can be trimmed to 1 % deviation within all temperature range when turning on auto-trim function (system must have external 32.768 kHz crystal input) otherwise 12/16 MHz OSC has 2 % deviation within all temperarure range.
  - Low power 10 kHz OSC for watchdog and low power system operation
  - Supports one PLL, up to 32 MHz, for high performance system operation
  - External 4~24 MHz crystal input for precise timing operation
  - External 32.768 kHz crystal input for RTC function and low power system operation
- GPIO
  - Three I/O modes:
    - Push-Pull output
    - Open-Drain output
    - Input only with high impendence
  - All inputs with Schmitt trigger
  - I/O pin configured as interrupt source with edge/level setting
  - Supports High Driver and High Sink I/O mode
  - Supports input 5V tolerance, except PA.0 ~ PA.7, PA.12, PA.13, P.0(X32I), PF.1(X32O)
- Timer
  - Supports 4 sets of 32-bit timers, each with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent Clock Source for each timer
  - Provides one-shot,periodic, output toggle and continuous operation modes
  - Internal trigger event to ADC and PDMA
  - Supports PDMA mode
  - Wake system up from Power-down mode
- Watchdog Timer
  - Clock Source from LIRC (Internal 10 kHz Low Speed Oscillator Clock)
  - Selectable time-out period from 1.6 ms ~ 26 sec (depending on clock source)
  - Interrupt or reset selectable when watchdog time-out
  - Wake system up from Power-down mode
- Window Watchdog Timer(WWDT)
  - 6-bit down counter and 6-bit compare value to make the window period flexible

- Selectable WWDT clock pre-scale counter to make WWDT time-out interval variable.

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 periodic options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Wake system up from Power-down mode
  - Supports 80 bytes spare registers and a snoop pin to clear the content of these spare registers
  - Supports 1, 1/2, 1/4, 1/8, 1/16 Hz clock output
- PWM/Capture
  - Supports 1 PWM module with two 16-bit PWM generators
  - Provides four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock divider, one 8-bit prescaler, two clock selectors, and one Dead-zone generator for complementary paired PWM
  - (Shared with PWM timers) with four 16-bit digital capture timers provides four rising/ falling/both capture inputs.
  - Supports Capture interrupt
- UART
  - Up to 1 Mbit/s baud rate and support 9600 baud rate @ 32kHz, low power mode
  - Up to two 16-byte FIFO UART controllers
  - UART ports with flow control (TX, RX, CTSn and RTSn)
  - Supports IrDA (SIR) function
  - Supports LIN function
  - Supports RS-485 9 bit mode and direction control (Low Density Only)
  - Programmable baud rate generator
  - Supports PDMA mode
  - Wake system up (CTS, received data or RS-485 address matched) from Power-down mode
- SPI
  - Up to two sets of SPI controller
  - Master up to 32 MHz, and Slave up to 16 MHz
  - Supports SPI/MICROWIRE Master/Slave mode
  - Full duplex synchronous serial data transfer

- Brown-out
  - Built-in 2.5V/2.0V/1.7V BOD for wide operating voltage range operation
- 96-bit unique ID
- 128-bit unique customer ID
- Operating Temperature: -40℃~85℃
- Packages:
  - All Green package (RoHS)
  - LQFP 100-pin(14x14) / 64-pin(10x10) / 64-pin(7x7) / 48-pin(7x7)

4.3.1.3 NuMicro™ Nano102 QFN 33-pin

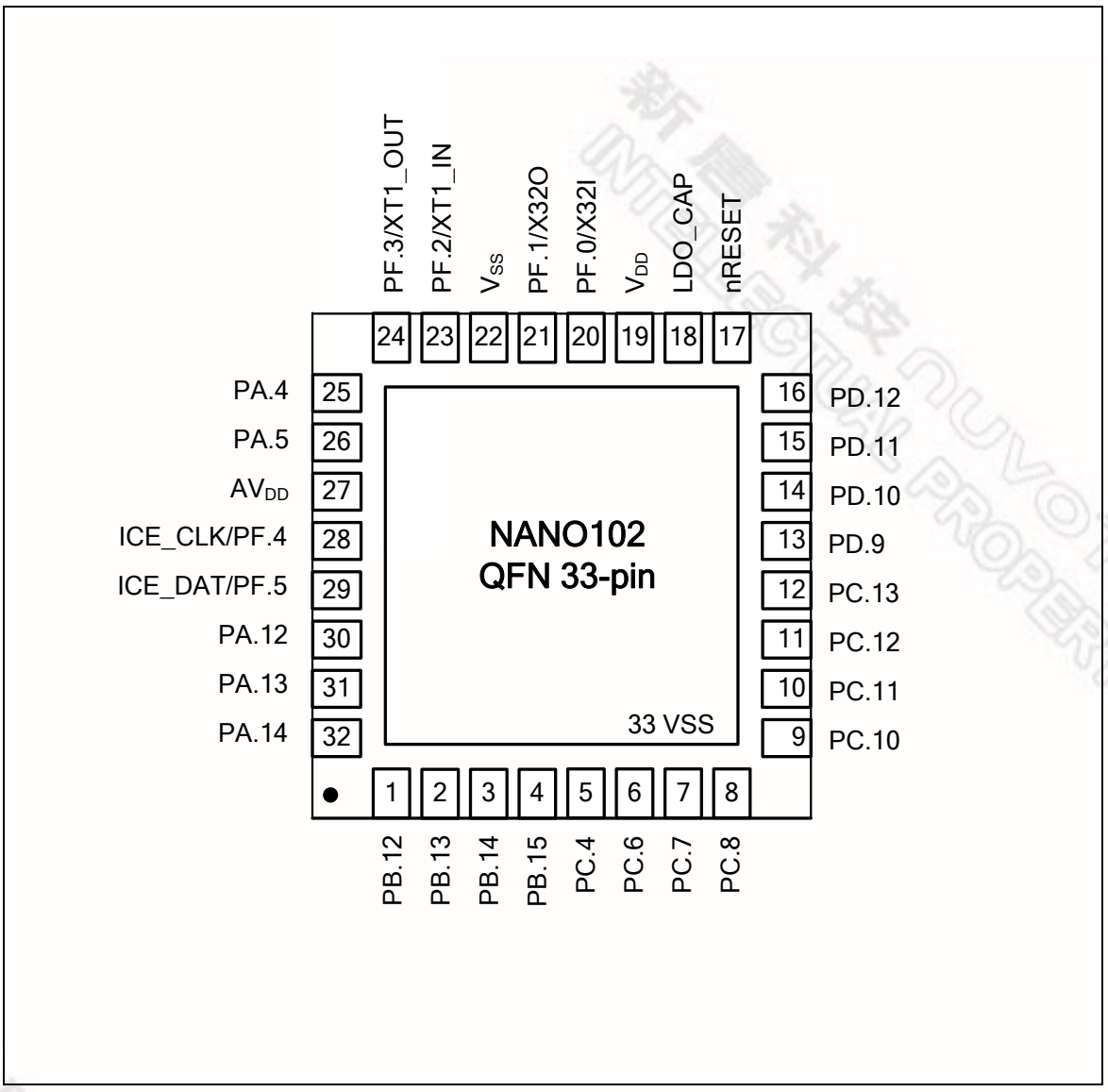


Figure 4-4 NuMicro™ Nano102 QFN 32-pin Diagram

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			PWM0_CH1	I/O	PWM0 Channel1 output
9	7		PC.2	I/O	General purpose digital I/O pin
			I2C1_SCL	O	I^2C1 clock pin
			PWM0_CH2	I/O	PWM0 Channel2 output
10	8		PC.3	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			PWM0_CH3	I/O	PWM0 Channel3 output
11	9	5	PC.4	I/O	General purpose digital I/O pin
			UART1_CTSn	I	UART1 Clear to Send input pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
12	10		PC.5	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
13	11	6	PC.6	I/O	General purpose digital I/O pin
			UART1_RTSn	O	UART1 Request to Send output pin
			SC0_DAT	I/O	SmartCard0 DATA pin (SC0_UART_RXD)
14	12	7	PC.7	I/O	General purpose digital I/O pin
			UART1_RXD	I	UART1 Data receiver input pin
			SC0_PWR	O	SmartCard0 Power pin
15	13	8	PC.8	I/O	General purpose digital I/O pin
			UART1_TXD	O	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SC0_RST	O	SmartCard0 RST pin
16	14		PC.9	I/O	General purpose digital I/O pin
		9	PC.10	I/O	General purpose digital I/O pin
			I2C1_SCL	I/O	I^2C1 clock pin
			SC1_CD	I	SmartCard1 card detect
		10	PC.11	I/O	General purpose digital I/O pin
			I2C1_SDA	I/O	I^2C 1 data I/O pin
			SC1_PWR	O	SmartCard1 PWR pin
		11	PC.12	I/O	General purpose digital I/O pin
			SC1_CLK	O	SmartCard1 clock pin (SC1_UART_TXD)

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			AD0	AI	ADC analog input0
46	35		PA.1	I/O	General purpose digital I/O pin
			AD1	AI	ADC analog input1
			ACMP0_P3	AI	Comparator0 P-end input3
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
47	36		PA.2	I/O	General purpose digital I/O pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
			AD2	AI	ADC analog input2
			ACMP0_P2	AI	Comparator0 P-end input2
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
48	37		PA.3	I/O	General purpose digital I/O pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			INT1	I	External interrupt 1
			AD3	AI	ADC analog input3
			ACMP0_P1	AI	Comparator0 P-end input1
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
49	38	25	PA.4	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
			AD4	AI	ADC analog input4
			ACMP0_P0	AI	Comparator0 P-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
50	39	26	PA.5	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			SC0_PWR	O	SmartCard0 Power pin
			AD5	AI	ADC analog input5
			ACMP0_N	AI	Comparator0 N-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
51	40		PA.6	I/O	General purpose digital I/O pin
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
			SC0_RST	O	SmartCard0 RST pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_SEG26	O	LCD segment output 26 at 100-pin
			LCD_SEG22	O	LCD segment output 22 at 64-pin
			LCD_SEG15	O	LCD segment output 15 at 48-pin
			UART0_RTSn	O	UART0 Request to Send output pin
			SPI0_MOSI0	I/O	SPI0 1st MOSI (Master Out, Slave In) pin
			TM0	I/O	Timer0 external counter input or Timer0 toggle out.
			FCLK0	O	Frequency Divider0 output pin
9	4	2	PB.13	I/O	General purpose digital I/O pin
			LCD_SEG25	O	LCD segment output 25 at 100-pin
			LCD_SEG21	O	LCD segment output 21 at 64-pin
			LCD_SEG14	O	LCD segment output 14 at 48-pin
			UART0_RXD	I	UART0 Data receiver input pin
			SPI0_MISO0	I/O	SPI0 1st MISO (Master In, Slave Out) pin
10	5	3	PB.14	I/O	General purpose digital I/O pin
			LCD_SEG24	O	LCD segment output 24 at 100-pin
			LCD_SEG20	O	LCD segment output 20 at 64-pin
			LCD_SEG13	O	LCD segment output 13 at 48-pin
			UART0_TXD	O	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI0_CLK	I/O	SPI0 serial clock pin
11			NC		
12	6	4	PB.15	I/O	General purpose digital I/O pin
			LCD_SEG23	O	LCD segment output 23 at 100-pin
			LCD_SEG19	O	LCD segment output 19 at 64-pin
			LCD_SEG12	O	LCD segment output 12 at 48-pin
			UART0_CTSn	I	UART0 Clear to Send input pin
			SPI0_SS0	I/O	SPI0 1st slave select pin
13	7	5	PC.0	I/O	General purpose digital I/O pin
			LCD_SEG22	O	LCD segment output 24 at 100-pin
			LCD_SEG18	O	LCD segment output 18 at 64-pin
			LCD_SEG11	O	LCD segment output 11 at 48-pin
			SPI0_SS1	I/O	SPI0 2nd slave select pin
			I2C0_SCL	I/O	I^2C0 clock pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			UART1_RXD	**I**	UART1 Data receiver input pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
100	64		PB.6	**I/O**	General purpose digital I/O pin
			LCD_SEG34	**O**	LCD segment output 34 at 100-pin
			LCD_SEG25	**O**	LCD segment output 25 at 64-pin
			UART1_TXD	**O**	UART1 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_SS1	**I/O**	SPI1 2nd slave select pin
			FCLK0	**O**	Frequency Divider0 output pin

Note: Pin Type: I = Digital Input, O=Digital Output; AI=Analog Input; AO= Analog Output; P=Power Pin; AP=Analog Power.

6.6 Flash Memory Controller (FMC)

6.6.1 Overview

This chip is equipped with 16/32 Kbytes on-chip embedded flash memory for application program memory (APROM) that can be updated through ISP/IAP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip powered on Cortex-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, this chip also provides Data Flash Region, the Data Flash is shared with original program memory and its start address is configurable and defined by user in Config1. The Data Flash size is defined by user application request.

6.6.2 Features

- 16/32 Kbytes application program memory (APROM)
- 4 Kbytes in system programming (ISP) loader program memory (LDROM)
- Programmable Data Flash start address and memory size with 512 bytes page erase unit
- 512 bytes system program memory (SPROM)
- In System Program (ISP)/In Application Program (IAP) to update on chip flash memory

6.7 General Purpose I/O Controller

6.7.1 Overview

The NuMicro Nano112™ series have up to 80 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 80 pins are arranged in 6 ports named with GPIOA, GPIOB, GPIOC, GPIOD, GPIOE and GPIOF. Each one of the 80 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be independently software configured as input, output, and open-drain mode. Each I/O pin has a very weak individual pull-up resistor which is about 110 KΩ~300 KΩ for V_{DD} from 1.8 V to 3.6 V.

6.7.2 Features

- Three I/O modes:
  - Schmitt trigger Input-only with high impendence
  - Push-pull output
  - Open-drain output
- I/O pin configured as interrupt source with edge/level setting
- Enabling the pin interrupt function will also enable the pin wake-up function

6.11 Watchdog Timer Controller

6.11.1 Overview

The purpose of Watchdog Timer is to perform a system reset after the software running into a problem. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up CPU from power-down mode. The watchdog timer includes an 18-bit free running counter with programmable time-out intervals.

6.11.2 Features

- 18-bit free running WDT counter for Watchdog timer time-out interval.
- Selectable time-out interval (2^4 ~ 2^18) and the time-out interval is 104 ms ~ 26.316 s (if WDT_CLK = 10 kHz).
- Reset period = (1 / 10 kHz) * 63, if WDT_CLK = 10 kHz.

8 POWER COMSUMPTION

Part No	Test Condition		VDD	CPU clock	Current
Nano102/112 series	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.89mA 157uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Crystal Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	800uA 67uA/MHz
	Operating Mode: CPU run while(1) in FLASH ROM Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	1.65mA 137uA/MHz
	Idle Mode: CPU stop Clock = 12MHz Internal RC Oscillator Disable all peripheral Set LDO output = 1.6V		3.3V	12 MHz	560uA 46uA/MHz
	RTC + LCD Mode: (RAM retention) (Power down with LXT and LCD enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC and LCD circuit. Without panel loading Set LDO output = 1.6V Only for Nano112 LCD series	InternL C-Type (With internal Charge pump)	3.3V	Stop	9.5uA
		InternL R-Type (With internal resistor ladder) 200kΩ			8.3uA
		InternL R-Type (With internal resistor ladder) 300kΩ			6.4uA
		InternL R-Type (With internal resistor ladder) 400kΩ			5.5uA
		External C-Type (With 0.1uF cap. ladder)			2.5uA
		External R-type (With 1MΩ resister ladder)			3.7uA
	RTC Mode: (RAM retention) (Power down with LXT enable) CPU stop Clock = 32.768KHz Crystal Oscillator Disable all peripheral except RTC circuit Set LDO output = 1.6V		3.3V	Stop	1.5uA
	Power Down Mode: (RAM retention) CPU and all clocks stop Set LDO output = 1.6V		3.3V	Stop	0.65uA
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from wake-up event to first CPU core valid clock)		3.3V	12 MHz	6us
	Wake-Up time from Power Down Mode Clock = Internal 12 MHz RC Oscillator (from interrupt event to interrupt service routine first instruction)		3.3V	12 MHz	7us

9.4.3 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	℃	-
V_{POR}	Reset Voltage		1.6		V	-

9.4.4 Temperature Sensor

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION (supply voltage = 3V)
		MIN.	TYP.	MAX.	UNIT	
Detection Temperature	T_{DET}	-40		+85	^oC	
Operating current	I_{TEMP}	-	5	-	μA	
Gain	V_{TG}	-1.76	-1.68	-1.60	mV/^oC	
Offset	V_{TO}	735	745	755	mV	Tempeature at 0 ^oC

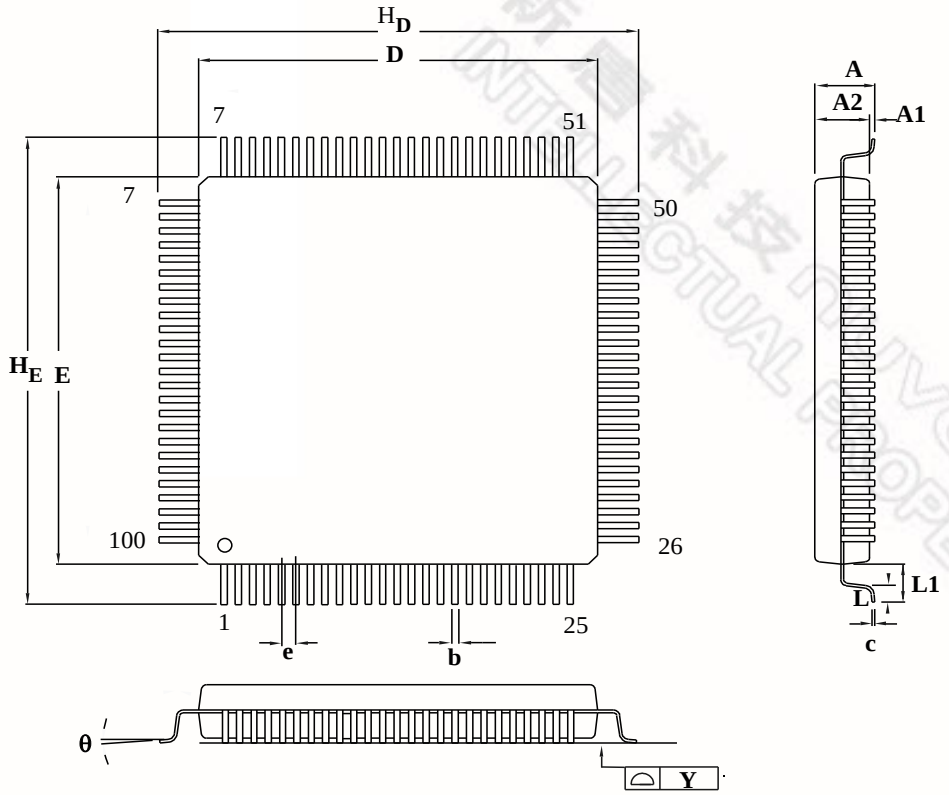
Note: Internal operation voltage comes form LDO.

9.4.5 LCD

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Operating voltage	V_{DD}	1.8	-	3.6	V	
VLCD voltage	V_{LCD34}	-	3.4	-	V	CPUMP_VOL_SET=111, no loading
VLCD voltage	V_{LCD33}	-	3.3	-	V	CPUMP_VOL_SET=110, no loading
VLCD voltage	V_{LCD32}	-	3.2	-	V	CPUMP_VOL_SET=101, no loading
VLCD voltage	V_{LCD31}	-	3.1	-	V	CPUMP_VOL_SET=100, no loading
VLCD voltage	V_{LCD30}	-	3.0	-	V	CPUMP_VOL_SET=011, no loading
VLCD voltage	V_{LCD29}	-	2.9	-	V	CPUMP_VOL_SET=010, no loading
VLCD voltage	V_{LCD28}	-	2.8	-	V	CPUMP_VOL_SET=001, no loading
VLCD voltage	V_{LCD27}	-	2.7	-	V	CPUMP_VOL_SET=000, no loading
Operating current (Include 32.768 KHz crystal OSC and RTC operating)	I_{LCDint}	-	9.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (internal C type, with 0.1uF)
	I_{LCDext}	I_{LCDint}	2.5	-	μA	V_{DD} = 3V, frame rate = 64Hz Without loading (external C type with 0.1uF)

10 PACKAGE DIMENSIONS

10.1 100L LQFP (14x14x1.4 mm footprint 2.0 mm)



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°