Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT
Number of I/O	58
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 7x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/nano112sc2an

2 FEATURES

The equipped features are dependent on the product line and their sub products.

2.1 Nano102 Features – Base Line

- Low Supply Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Operation mode : 150 uA/MHz
  - Power-down mode : 1.5 uA (RTC on, RAM retention)
  - Deep power down mode : 650 nA (RAM retention)
- Fast Wake-Up From Standby Mode : Less than 6 μs
- Core
  - ARM® Cortex™-M0 core running up to 32 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Flash EPROM Memory
  - Runs up to 32 MHz with zero wait state for discontinuous address read access
  - 16/32 Kbytes application program memory (APROM)
  - 4 KB in system programming (ISP) loader program memory (LDROM)
  - Programmable data flash start address and memory size with 512 bytes page erase unit
  - In System Program (ISP)/In Application Program (IAP) to update on-chip Flash EPROM
- SRAM Memory
  - 4/8 Kbytes embedded SRAM
  - Supports DMA mode
- DMA: Supports 5 channels: 4 PDMA channels and one CRC channel
  - PDMA
    - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
    - Supports word boundary address
    - Supports word alignment transfer length in memory-to-memory mode
    - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
    - Supports word/half-word/byte transfer data width from/to peripheral
    - Supports address direction: increment, fixed, and wrap around
  - CRC

enable ADC

- SmartCard (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separates receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 267 ETU)
  - A 24-bit and two 8-bit time-out counter for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detect the card is removal
  - Supports UART mode (full-duplex)
- ACMP
  - Suuports up to 2 analog comparators
  - Analog input voltage range: 0 ~ AV_{DD}
  - Supports Hysteresis function
  - Two analog comparators with optional internal reference voltage input at negative end
- Wake-up source
  - Support RTC, WDT, I²C, Timer, UART, SPI, BOD, GPIO
- LCD
  - LCD driver for up to 4 COM x 36 SEG or 6 COM x 34 SEG
  - Supports Static,1/2 bias and 1/3 bias voltage
  - Six display modes; Static, 1/2 duty, 1/3 duty, 1/4 duty, 1/5 duty and 1/6 duty.
  - Selectable LCD frequency by frequency divider
  - Configurable frame frequency
  - Internal Charge pump, adjustable contrast adjustment
  - Configurable Charge pump frequency
  - Blinking capability
  - Supports R-type/C-type/External C-type method
  - Configurable internal R-ladder resistor value (200K/300K/400K)
  - LCD frame interrupt
- One built-in temperature sensor with 1℃ resolution

4.2.2 NuMicro™ Nano112 LCD Line Selection Guide

Part No.	Flash	SRAM	Data Flash	ISP ROM	I/O	Timer (32-bit)	Connectivity			Comp	PWM (16-bit)	ADC (12-bit)	RTC	IRC 10KHz / 12MHz / 16MHz	PDMA	LCD	ISO-7816-3	ISP ICP	Package	Maximum Operating Temp. Range (°C)
							UART	SPI	I²C											
NANO112LB1AN	16K	4K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112LC2AN	32K	8K	Configurable	4K	up to 40	4	4	2	2	2	4	7	√	√	4	4x20, 6x18	2	√	LQFP48	-40 to +85
NANO112SB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112SC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64	-40 to +85
NANO112RB1AN	16K	4K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112RC2AN	32K	8K	Configurable	4K	up to 58	4	4	2	2	2	4	7	√	√	4	4x32, 6x30	2	√	LQFP64*	-40 to +85
NANO112VC2AN	32K	8K	Configurable	4K	up to 80	4	4	2	2	2	4	8	√	√	4	4x36, 6x34	2	√	LQFP100	-40 to +85

LQFP48: 7x7mm
LQFP64: 7x7mm
LQFP64*: 10x10mm

Pin No.			Pin Name	Pin Type	Description
64-pin	48-pin	32-pin			
			AD0	AI	ADC analog input0
46	35		PA.1	I/O	General purpose digital I/O pin
			AD1	AI	ADC analog input1
			ACMP0_P3	AI	Comparator0 P-end input3
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
47	36		PA.2	I/O	General purpose digital I/O pin
			SC0_CLK	O	SmartCard0 clock pin (SC0_UART_TXD)
			INT0	I	External interrupt0 input pin
			AD2	AI	ADC analog input2
			ACMP0_P2	AI	Comparator0 P-end input2
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
48	37		PA.3	I/O	General purpose digital I/O pin
			SC0_DAT	I/O	SmartCard0 DATA pin(SC0_UART_RXD)
			INT1	I	External interrupt 1
			AD3	AI	ADC analog input3
			ACMP0_P1	AI	Comparator0 P-end input1
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
49	38	25	PA.4	I/O	General purpose digital I/O pin
			SC0_CD	I	SmartCard0 card detect pin
			AD4	AI	ADC analog input4
			ACMP0_P0	AI	Comparator0 P-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
50	39	26	PA.5	I/O	General purpose digital I/O pin
			SPI1_SS0	I/O	SPI1 1st slave select pin
			I2C1_SDA	I/O	I^2C1 data I/O pin
			SC0_PWR	O	SmartCard0 Power pin
			AD5	AI	ADC analog input5
			ACMP0_N	AI	Comparator0 N-end input0
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
51	40		PA.6	I/O	General purpose digital I/O pin
			ACMP0_CHDIS	O	Comparator0 charge/discharge path
			SC0_RST	O	SmartCard0 RST pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			LCD_DH2	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH1	**I/O**	PWM0 Channel1 output
			TC0	**I**	Timer0 capture input
44	31		PD.12	**I/O**	General purpose digital I/O pin
			CLK_Hz	**O**	1, 1/2, 1/4, 1/8, 1/16 Hz clock output
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 100-pin
			LCD_DH1	**O**	LCD external capacitor pin of charge pump circuit at 64-pin
			PWM0_CH0	**I/O**	PWM0 Channel0 output
			TM1	**I/O**	Timer1 external counter input
			FCLK0	**O**	Frequency Divider0 output pin
45					NC
46	32	21	V_{LCD}	**P**	LCD power supply pin
47					NC
48	33	22	PD.13	**I/O**	General purpose digital I/O pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 100-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 64-pin
			LCD_V1	**I**	Input pin of the 1st most positive LCD level at 48-pin
			INT1	**I**	External interrupt 1 input pin
49	34	23	PD.14	**I/O**	General purpose digital I/O pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 100-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 64-pin
			LCD_V2	**I**	Input pin of the 2nd most positive LCD level at 48-pin
50	35	24	PD.15	**I/O**	General purpose digital I/O pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 100-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 64-pin
			LCD_V3	**I**	Input pin of the 3rd most positive LCD level at 48-pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
84			PA.8	**I/O**	General purpose digital I/O pin
			SC0_PWR	**O**	SmartCard0 Power pin
85			PA.9	**I/O**	General purpose digital I/O pin
			SC0_RST	**O**	SmartCard0 RST pin
86			PA.10	**I/O**	General purpose digital I/O pin
			SC0_CLK	**O**	SmartCard0 clock pin (SC0_UART_TXD)
87			PA.11	**I/O**	General purpose digital I/O pin
			SC0_DAT	**I/O**	SmartCard0 DATA pin(SC0_UART_RXD)
			STADC	**I**	ADC external trigger input.
88	56	45	PA.12	**I/O**	General purpose digital I/O pin
			LCD_SEG19	**O**	LCD segment output 19 at 48-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			SPI1_MOSI0	**I/O**	SPI1 1st MOSI (Master Out, Slave In) pin
			I2C0_SCL	**I/O**	I^2C 0 clock pin
			ACMP1_P	**AI**	Comparator1 P-end input
89	57	46	PA.13	**I/O**	General purpose digital I/O pin
			LCD_SEG18	**O**	LCD segment output 18 at 48-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			SPI1_MISO0	**I/O**	SPI1 1st MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			ACMP1_N	**AI**	Comparator1 N-end input
90	58	47	PA.14	**I/O**	General purpose digital I/O pin
			ACMP0_CHDIS	**O**	Comparator0 charge/discharge path
			LCD_SEG31	**O**	LCD segment output 31 at 64-pin
			LCD_SEG17	**O**	LCD segment output 17 at 48-pin
			SPI1_CLK	**I/O**	SPI1 serial clock pin
			I2C1_SCL	**I/O**	I^2C1 clock pin
91	59	48	PA.15	**I/O**	General purpose digital I/O pin
			LCD_SEG30	**O**	LCD segment output 30 at 64-pin
			LCD_SEG16	**O**	LCD segment output 16 at 48-pin
			SPI1_SS0	**I/O**	SPI1 1st slave select pin

Pin No.			Pin Name	Pin Type	Description
100-pin	64-pin	48-pin			
			I2C1_SDA	**I/O**	I^2C1 data I/O pin
			ACMP1_OUT	**O**	Comparator1 output
			TC3	**I**	Timer3 capture input
92	60		PB.0	**I/O**	General purpose digital I/O pin
			LCD_SEG29	**O**	LCD segment output 29 at 64-pin
			UART0_TXD	**O**	UART0 Data transmitter output pin (This pin could be modulated with PWM0 output.)
			FCLK1	**O**	Frequency Divider1 output pin
93	61		PB.1	**I/O**	General purpose digital I/O pin
			LCD_SEG28	**O**	LCD segment output 28 at 64-pin
			UART0_RXD	**I**	UART0 Data receiver input pin
			TC2	**I**	Timer 2 capture input
			INT1	**I**	External interrupt1 input pin
94	62		PB.2	**I/O**	General purpose digital I/O pin
			LCD_SEG27	**O**	LCD segment output 27 at 64-pin
			UART0_RTSn	**O**	UART0 Request to Send output pin
			SPI1_MOSI1	**I/O**	SPI1 2nd MOSI (Master Out, Slave In) pin
			I2C0_SCL	**O**	I^2C0 clock pin
			TM3	**I/O**	Timer3 external counter input or Timer3 toggle out.
95	63		PB.3	**I/O**	General purpose digital I/O pin
			LCD_SEG26	**O**	LCD segment output 26 at 64-pin
			UART0_CTSn	**I**	UART0 Clear to Send input pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
			I2C0_SDA	**I/O**	I^2C0 data I/O pin
			TM2	**I/O**	Timer2 external counter input or Timer2 toggle out.
96			V_{DD}	**P**	Power supply for I/O ports and LDO source
97			V_{SS}	**G**	Ground for digital circuit
98			PB.4	**I/O**	General purpose digital I/O pin
			UART1_RTSn	**O**	UART1 Request to Send output pin
			SPI1_MISO1	**I/O**	SPI1 2nd MISO (Master In, Slave Out) pin
99			PB.5	**I/O**	General purpose digital I/O pin
			LCD_SEG35	**O**	LCD segment output 35 at 100-pin

5.2 Nano112 Block Diagram

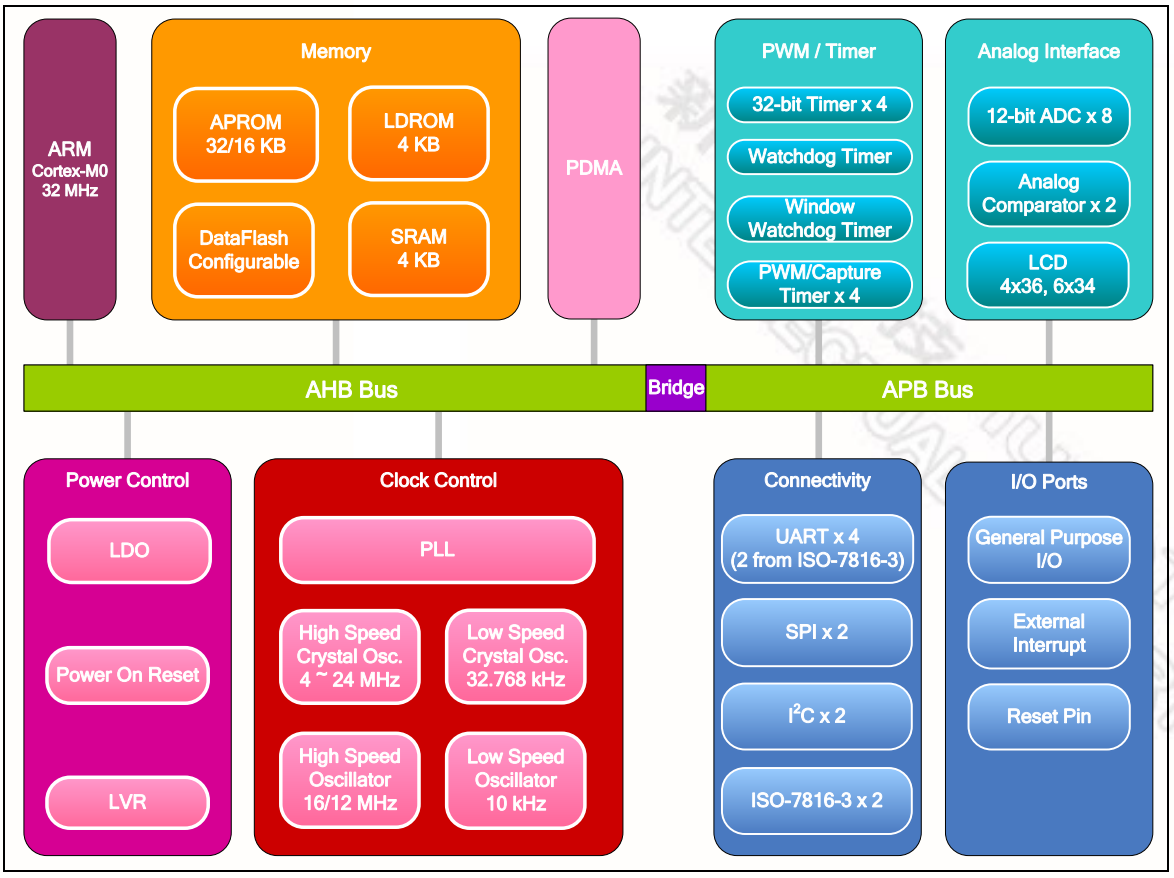


Figure 5-2 NuMicro™ Nano112 Block Diagram

6.3 Nested Vectored Interrupt Controller (NVIC)

6.3.1 Overview

The Cortex-M0 provides an interrupt controller as an integral part of the exception mode, named as “Nested Vectored Interrupt Controller (NVIC)”. It is closely coupled to the processor kernel and provides following features:

6.3.2 Features

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in “Handler Mode”. This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one’s priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers “PC, PSR, LR, R0~R3, R12” to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports “Tail Chaining” which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports “Late Arrival” which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the “ARM® Cortex™-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.8.2 Features

- Supports four PDMA channels (CH1 ~ CH4) and one CRC channel. Each PDMA channel can support a unidirectional transfer
- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Hardware round robin priority scheme. DMA channel 1 has the highest priority and channel 4 has the lowest priority
- PDMA
  - Peripheral-to-memory, memory-to-peripheral, and memory-to-memory transfer
  - Supports word boundary address
  - Supports word alignment transfer length in memory-to-memory mode
  - Supports word/half-word/byte alignment transfer length in peripheral-to-memory and memory-to-peripheral mode
  - Supports word/half-word/byte transfer data width from/to peripheral
  - Supports address direction: increment, fixed, and wrap around
  - Supports time-out function in all channel
- Cyclic Redundancy Check (CRC)
  - Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
    - CRC-CCITT: X16 + X12 + X5 + 1
    - CRC-8: X8 + X2 + X + 1
    - CRC-16: X16 + X15 + X2 + 1
    - CRC-32: X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1
  - Programmable seed value
  - Supports programmable order reverse setting for input data and CRC checksum
  - Supports programmable 1's complement setting for input data and CRC checksum
  - Supports CPU mode or DMA transfer mode
  - Supports 8/16/32-bit of data width in CRC CPU mode
    - 8-bit write mode: 1-AHB clock cycle operation
    - 16-bit write mode: 2-AHB clock cycle operation
    - 32-bit write mode: 4-AHB clock cycle operation
  - Supports byte alignment transfer length in CRC DMA mode

6.9 Timer Controller

6.9.1 Overview

This chip is equipped with four timer modules including TIMER0, TIMER1, TIMER2 and TIMER3, which allow user to easily implement a counting scheme or timing control for applications. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

6.9.2 Features

- Independent Clock Source for each Timer (TMRx_CLK, x= 0, 1,2,3)
- Time-out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Counting cycle time = (1 / TMRx_CLK) * (2^8) * (2^24)
- Internal 8-bit pre-scale counter
- Internal 24-bit up counter is readable through TDR (Timer Data Register)
- Supports One-shot, Periodic, Output Toggle and Continuous Counting Operation mode
- Supports external pin capture for interval measurement
- Supports external pin capture for timer counter reset
- Supports Inter-Timer trigger
- Supports event generator in TIMER 0 and TIMER 2 to generate event to TIMER1 and TIMER3, respectively.
- Supports Internal trigger event to ADC and PDMA

6.10.2 Features

6.10.2.1 PWM Function:

- PWM controllers has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators
- Up to 4 PWM channels or 2 PWM paired channels
- Up to 16 bits PWM counter width
- PWM Interrupt request synchronous with PWM period
- Single-shot or Continuous mode
- Two Dead-Zone generators

6.10.2.2 Capture Function:

- Timing control logic shared with PWM timer.
- 4 Capture input channels shared with 4 PWM output channels.
- Each channel supports one rising latch register CRL (PWM_CRL0[15:0]), one falling latch register CFL (PWM_CFL0[15:0]) and Capture interrupt flag CAPIF0 (PWM_CAPINTSTS[0]).
- Four 16-bit counters for four capture channels or two 32-bit counter for two capture channels when cascade is enabled: when CH01CASKEN (PWM_CAPCTL[13]) is set, the original 16-bit counter of channel 1 will combine with channel 0's 16 bit counter for channel 0 input capture counting and so does CH23CASKEN(PWM_CAPCTL[29]) for channel 2, 3
- Supports PDMA transfer function for PWM channel 0, 2

6.16 I²C

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. Serial, 8-bit oriented bi-directional data transfers can be made up to 1 Mbps.

Data is transferred between a Master and a Slave synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8-bit long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte.

A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL.

The controller's on-chip I²C logic provides the serial interface that meets the I²C bus standard mode specification. The I²C controller handles byte transfers autonomously. Pull up resistor is needed for I²C operation as these are open drain pins.

The I²C controller is equipped with two slave address registers. The contents of the registers are irrelevant when I²C is in Master mode. In the Slave mode, the seven most significant bits must be loaded with the user's own slave address. The I²C hardware will react if the contents of I2CADDR are matched with the received slave address.

This controller supports the "General Call (GC)" function. If the GCALL (I2CSADDR[0]) bit is set this controller will respond to General Call address (00H). Clear GC bit to disable general call function. When GCALL bit is set and the I²C is in Slave mode, it can receive the general call address which is equal to 00H after master sends general call address to the I²C bus, then it will follow status of GC mode. If it is in Master mode, the ACK bit must be cleared when it sends general call address of 00H to the I²C bus.

The I²C-bus controller supports multiple address recognition with two address mask register. When the bit in the address mask register is set to one, it means the received corresponding address bit is don't-care. If the bit is set to 0, that means the received corresponding register bit should be exact the same as address register.

6.16.2 Features

- Supports two I2C channels and both of them can acts as Master or Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- One built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows.
- Programmable clock divider allows versatile rate control
- Supports 7-bit addressing mode

6.20 Analog Comparator Controller (ACMP)

6.20.1 Overview

The Nano112 series contains two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes. The comparator ACMP0 can be used as normal comparator or it can emulate ADC function. The comparator ACMP1 can be used as normal comparator only.

6.20.2 Features

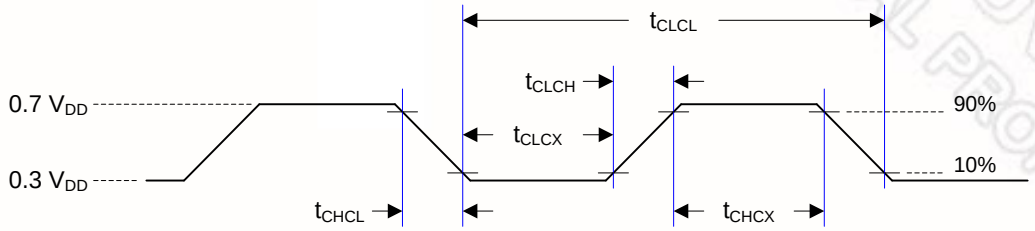
- Analog input voltage range: 0 ~ AV_{DD}
- Supports hysteresis function
- Supports wake-up function
- Comparator ACMP0 supports
  - 4 positive sources(ACMP0_Px)
    - PA.1, PA.2, PA.3, or PA.4
  - 4 negative sources
    - PA.5 (ACMP0_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP1 supports
  - 1 positive source
    - PA.12(ACMP1_P)
  - 4 negative sources
    - PA.13(ACMP1_N)
    - Comparator Reference Voltage (CRV)
    - Int_V_{REF}
    - AGND
- Comparator ACMP0 supports three operation modes:
  - Normal Comparator mode
  - Single Slope ADC mode: Resistance measurement (e.g. PTC, NTC, PT1000)
    - Supports to measure 7 channels resistor
  - Sigma-Delta ADC mode
    - Supports up to 4 channel voltage input from ACMP0_Px

Operating Current Idle Mode HCLK =16 MHz V_{LDO1}=1.6 V	$I_{IDLE131}$		4.2		mA	3.3 V	X	16 MHz	X	V
	$I_{IDLE141}$		0.7		mA	3.3 V	X	16 MHz	X	X
	$I_{IDLE151}$		4.1		mA	1.8 V	X	16 MHz	X	V
	$I_{IDLE161}$		0.7		mA	1.8 V	X	16 MHz	X	X
Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	$I_{IDLE132}$		2.9		mA	3.3 V	X	12 MHz	X	V
	$I_{IDLE142}$		0.6		mA	3.3 V	X	12 MHz	X	X
	$I_{IDLE152}$		2.9		mA	1.8 V	X	12 MHz	X	V
	$I_{IDLE162}$		0.6		mA	1.8 V	X	12 MHz	X	X
Operating Current Idle Mode HCLK =12 MHz V_{LDO1}=1.6 V	I_{IDLE13}		2.8		mA	3.3 V	12 MHz	X	X	V
	I_{IDLE14}		0.8		mA	3.3 V	12 MHz	X	X	X
	I_{IDLE15}		2.8		mA	1.8 V	12 MHz	X	X	V
	I_{IDLE16}		0.8		mA	1.8 V	12 MHz	X	X	X
Operating Current Idle Mode HCLK =4 MHz V_{LDO1}=1.6 V	I_{IDLE17}		1.0		mA	3.3 V	4 MHz	X	X	V
	I_{IDLE18}		0.3		mA	3.3 V	4 MHz	X	X	X
	I_{IDLE19}		1.0		mA	1.8 V	4 MHz	X	X	V
	I_{IDLE20}		0.3		mA	1.8 V	4 MHz	X	X	X
Operating Current Idle Mode HCLK =32.768 kHz V_{LDO1}=1.6 V	I_{IDLE21}		96		uA	V_{DD}	LXT (kHz)	HIRC	PLL	All digital module
						3.3 V	32.768	X	X	V
	I_{IDLE22}		90		uA	3.3 V	32.768	X	X	X
	I_{IDLE23}		92		uA	1.8 V	32.768	X	X	V
	I_{IDLE24}		86		uA	1.8 V	32.768	X	X	X
Operating Current Idle Mode HCLK =10 kHz V_{LDO1}=1.6 V	I_{IDLE25}		90		uA	V_{DD}	HXT/LXT	LIRC (kHz)	PLL	All digital module
						3.3 V	X	10	X	V
	I_{IDLE26}		89		uA	3.3 V	X	10	X	X
	I_{IDLE27}		86		uA	1.8 V	X	10	X	V
	I_{IDLE28}		84		uA	1.8 V	X	10	X	X
Standby Current Power-down Mode V_{LDO1}=1.6 V	I_{PWD1}		0.65		uA	V_{DD}	HXT/HIRC PLL	LXT (kHz)	RTC	RAM retension
						3.3 V	X	X	X	V
	I_{PWD2}		0.65		uA	1.8 V	X	X	X	V
	I_{PWD3}		1.5		uA	3.3 V	X	32.768	V	V
	I_{PWD4}		1.5		uA	1.8 V	X	32.768	V	V

9.3 AC Electrical Characteristics

9.3.1 External Input Clock

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Clock High Time	t_{CHCX}	10	-		nS	
Clock Low Time	t_{CLCX}	10	-		nS	
Clock Rise Time	t_{CLCH}	2	-	15	nS	
Clock Fall Time	t_{CHCL}	2	-	15	nS	



Note: Duty cycle is 50%.

9.3.2 External 4~24 MHz XTAL Oscillator

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{HXT}	4	12	24	MHz	VDD = 1.8V ~ 3.6V
Temperature	T_{HXT}	-40	-	+85	°C	
Operating current	I_{HXT}		0.3		mA	VDD = 3.0V

9.3.2.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
4MHz ~ 24 MHz	20pF	20pF	without

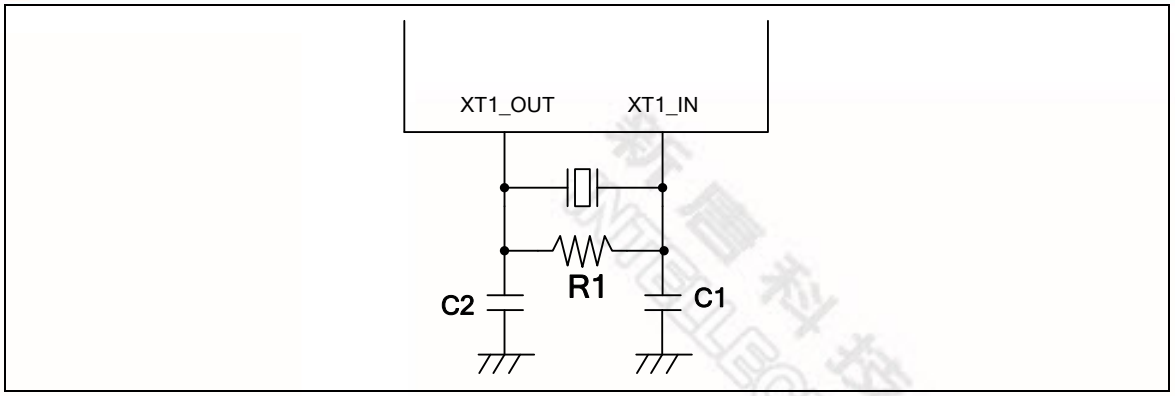


Figure 9-1 Typical Crystal Application Circuit

9.3.3 External 32.768 kHz Crystal

PARAMETER	SYM.	SPECIFICATIONS				TEST CONDITION
		MIN.	TYP.	MAX.	UNIT	
Oscillator frequency	f_{LXT}		32.768		kHz	VDD = 1.8V ~ 3.6V
Temperature	T_{LXT}	-40	-	+85	°C	
Operating current	I_{LXT}		1		μA	VDD = 3.0V

9.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C3	C4	R2
32.768 kHz	20pF	20pF	without

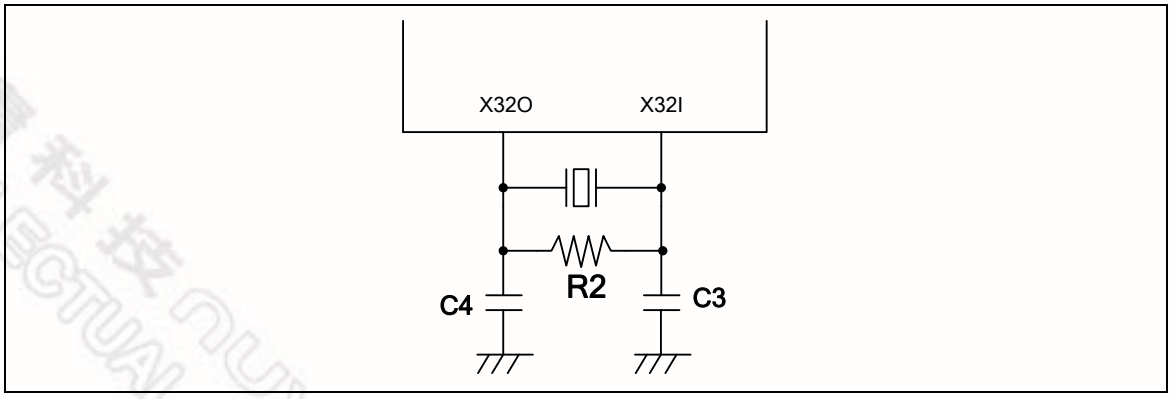
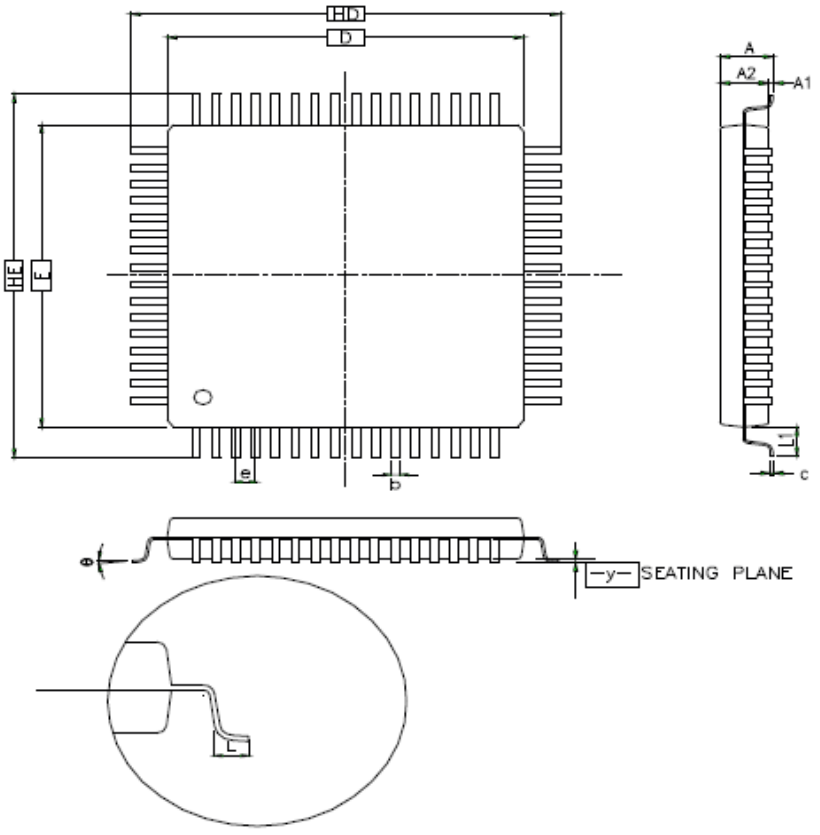


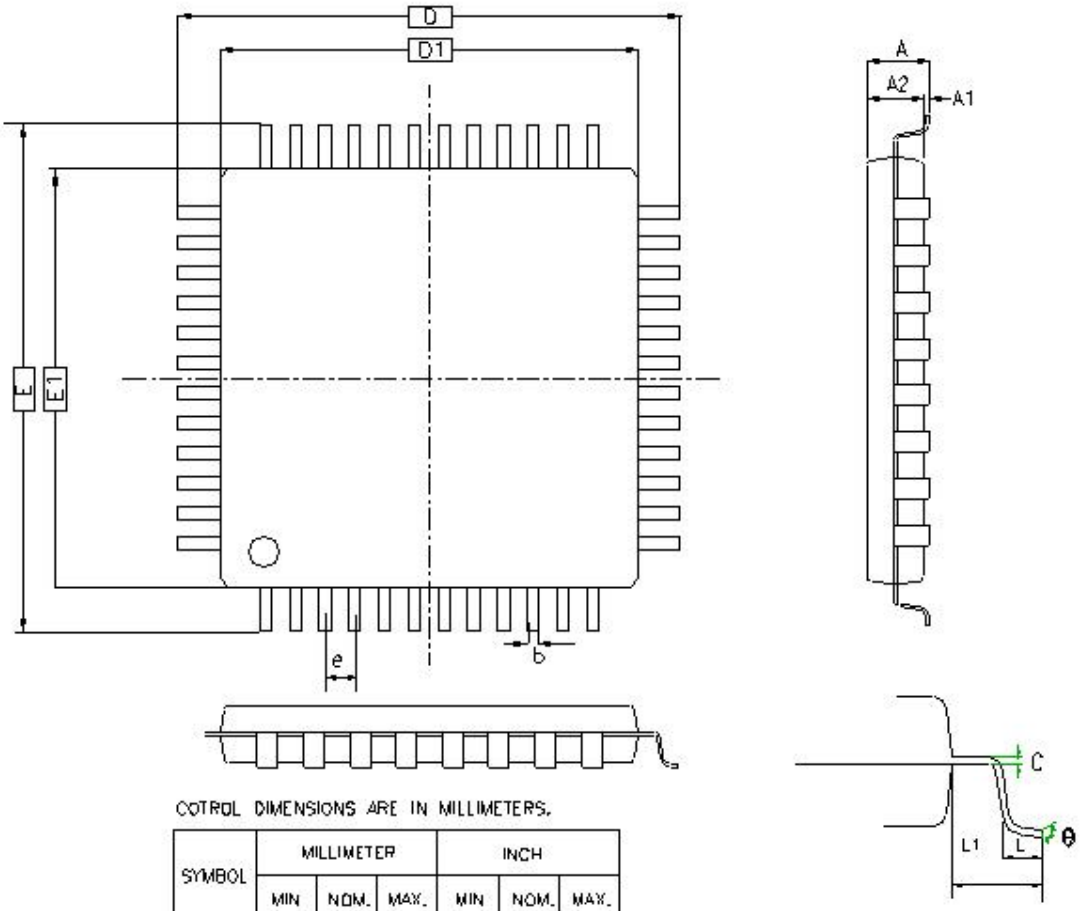
Figure 9-2 Typical Crystal Application Circuit

10.2 64R LQFP(10x10x1.4 mm footprint 2.0 mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.008	0.011	0.17	0.20	0.27
c	0.004	—	0.008	0.09	—	0.20
D	—	0.393	—	—	10.00	—
E	—	0.393	—	—	10.00	—
e	—	0.020	—	—	0.50	—
H_D	—	0.472	—	—	12.00	—
H_E	—	0.472	—	—	12.00	—
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
y	—	0.004	—	—	0.10	—
θ	0°	3.5°	7°	0°	3.5°	7°

10.4 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.260
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

11 REVISION HISTORY

Date	Revision	Description
2014.03.28	1.00	1. Initial release
2014.05.08	1.01	1. Modified some typos and format.
2014.09.02	1.02	1. Modified the pin description for LCD_Vx in section 4.4. 2. Modified all PWM1 group to PWM0 group in section 6.10. 3. Modified “PWM1 channel 2 and 3” to “PWM0 channel 2 and 3” in section 6.10. 4. Modified some typos and format.
2015.01.15	1.03	1. Updated ADC channel number in NANO102 feature list in Chapter 2. 2. Corrected typo in NANO102 64-pin sequence in section 4.4. 3. Updated all power related pins from “VDD, VSS, AVDD, AVSS, VTEMP and VLCD” to “V_{DD}, V_{SS}, AV_{DD}, AV_{SS}, V_{TEMP} and V_{LCD}” in the Datashhet.