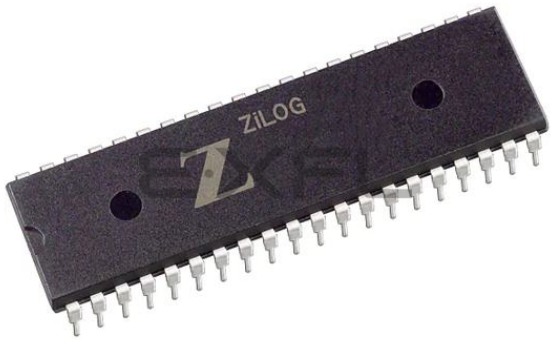

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	32
Program Memory Size	16KB (16K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c6116pscr3353

GENERAL DESCRIPTION (Continued)

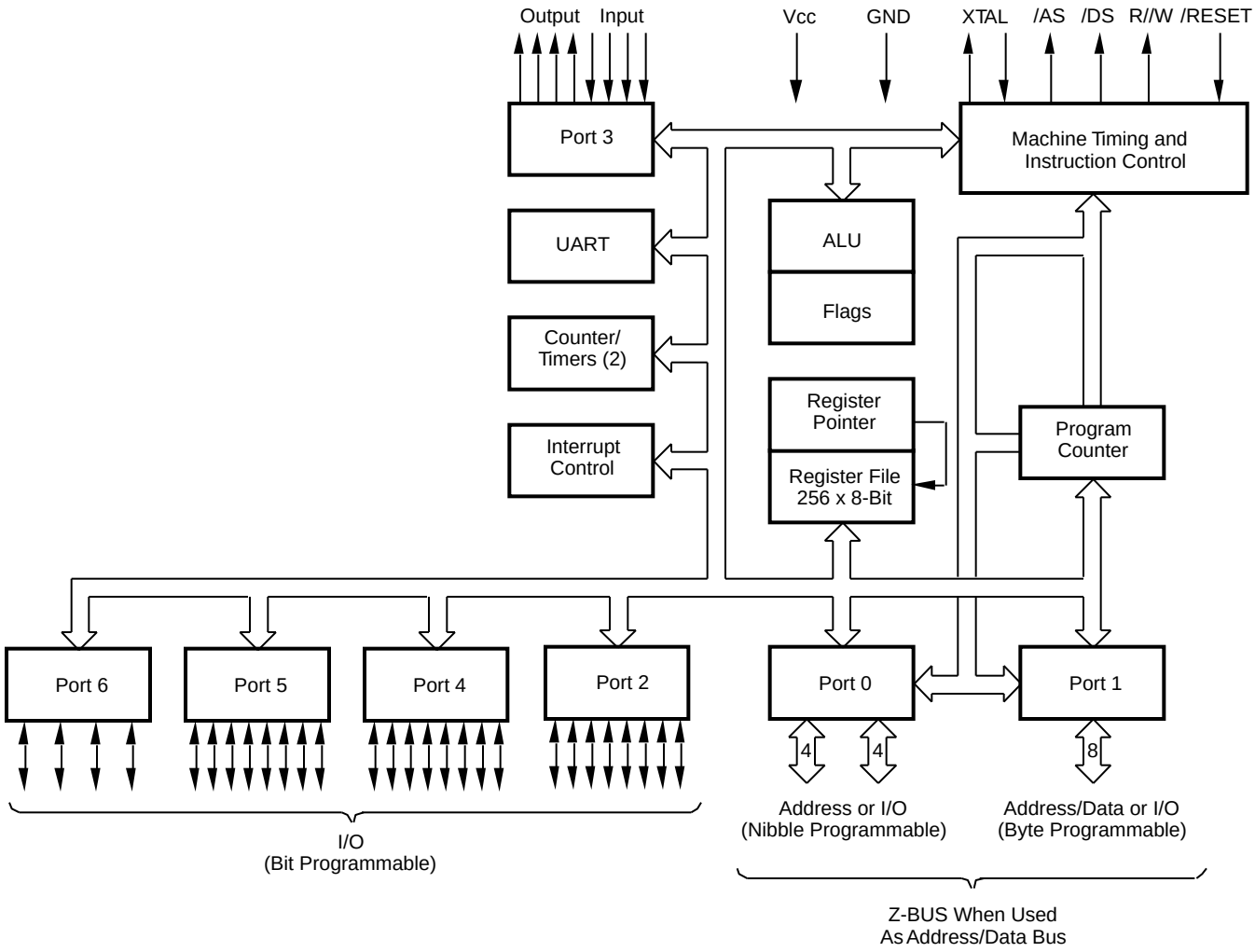


Figure 3. Z86C96 Functional Block Diagram

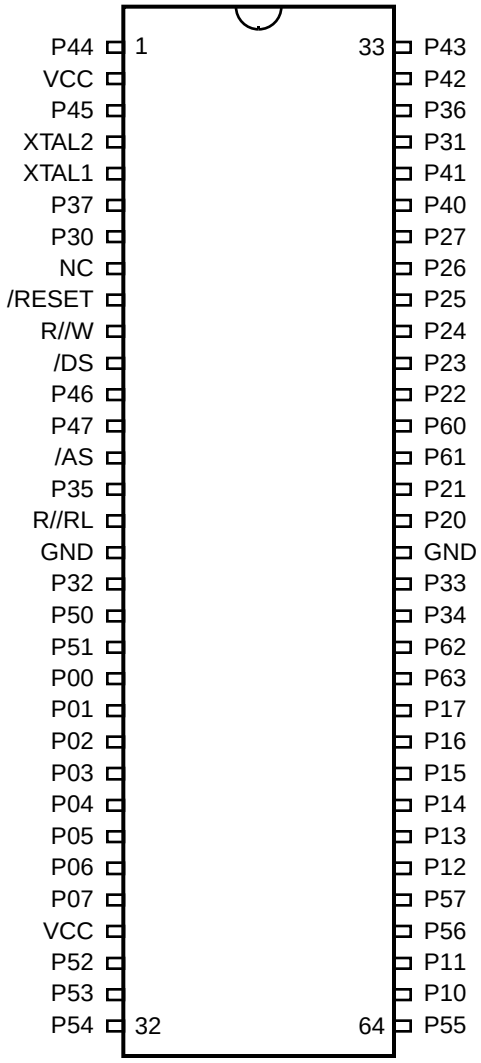


Figure 6. Z86C62/C96 64-Pin DIP Pin Assignments

Table 3. Z86C62/C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R//RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

DC ELECTRICAL CHARACTERISTICS

Z86C61/62/96

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC} – 100 mV		V_{CC} – 100 mV		V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0_V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	VRL = 0 V
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current		40		40	30	mA	[1] @ 20 MHz
I_{CC1}	Standby Current		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}

Notes:

1. All inputs driven to either 0V or V_{CC}, outputs floating.
2. V_{CC} = 3.0V to 3.6V
3. V_{CC} = 4.5V to 5.5V

DC ELECTRICAL CHARACTERISTICS (Continued)

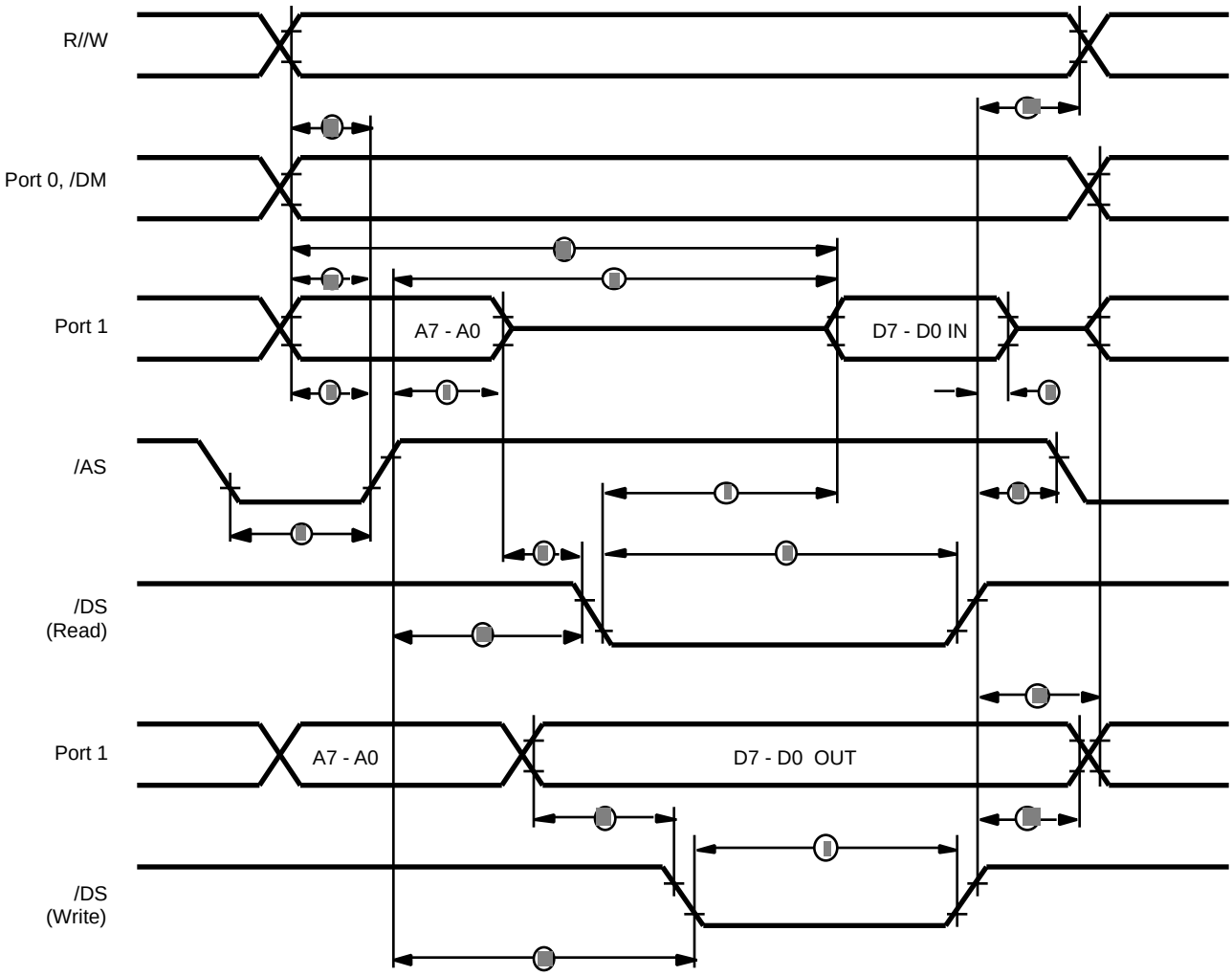


Figure 9. External I/O or Memory Read/Write

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (16 MHz)

			T_A = 0°C to +70°C 16 MHz		T_A = -40°C to +105°C 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	1,2,3
4	TwAS	/AS Low Width	40		40		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	80		80		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	2,3
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	2,3
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	2,3

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Table 5. Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67

Table 5. Clock Dependent Formulas

Number	Symbol	Equation
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

Additional Timing Diagram

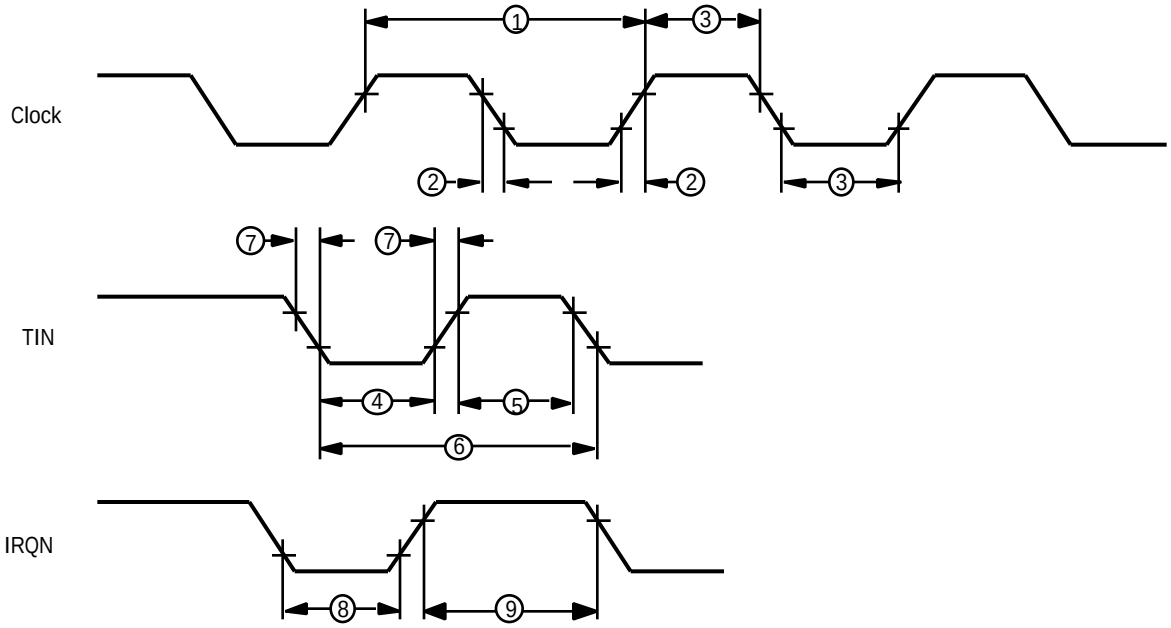


Figure 10. Additional Timing

AC CHARACTERISTICS

Handshake Timing Diagrams

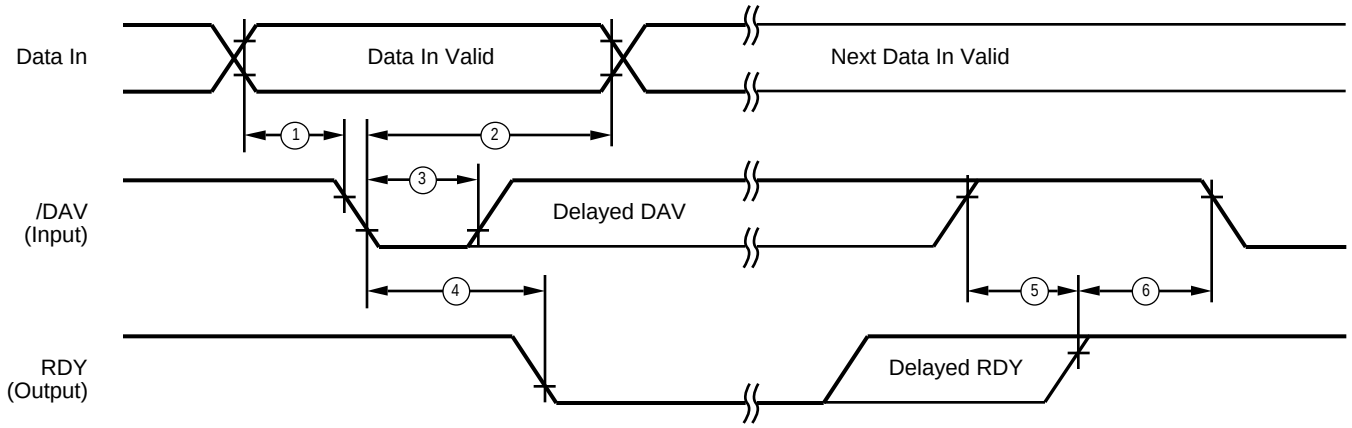


Figure 11. Input Handshake Timing

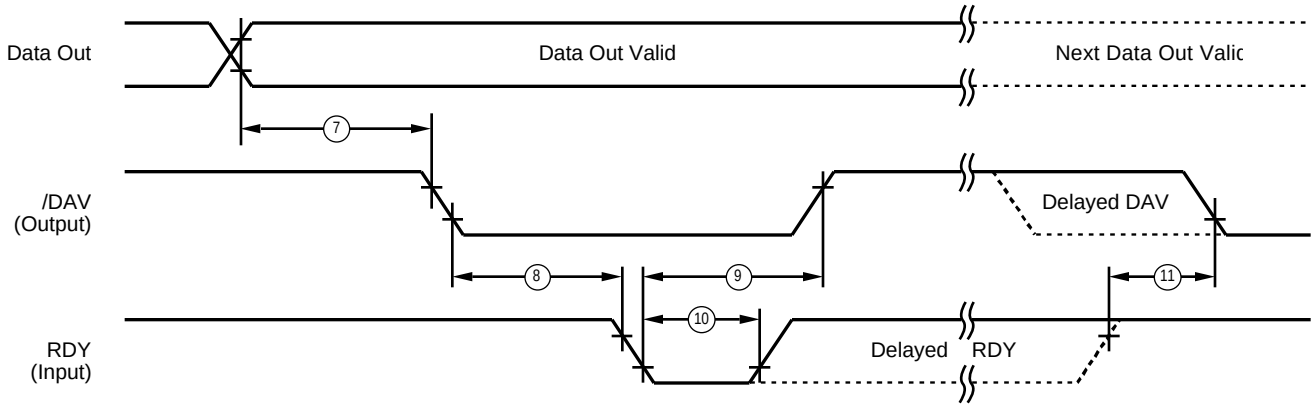


Figure 12. Output Handshake Timing

PIN FUNCTIONS

R//RL (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (Note: When left unconnected or pulled High to VCC the part functions as a normal Z86C61/62 ROM version.) This pin is only available on the 44-pin version of the Z86C61, and both versions of the Z86C62.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address out-put is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C61/62/96 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until VCC is stable, whichever is longer.

/P0DS Port 0 Data Strobe (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

/P1DS Port 1 Data Strobe (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

/DTIMERS Disable Timers (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

SCLK (output). System clock pin.

/SYNC Instruction SYNC Signal (output, active Low). This signal indicates the last clock of the current executing instruction.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 14).

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 15).

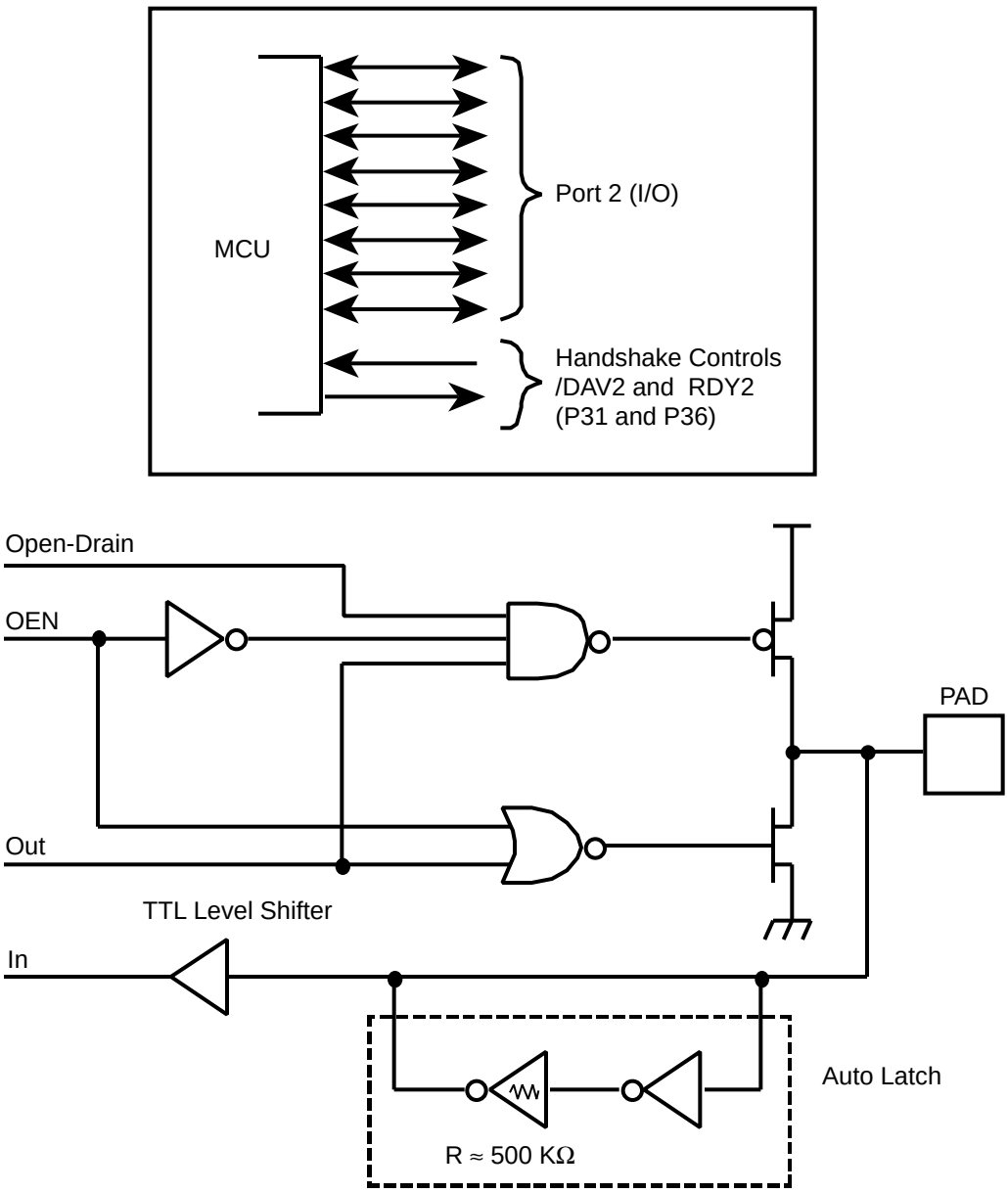


Figure 15. Port 2 Configuration

Port 3 (P37-P30). Port 3 is an 8-bit, CMOS-compatible four-fixed input and four-fixed output port. These eight I/O lines have four-fixed (P33-P30) input and four-fixed (P37-P34) output ports. Port 3, when used as serial I/O, are programmed as serial in and serial out, respectively (Figure 16).

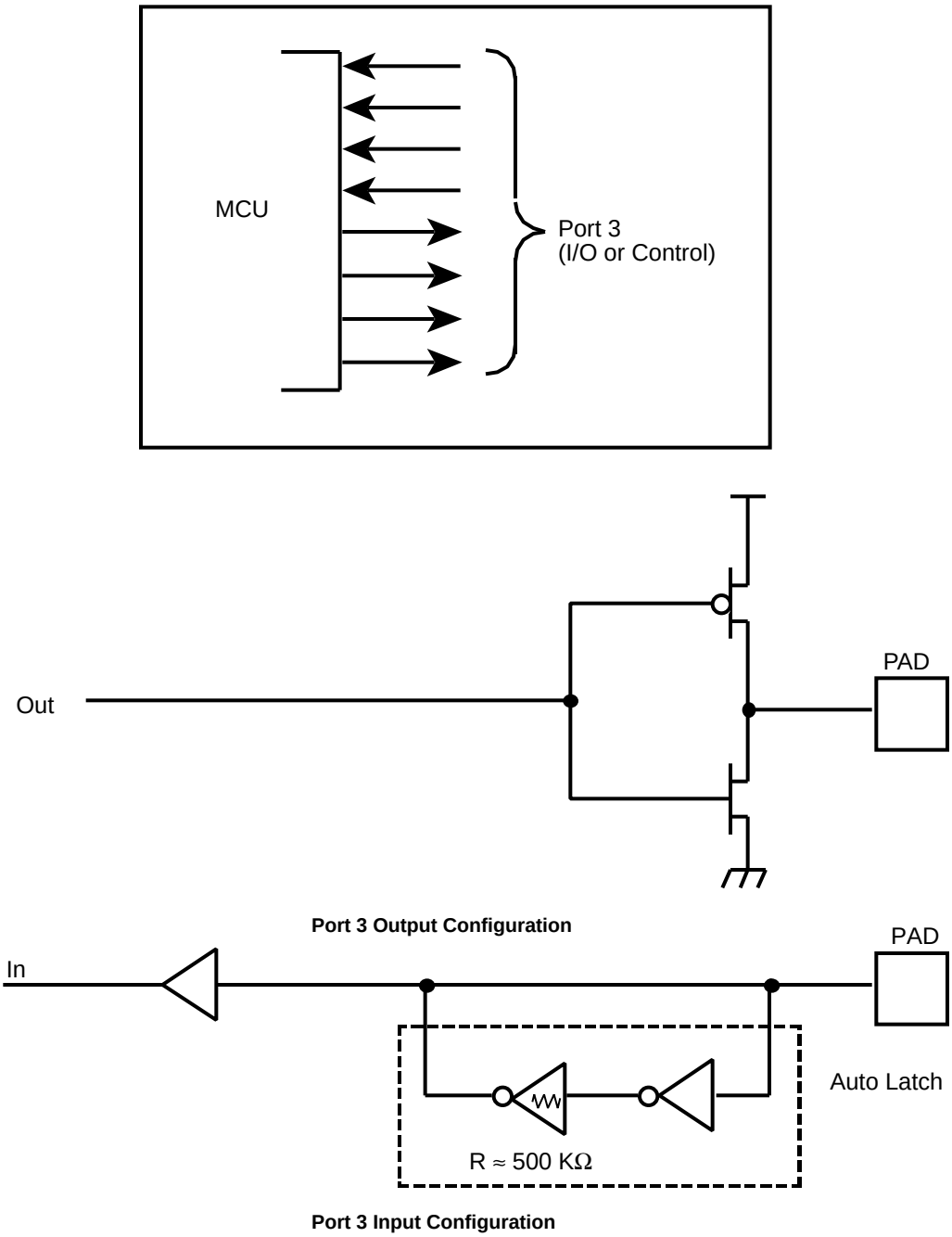


Figure 16. Port 3 Configuration

PIN FUNCTIONS (Continued)

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Table 6. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

Uart Operation

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C61/62/96 automatically adds a start bit and two stop bits to transmitted data (Figure 17). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Note: UART function is only available in standard timing mode (i.e., P01M D5 = 0).

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 18). Port address (F)02.

Port 5 (P57-P50). Same as Port 4. Port address (F)04.

Port 6 (P63-P60). Same as Port 4. (Note: this is a 4-bit port, bits D3-D0.) Port address (F)07.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

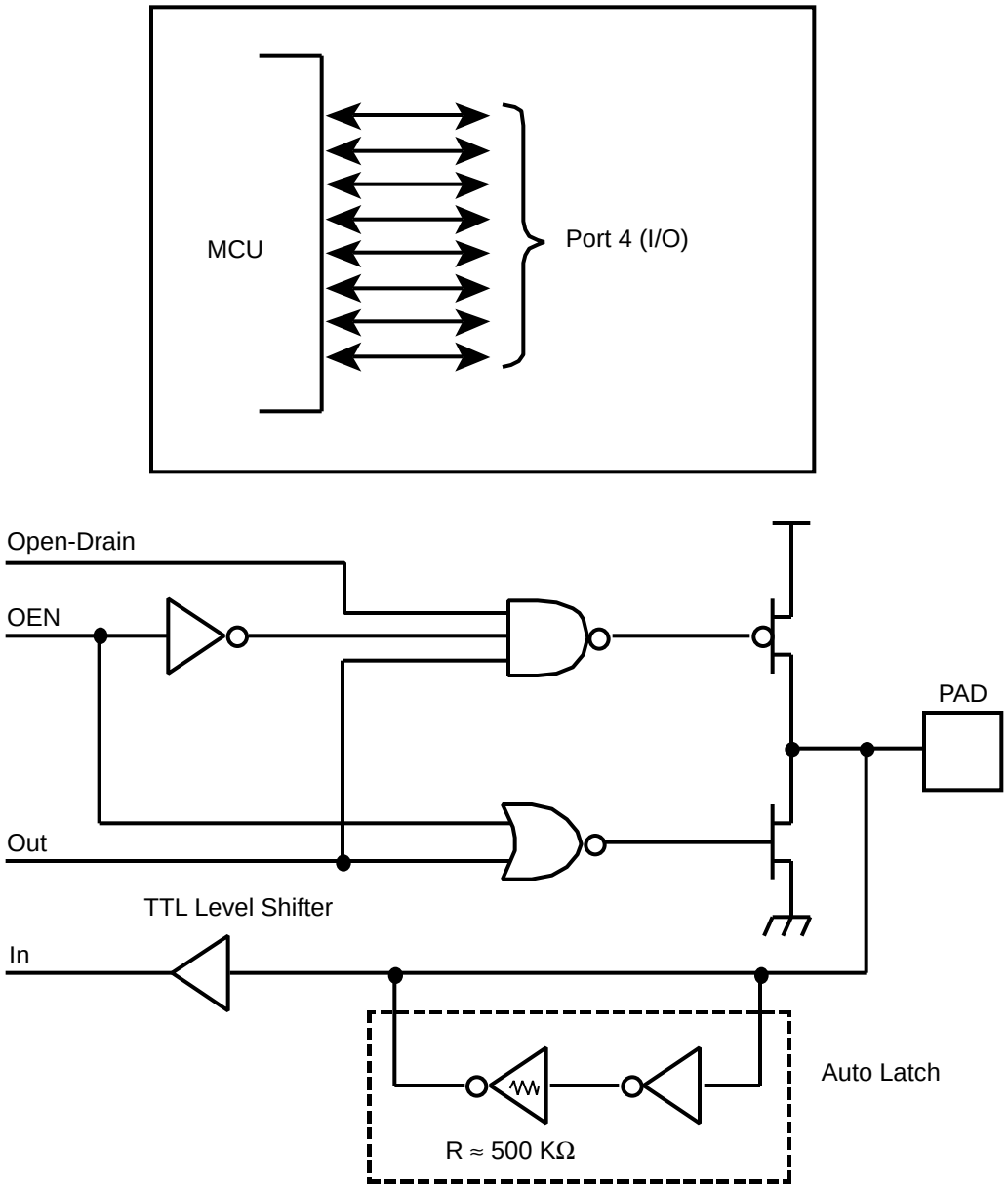


Figure 18. Port 4 Configuration

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C61/62 can address up to 48 KB of external program memory (Figure 19). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 16383 consists of on-chip ROM. At addresses 16384 and greater, the Z86C61/62 executes external program memory fetches. The Z86C96, and the Z86C61/62 in ROMless mode, can address up to 64 KB of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory (/DM). The ROM version can address up to 48 KB of external data memory space beginning at location 16384. The ROMless version can address up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 20). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

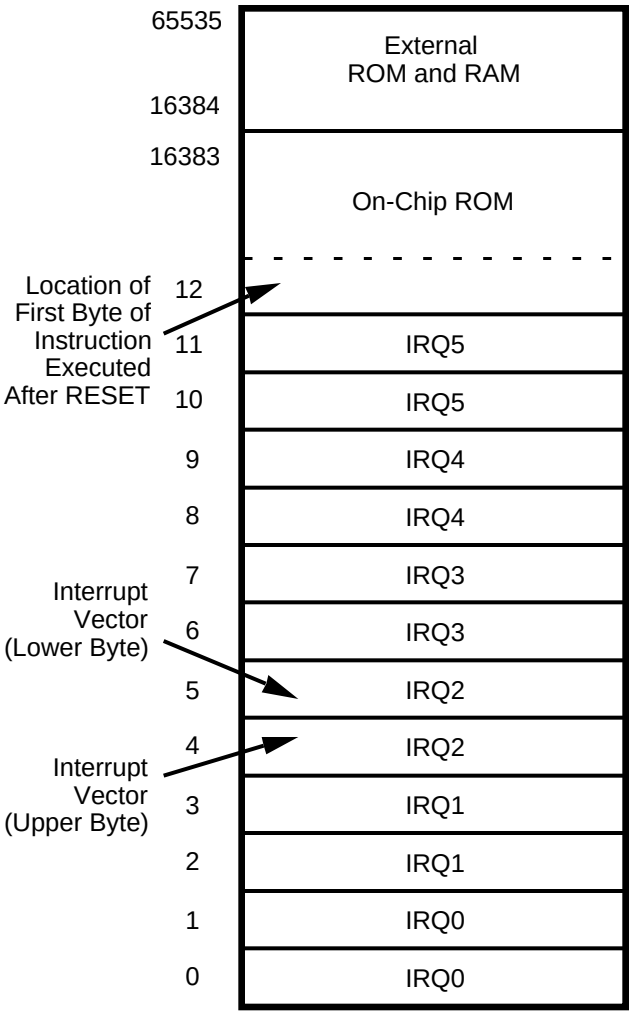


Figure 19. Program Memory Configuration

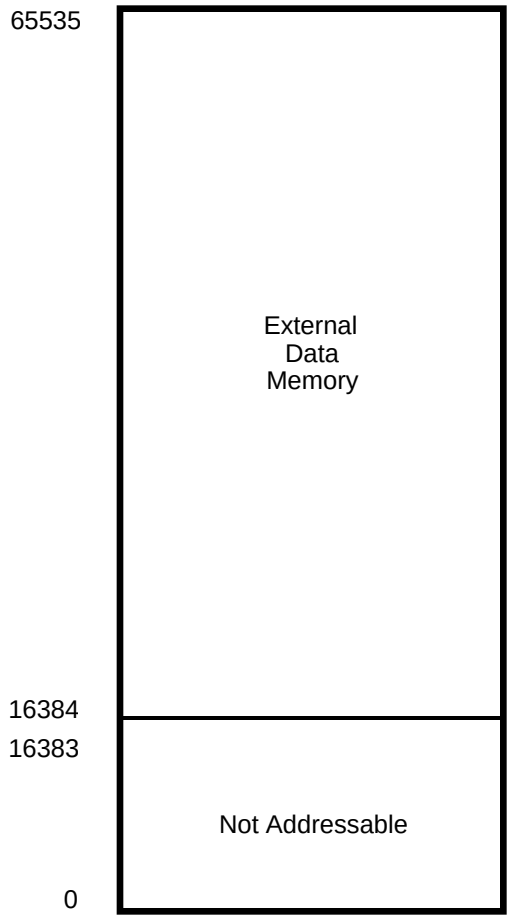


Figure 20. Data Memory Configuration

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 20).

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 21). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

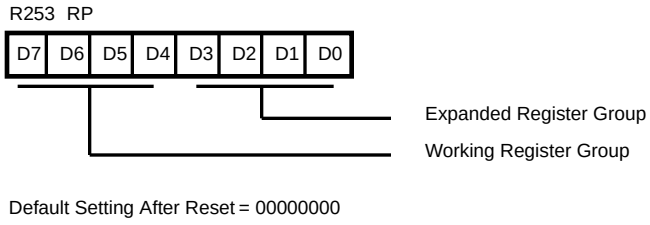


Figure 21. Register Pointer Register

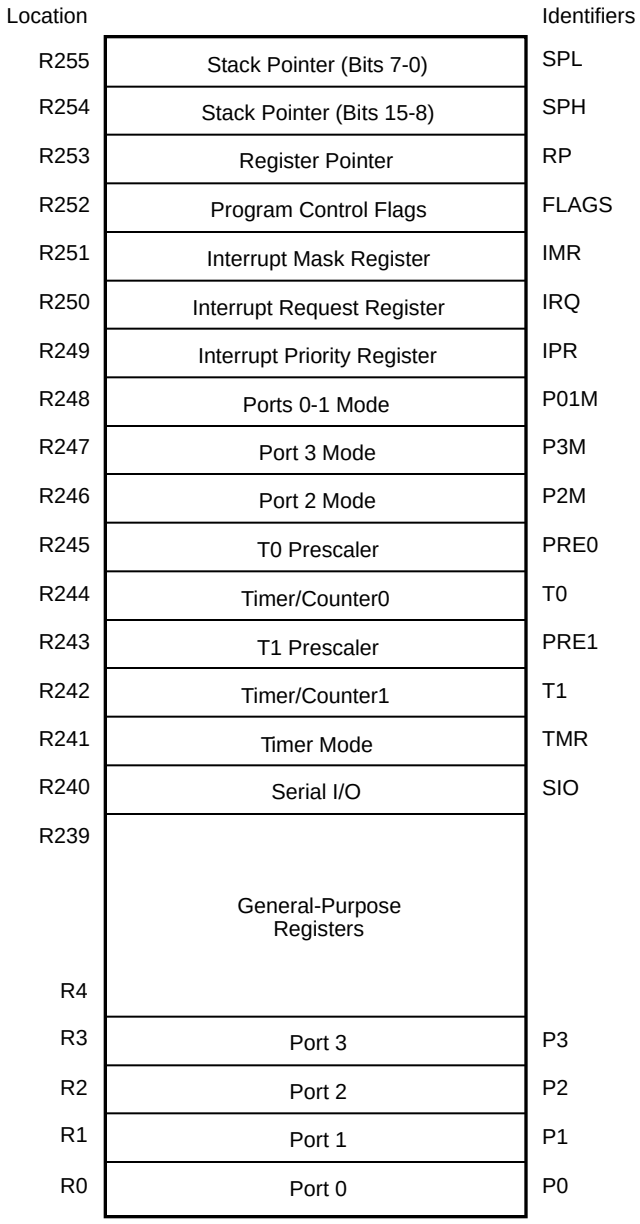


Figure 22. Register File

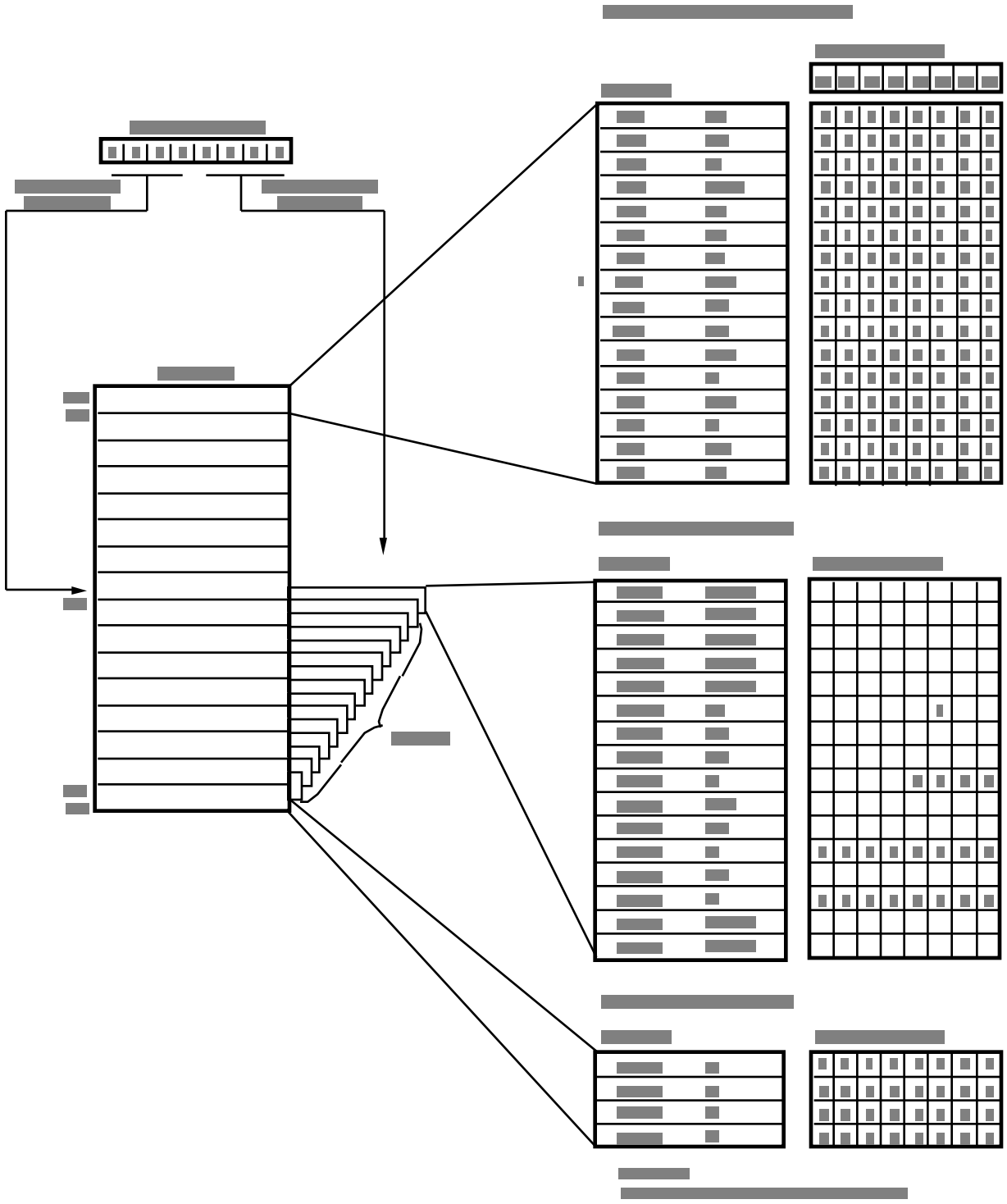


Figure 23. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 21). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 20) selects which group of 16 bytes in the register file, out of the full 236, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C61/62/96, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C61: (See Figures 21 and 22)

R253 RP = 00H	R0 = Port 0	R2 = Port 2
	R1 = Port 1	R3 = Port 3

But If:

R253 RP = 0FH
R0 = Reserved
R1 = Reserved
R2 = Port 4
R3 = Port 4, Direction Register
R9 = Port 6, Mode Register

Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general purpose register 12H
LD 12H, #11010110	Load value into general purpose register 12H
LD 2, #10010110	Load value into Port 4

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 16 Kbytes of program memory is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

Interrupts. The Z86C61/62/96 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 26). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C61/62/96 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

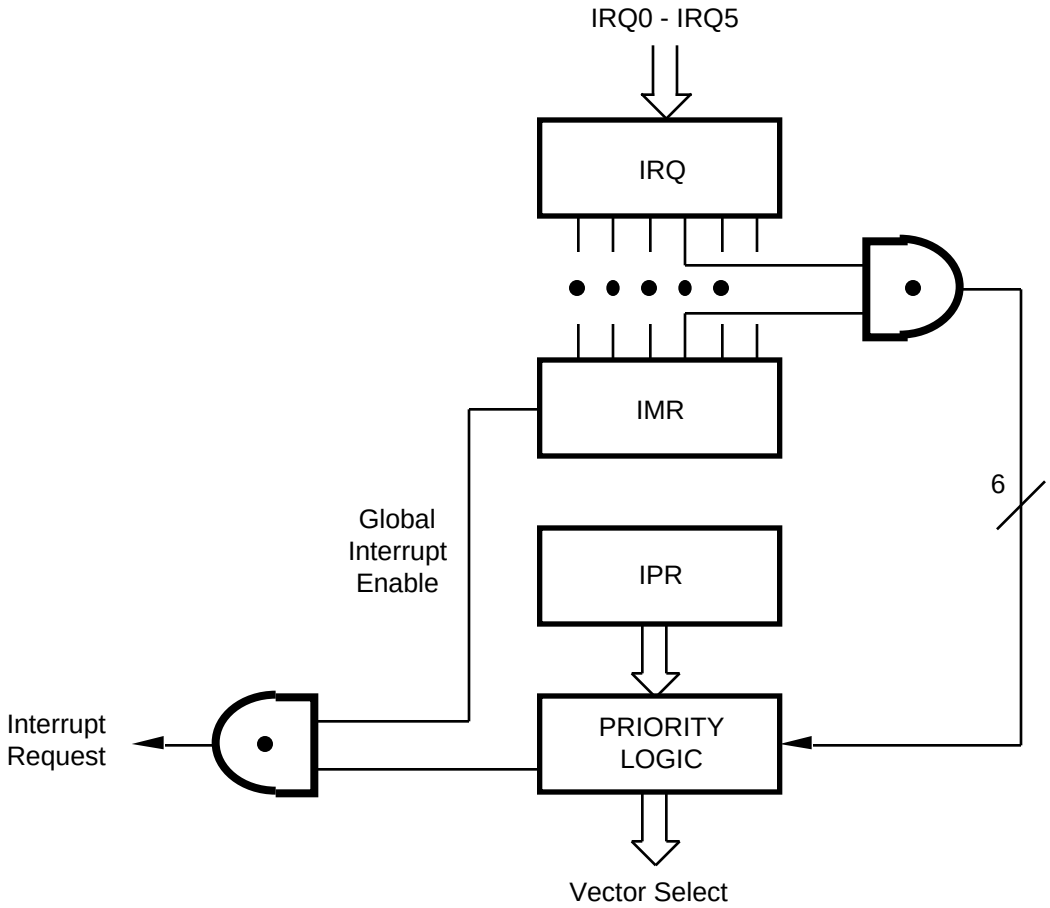


Figure 26. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C61/62/96 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to device ground (Figure 27).

Note: Actual capacitor values specified by the crystal manufacturer.

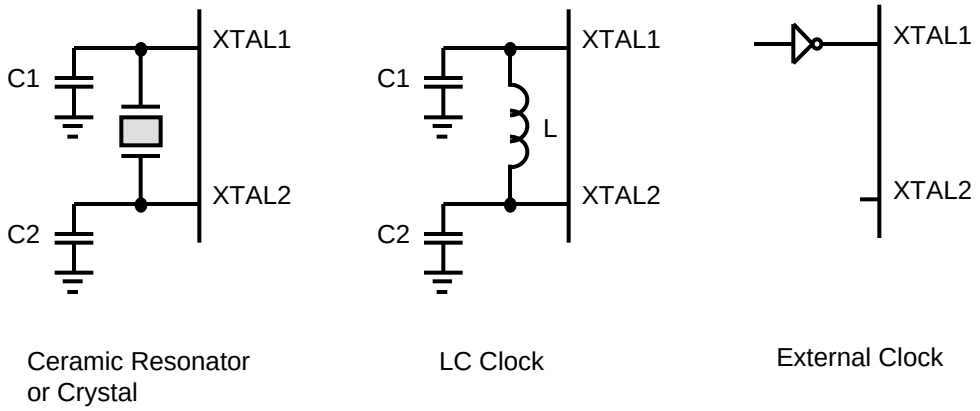


Figure 27. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                    or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

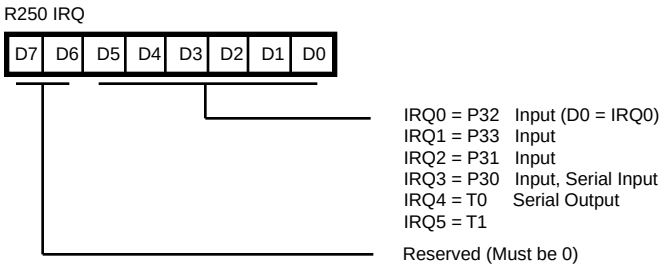


Figure 38. Interrupt Request Register (FAH: Read/Write)

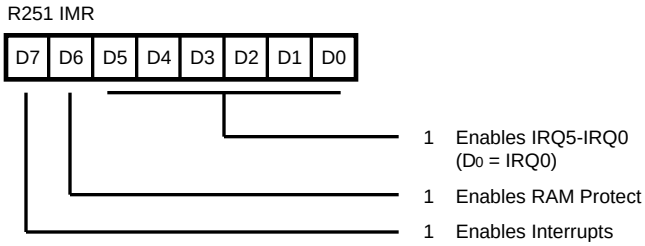


Figure 39. Interrupt Mask Register (FBH: Read/Write)

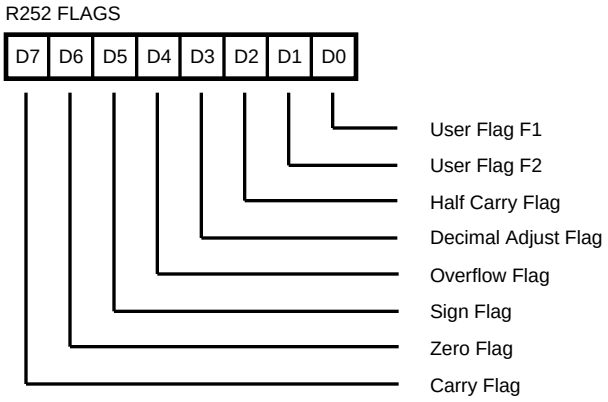


Figure 40. Flag Register (FCH: Read/Write)

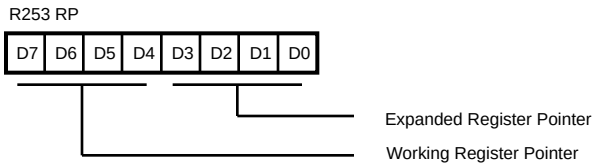


Figure 41. Register Pointer Register (FDH: Read/Write)

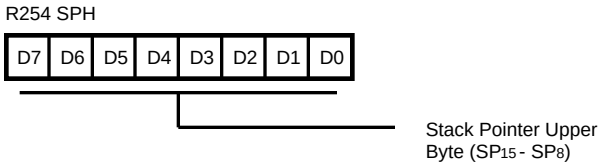


Figure 42. Stack Pointer Register (FEH: Read/Write)

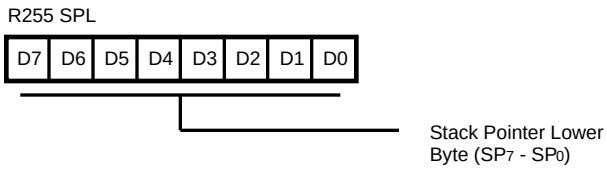
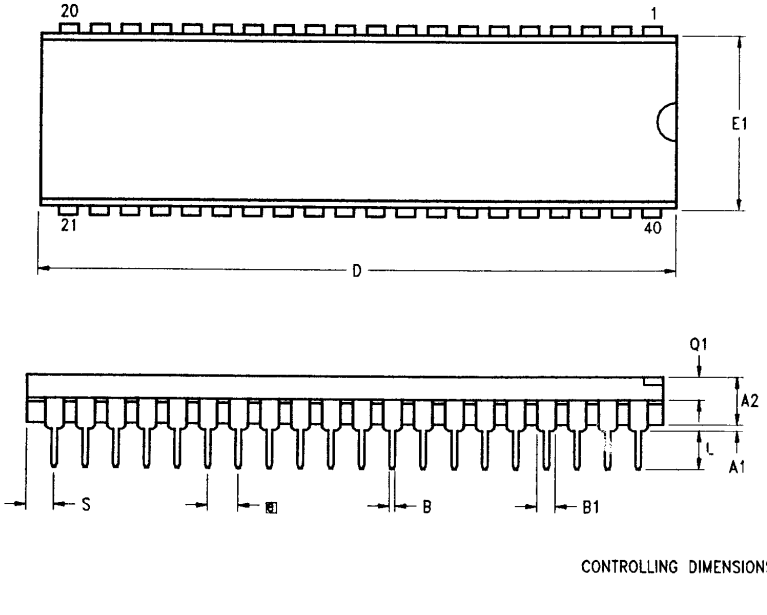


Figure 43. Stack Pointer Register (FFH: Read/Write)

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	1.02	.020	.040
A2	3.18	3.94	.125	.155
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
e	2.54 TYP		.100 TYP	
eA	15.49	16.76	.610	.660
L	3.05	3.81	.120	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

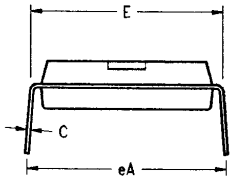


Figure 52. 40-Pin DIP Package Diagram

Figure 53. 44-Pin PLCC Package Diagram