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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	16MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	52
Program Memory Size	16KB (16K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	-
Supplier Device Package	64-DIP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c6216pscr3362

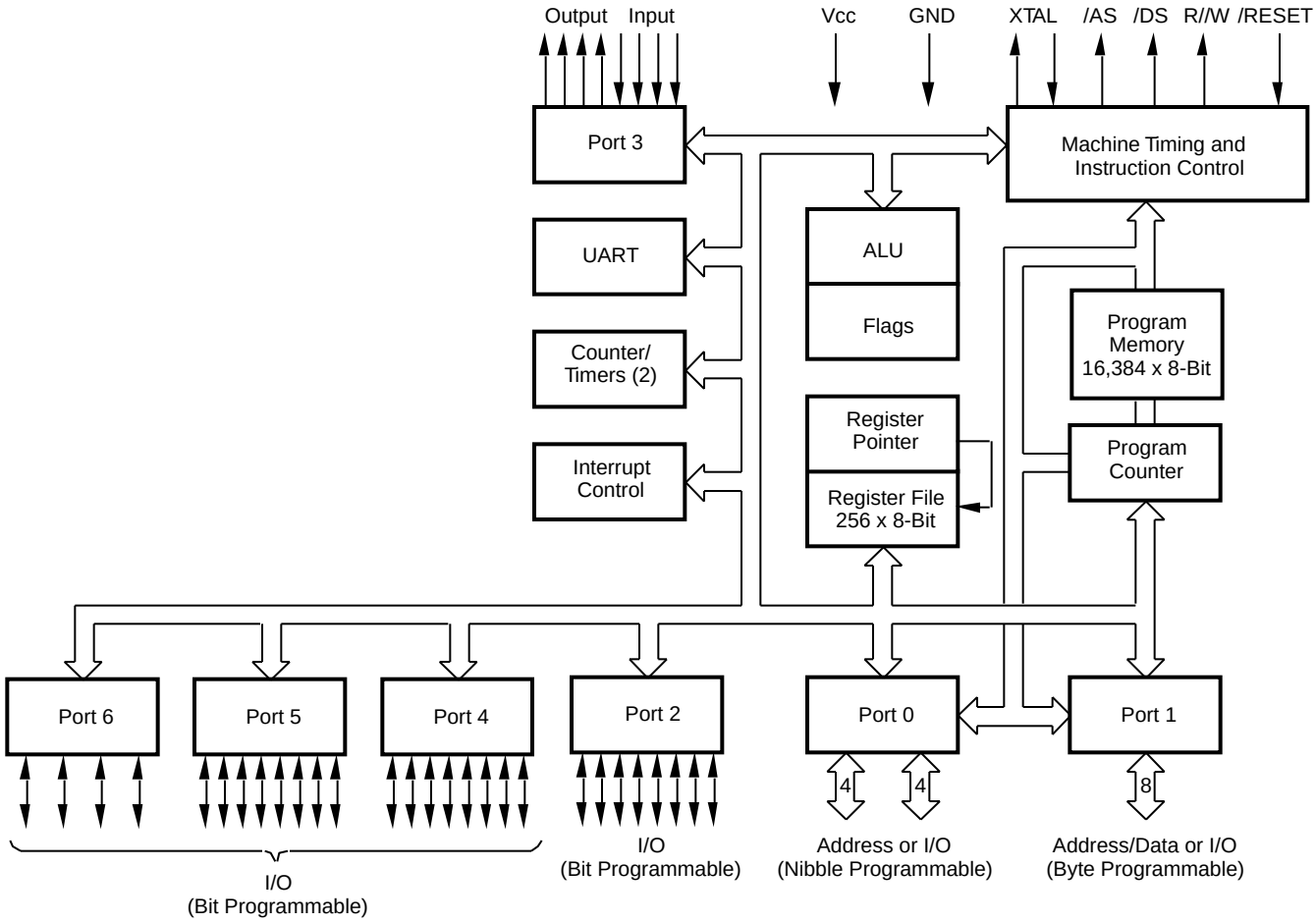


Figure 2. Z86C62 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

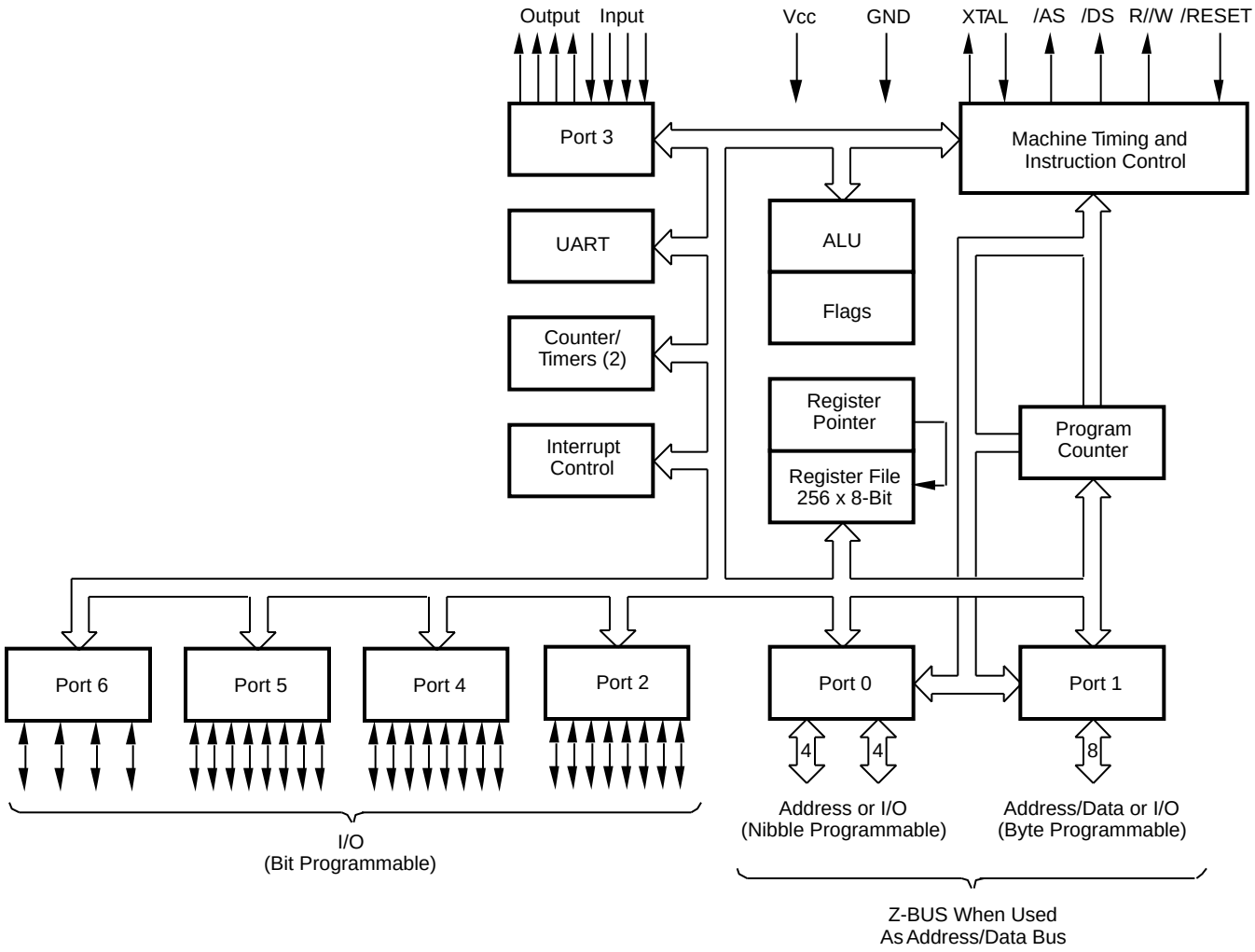


Figure 3. Z86C96 Functional Block Diagram

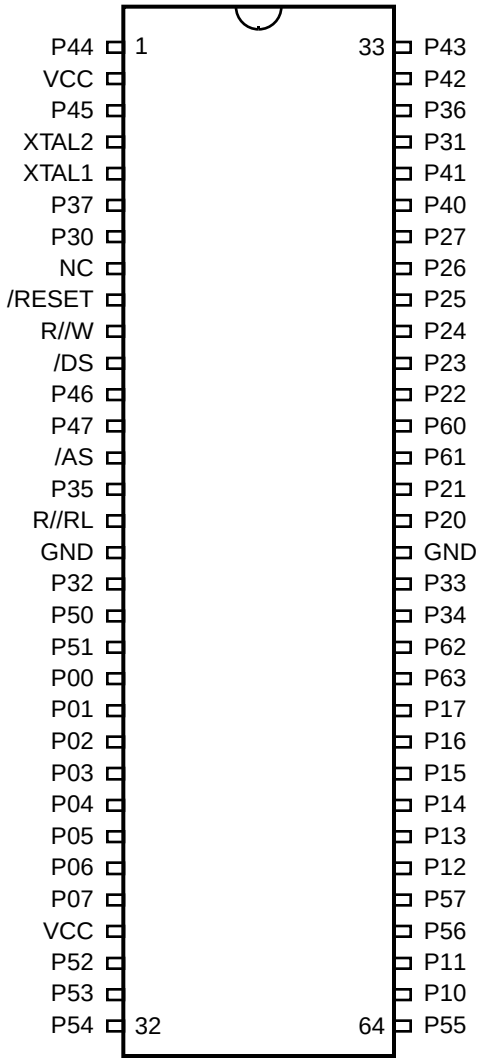


Figure 6. Z86C62/C96 64-Pin DIP Pin Assignments

Table 3. Z86C62/C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R//RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

Table 4. Z86C62/C96 68-Pin PLCC Pin Identification

Pin #	Symbol	Function	Direction
1-2	P44-P43	Port 4, Pins 3,4	In/Output
3	V_{CC}	Power Supply	Input
4	P45	Port 4, Pin 5	In/Output
5	XTAL2	Crystal, Oscillator Clock	Output
6	XTAL1	Crystal, Oscillator Clock	Input
7	P37	Port 3, Pin 7	Output
8	P30	Port 3, Pin 0	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/P0DS	Port 0 Data Strobe	Output
12	/DS	Data Strobe	Output
13-14	P47-P46	Port 4, Pins 6,7	In/Output
15	/P1DS	Port 1, Data Strobe	Output
16	/AS	Address Strobe	Output
17	/DTIMER	DTIMER	Input
18	P35	Port 3, Pin 5	Output
19	R//RL	ROM/ROMless control	Input
20	GND	Ground	Input
21	P32	Port 3, Pin 2	Input
22-23	P51-P50	Port 5, Pins 0,1	In/Output
24-31	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
32	V_{CC}	Power Supply	Input
33-36	P55-P52	Port 5, Pins 2,3,4,5	In/Output
37-38	P11-P10	Port 1, Pins 0,1	In/Output
39-40	P56-P57	Port 5, Pins 6,7	In/Output
41-46	P17-P12	Port 1, Pins2,3,4,5,6,7	In/Output
47-48	P63-P62	Port 6, Pins 3,2	In/Output
49	P34	Port 3, Pin 4	Output
50	P33	Port 3, Pin 3	Input
51	GND	Ground	Input
52	/SYNC	Synchronization	Output
53	SCLK	System Clock	Output
54-55	P21-P20	Port 2, Pins 0,1	In/Output
56-57	P60-P61	Port 6, Pins 1,0	In/Output
58-63	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
64-65	P41-P40	Port 4, Pins 0,1	In/Output
66	P31	Port 3, Pin 1	Input
67	P36	Port 3, Pin 6	Output
68	P42	Port 4, Pin 2	In/Output

DC ELECTRICAL CHARACTERISTICS

Z86C61/62/96

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC} – 100 mV		V_{CC} – 100 mV		V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0_V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	VRL = 0 V
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current		40		40	30	mA	[1] @ 20 MHz
I_{CC1}	Standby Current		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}

Notes:

1. All inputs driven to either 0V or V_{CC}, outputs floating.
2. V_{CC} = 3.0V to 3.6V
3. V_{CC} = 4.5V to 5.5V

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (20 MHz)

			T_A = 0°C to +70°C		T_A = -40°C to +105°C			
			20 MHz		20 MHz			
No	Sym	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	1,2,3
4	TwAS	/AS Low Width	30		30		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	65		65		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	2,3
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	2,3
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

AC CHARACTERISTICS

Additional Timing Table
Z86C61/62/96

			T_A = 0°C to +70°C 20/16 MHz		TA = -40°C to +105°C 20/16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	1
3	TwC	Input Clock Width	25		25		ns	1
4	TwTinL	Timer Input Low Width	75		75		ns	2
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	2
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	2
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	2
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	2,4
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	2,5
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	2,3

Notes:
1. Clock timing references use $0.8V_{CC}$ for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request through Port 3.
4. Interrupt request through Port 3 (P33-P31).
5. Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

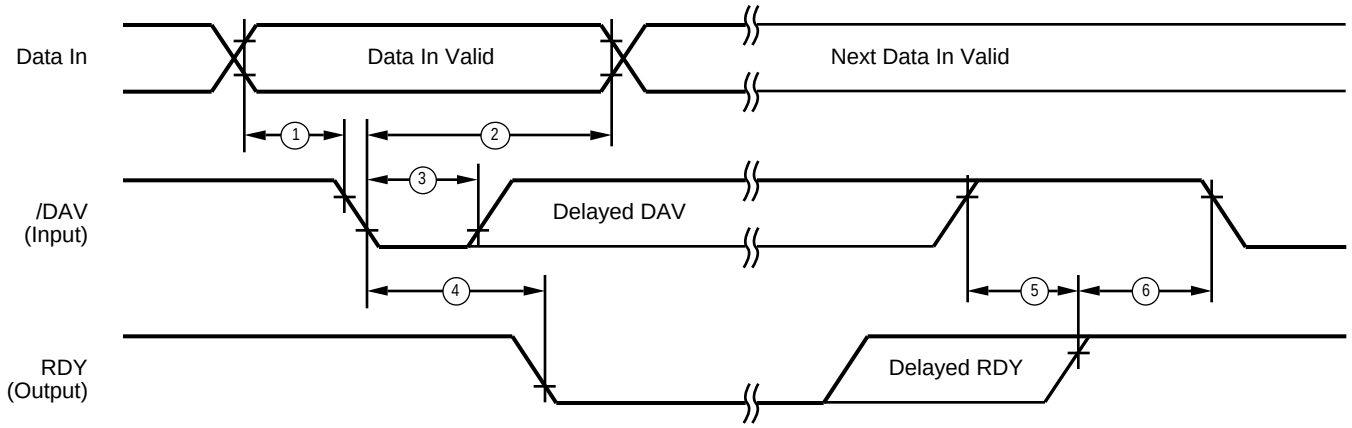


Figure 11. Input Handshake Timing

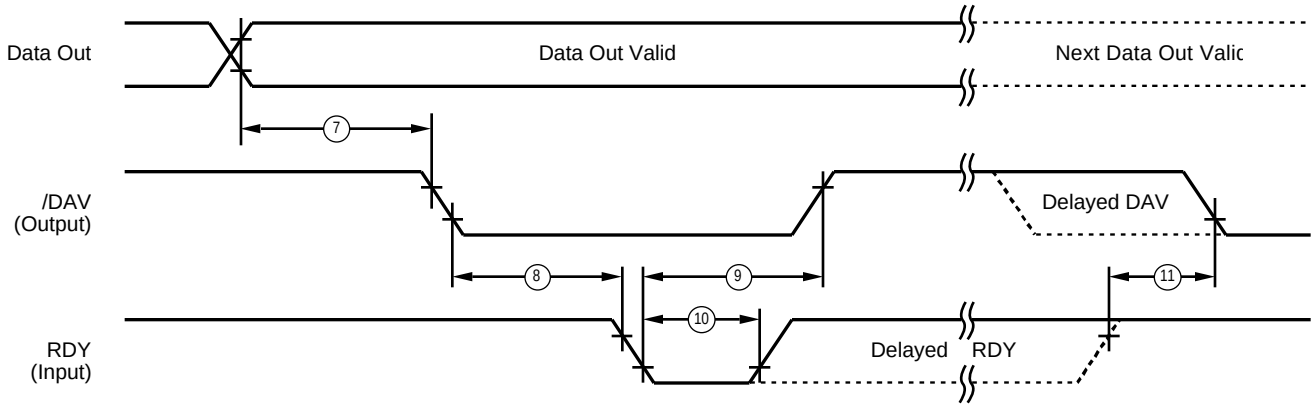


Figure 12. Output Handshake Timing

AC CHARACTERISTICS

Handshake Timing Table
Z86C61/62/96

			T_A = 0°C to +70°C		T_A = –40°C to +105°C		
			20/16 MHz		20/16 MHZ		Data
No	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY fall to DAV rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY rise to DAV fall Delay	115		115		OUT

PIN FUNCTIONS (Continued)

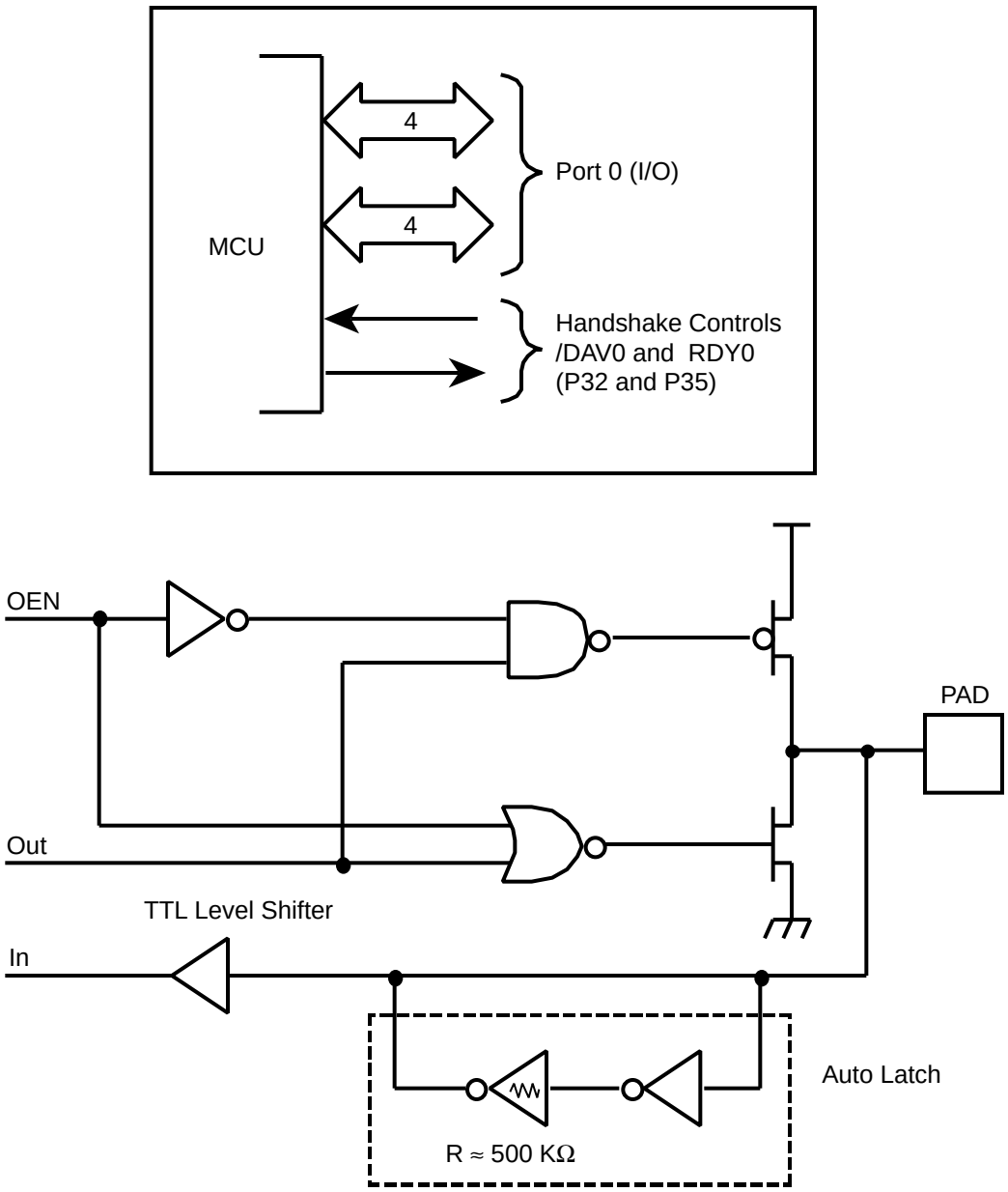


Figure 13. Port 0 Configuration

Port 1 (P17-P10). Port 1 is an 8-bit, byte programmable, bidirectional, TTL compatible port. It has multiplexed Address (A7-A0) and Data (D7-D0) ports. For Z86C61/62/96, these eight I/O lines can be programmed as Input or Output lines or can be configured under software control as an address/data port for interfacing external memory. When used as an I/O port, Port 1 may be placed under handshake control. In this configuration, Port 3 line P33 and P34 are used as the handshake controls RDY1 and /DAV1.

Memory locations greater than 16,384 are referenced through Port 1. To interface external memory, Port 1 must be programmed for the multiplexed Address/Data mode. If more than 256 external locations are required, Port 0 must output the additional lines.

Port 1 can be placed in high-impedance state along with Port 0, /AS, /DS, and R//W, allowing the microcontroller to share common resources in multiprocessor and DMA applications. Data transfers can be controlled by assigning P33 as a Bus Acknowledge input, and P34 as a Bus request output (Figure 14).

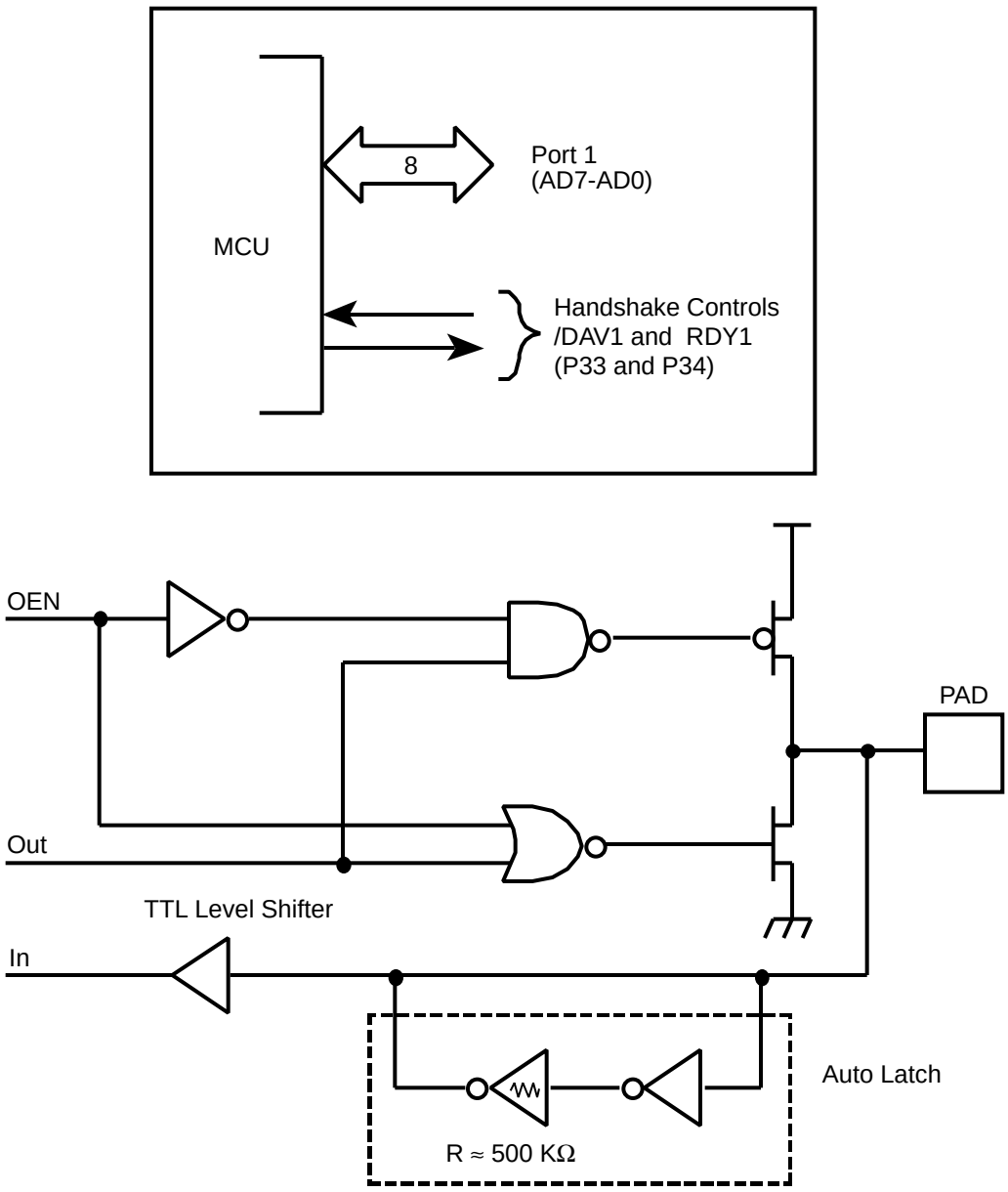


Figure 14. Port 1 Configuration

PIN FUNCTIONS (Continued)

Port 2 (P27-P20). Port 2 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 2 is always available for I/O operation. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines /DAV2 and RDY2. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to P27 (Figure 15).

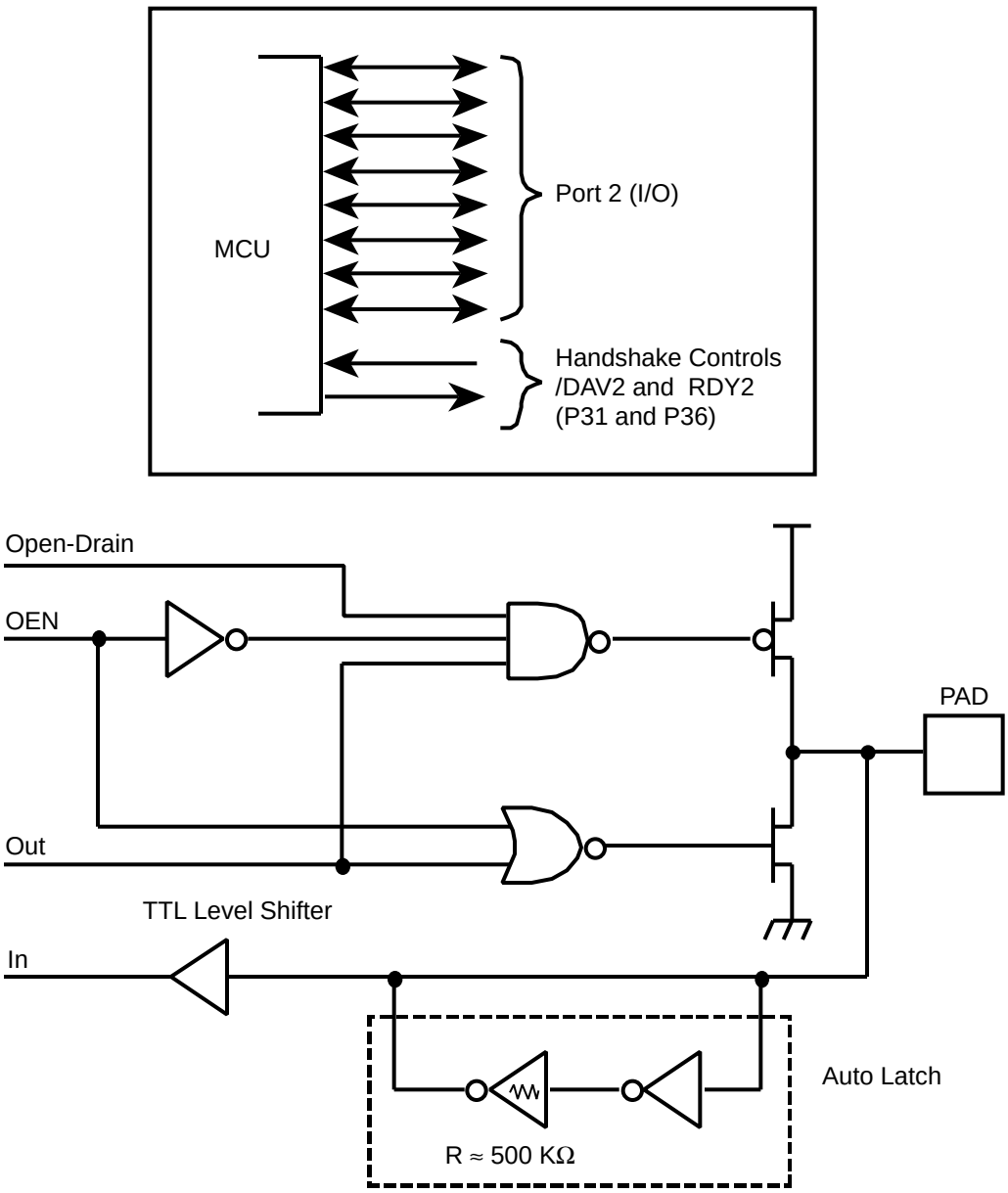


Figure 15. Port 2 Configuration

PIN FUNCTIONS (Continued)

Port 4 (P47-P40). Port 4 is an 8-bit, bit programmable, bi-directional, CMOS-compatible port. Each of these eight I/O lines can be independently programmed as an input or output or globally as an open-drain output. Port 4 is always available for I/O operation (Figure 18). Port address (F)02.

Port 5 (P57-P50). Same as Port 4. Port address (F)04.

Port 6 (P63-P60). Same as Port 4. (Note: this is a 4-bit port, bits D3-D0.) Port address (F)07.

Auto Latch. The Auto Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when it is not being driven by any source.

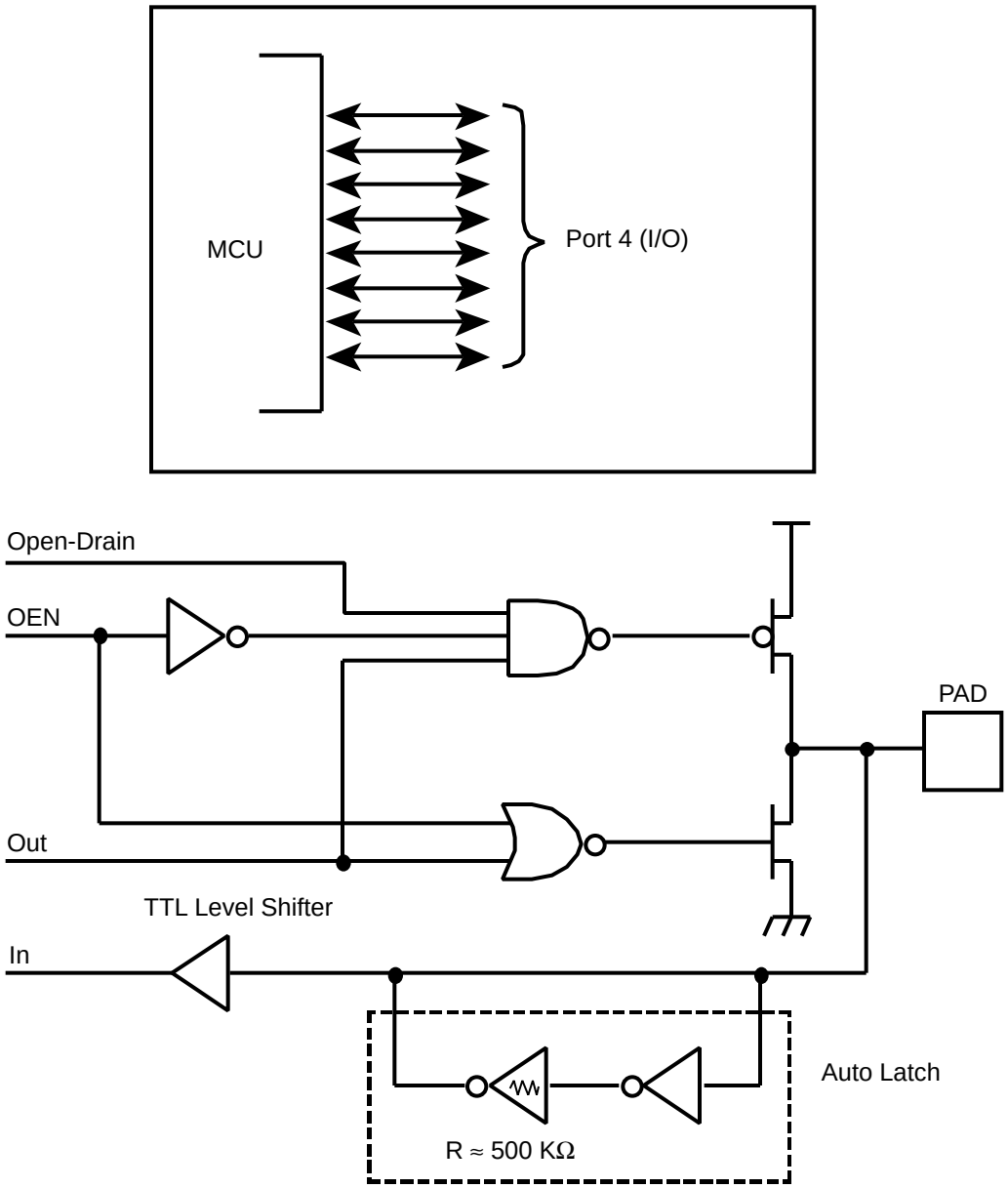


Figure 18. Port 4 Configuration

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 20).

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 21). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

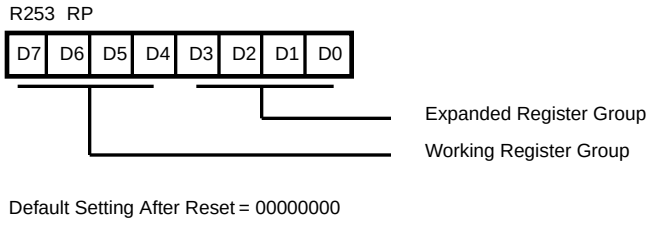


Figure 21. Register Pointer Register

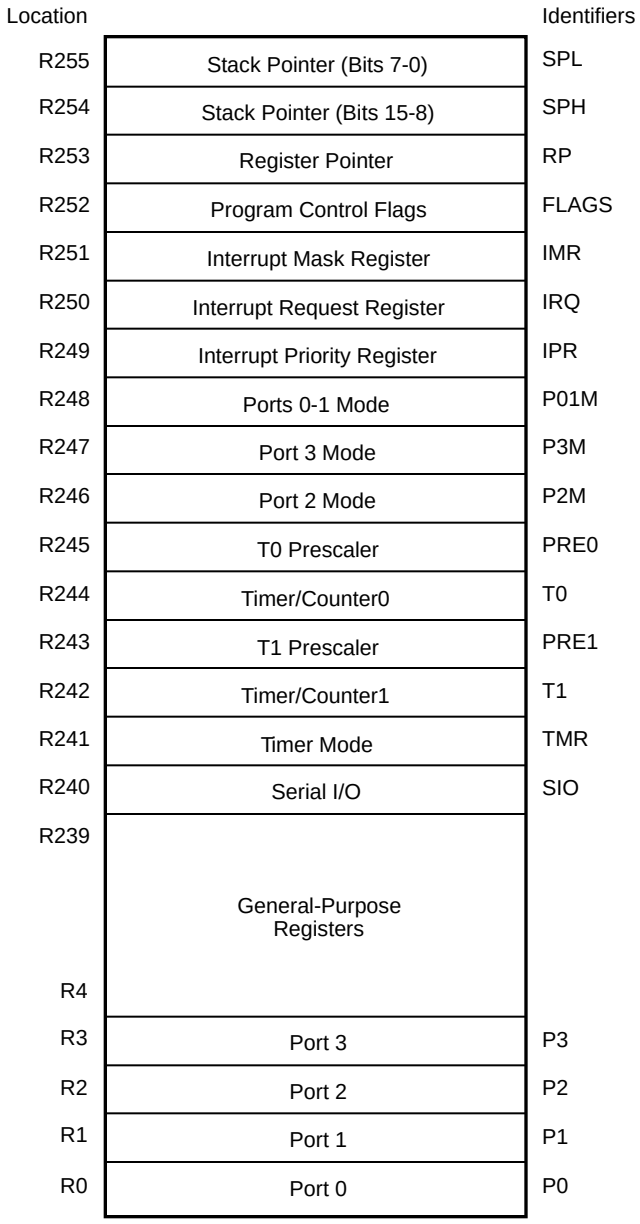


Figure 22. Register File

Interrupts. The Z86C61/62/96 has six different interrupts from eight different sources. The interrupts are maskable and prioritized. The eight sources are divided as follows: four sources are claimed by Port 3 lines P33-P30, one in Serial Out, one is Serial In, and two in the counter/timers (Figure 26). The Interrupt Mask Register globally or individually enables or disables the six interrupt requests. When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. All Z86C61/62/96 interrupts are vectored through locations in the program memory. When an interrupt machine cycle is activated, an interrupt request is granted. Thus, this disables all of the subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service. Software initialed interrupts are supported by setting the appropriate bit in the Interrupt Request Register (IRQ).

Internal interrupt requests are sampled on the falling edge of the last cycle of every instruction. The interrupt request must be valid 5TpC before the falling edge of the last clock cycle of the currently executing instruction.

For the ROMless mode, when the device samples a valid interrupt request, the next 48 (external) clock cycles are used to prioritize the interrupt, and push the two PC bytes and the FLAG register onto the stack. The following nine cycles are used to fetch the interrupt vector from external memory. The first byte of the interrupt service routine is fetched beginning on the 58th TpC cycle following the internal sample point, which corresponds to the 63rd TpC cycle following the external interrupt sample point.

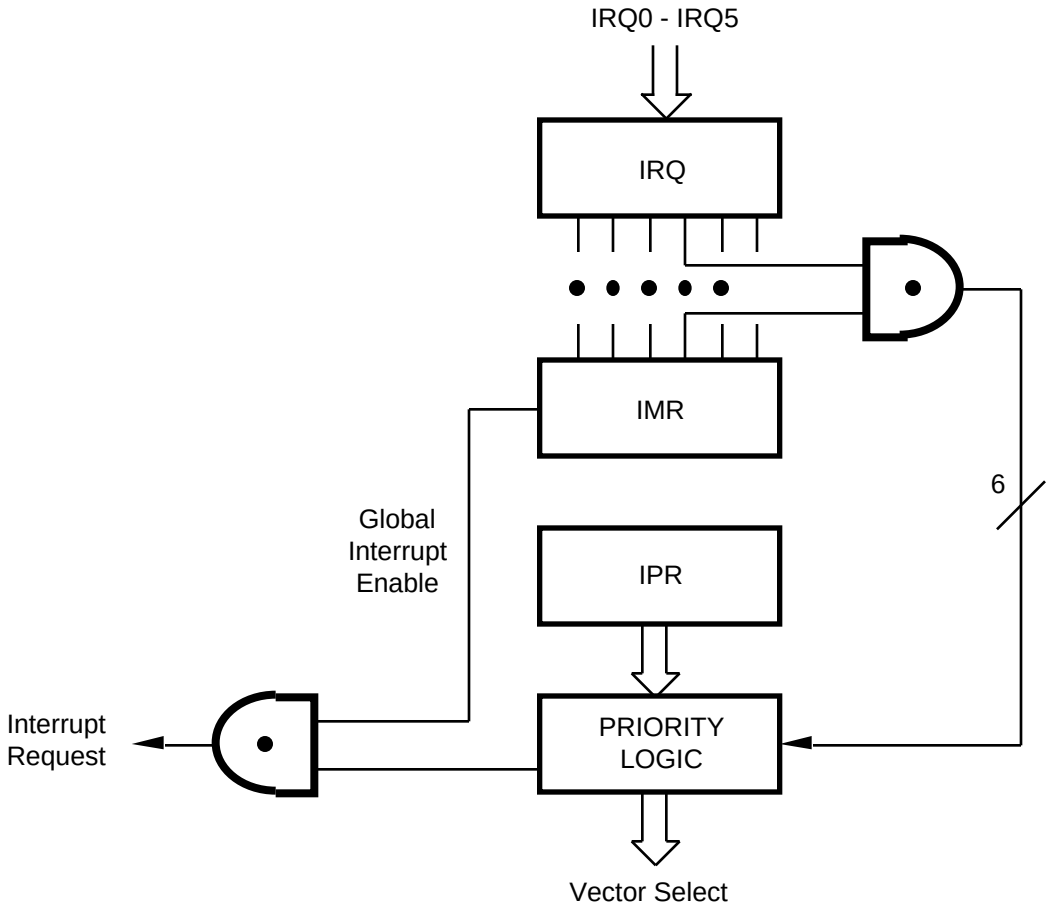


Figure 26. Interrupt Block Diagram

FUNCTIONAL DESCRIPTION (Continued)

Clock. The Z86C61/62/96 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 1 MHz to 20 MHz max, and series resistance (RS) is less than or equal to 100 Ohms. The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (10 pF < CL < 100 pF) from each pin to device ground (Figure 27).

Note: Actual capacitor values specified by the crystal manufacturer.

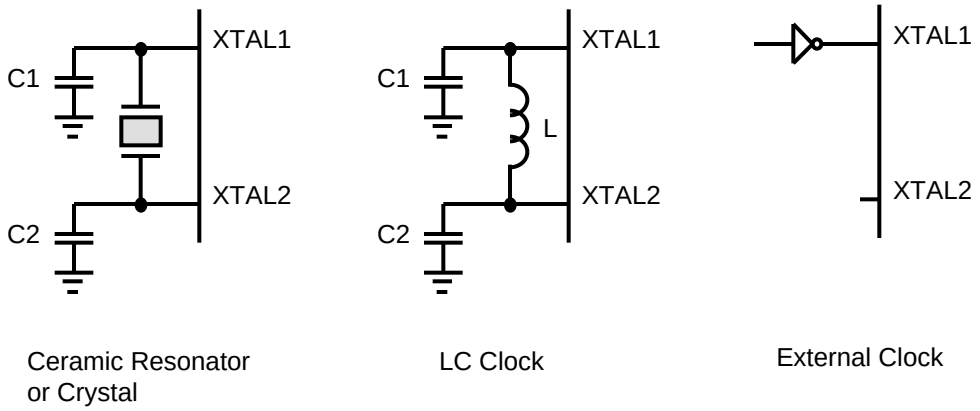


Figure 27. Oscillator Configuration

HALT. Turns off the internal CPU clock but not the XTAL oscillation. The counter/timers and the external interrupts IRQ0, IRQ1, IRQ2, and IRQ3 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after the HALT.

STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 5 µA (typical) or less. The STOP mode is terminated by a reset, which causes the processor to restart the application program at address 000CH.

In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=0FFH) immediately before the appropriate sleep instruction, i.e.,

```
FF      NOP     ; clear the pipeline
6F      STOP    ; enter STOP mode
                    or
FF      NOP     ; clear the pipeline
7F      HALT    ; enter HALT mode
```

Z8 CONTROL REGISTER DIAGRAMS (Continued)

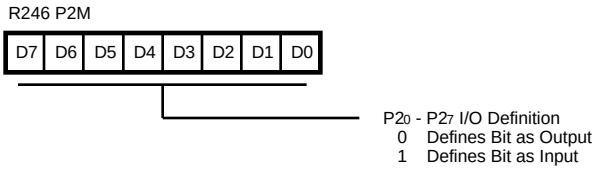


Figure 34. Port 2 Mode Register (F6H: Write Only)

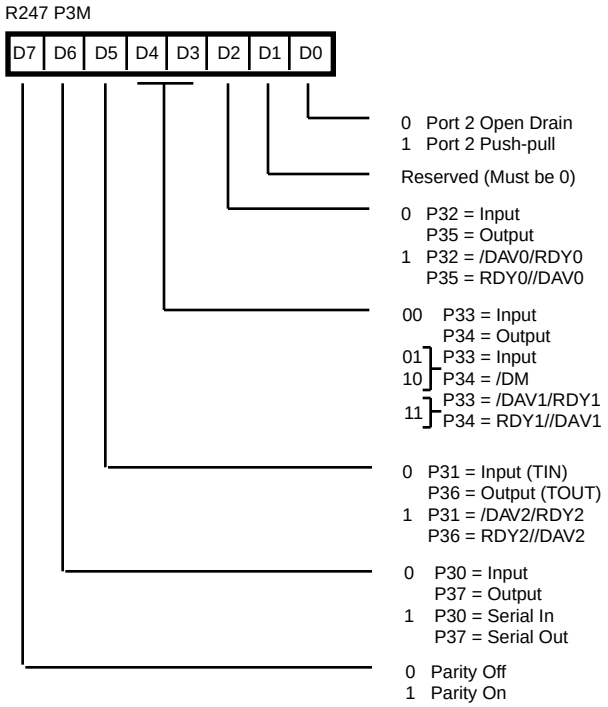


Figure 35. Port 3 Mode Register (F7H: Write Only)

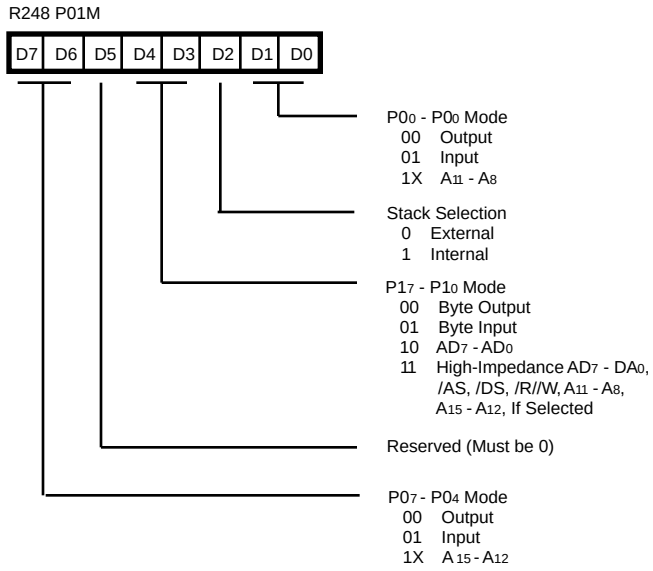


Figure 36. Port 0 and 1 Mode Register (F8H: Write Only)

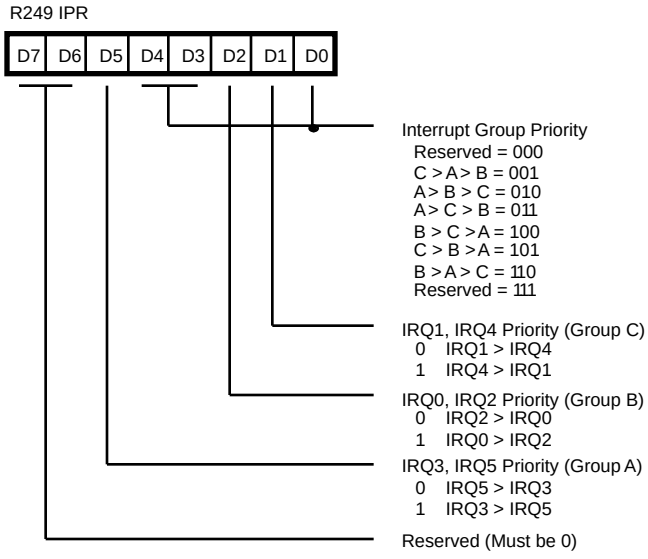


Figure 37. Interrupt Priority Register (F9H: Write Only)

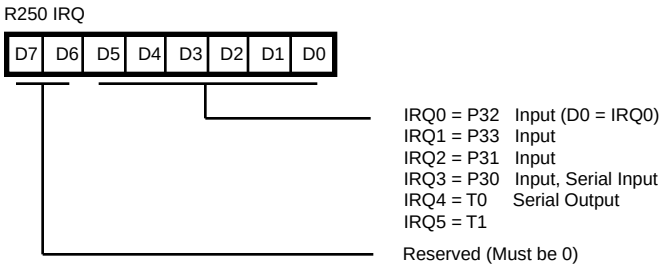


Figure 38. Interrupt Request Register (FAH: Read/Write)

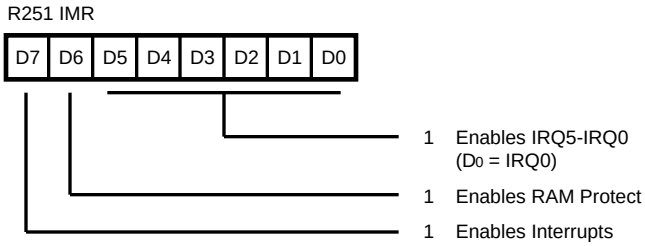


Figure 39. Interrupt Mask Register (FBH: Read/Write)

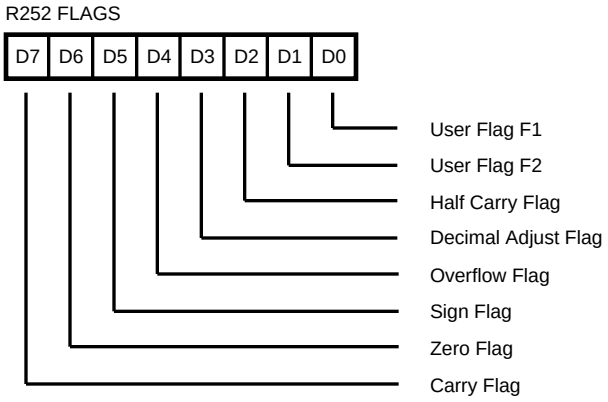


Figure 40. Flag Register (FCH: Read/Write)

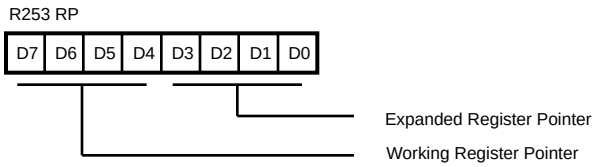


Figure 41. Register Pointer Register (FDH: Read/Write)

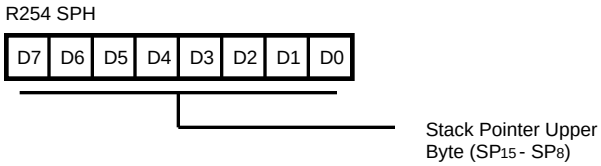


Figure 42. Stack Pointer Register (FEH: Read/Write)

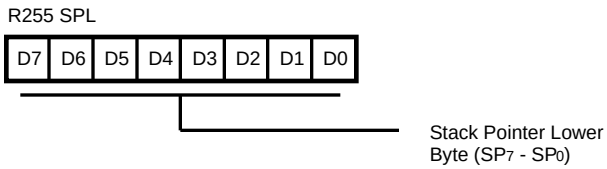


Figure 43. Stack Pointer Register (FFH: Read/Write)

Z8 EXPANDED REGISTER FILE CONTROL REGISTERS

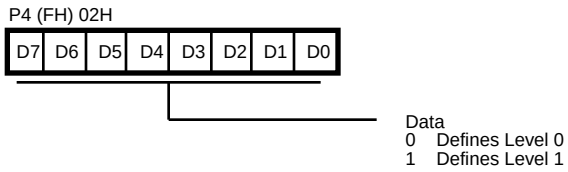


Figure 44. Port 4 Data Register (F) 02: Read/Write)

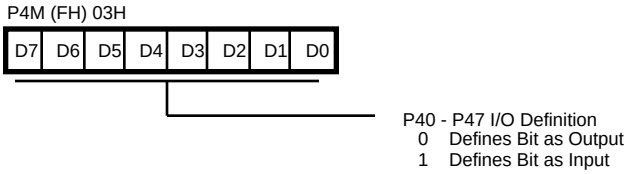


Figure 45. Port 4 Mode Register (F(03: (Write Only)

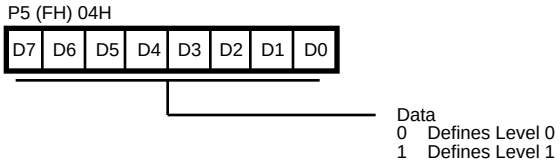


Figure 46. Port 5 Data Register (f) 04: (Read/Write)

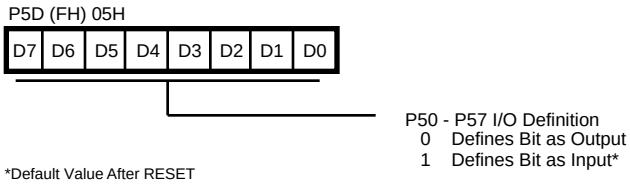


Figure 47. Port 5 Mode Register (F) 05: (Write Only)

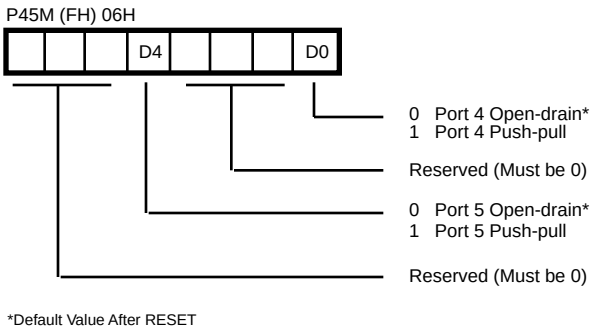


Figure 48. Port 4/5 Configuration Register (F) 06: (Write Only)

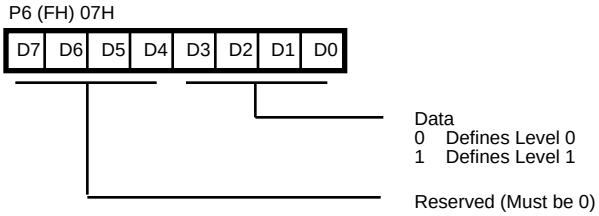


Figure 49. Port 6 Data Register (F) 07: (Read/Write)

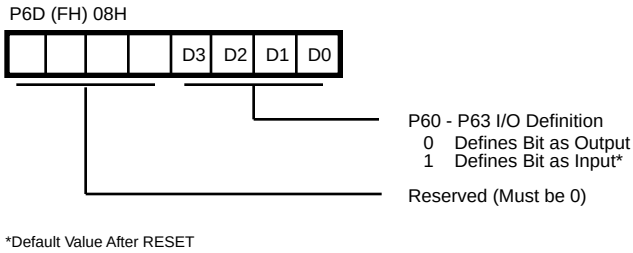


Figure 50. Port 6 Mode Register (F) 08: (Write Only)

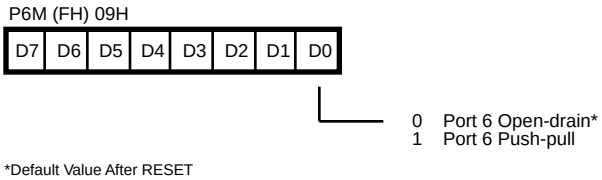


Figure 51. Port 6 Mode Register (F) 09: (Write Only)

ORDERING INFORMATION

Z86C61/62/96

16 MHz

40-pin DIP	44-pin PLCC
Z86C6116PSC	Z86C6116VSC

16 MHz

64-pin DIP	68-pin PLCC
Z86C6216PSC	Z86C6216VSC

20 MHz

64-pin DIP	68-pin PLCC
Z86C9620PSC	Z86C9620VSC

For fast results, contact your Zilog sales office for assistance in ordering the part desired.

Codes

Package
P = Plastic DIP
V = Plastic Chip Carrier

Preferred Temperature
S = 0°C to +70°C

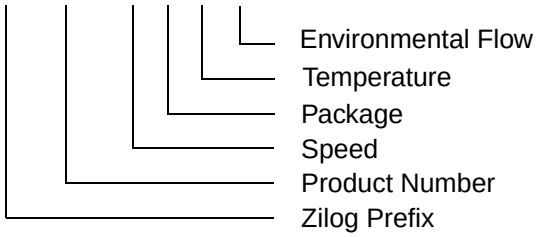
Longer Lead Time
E = -40°C to 105°C

Speeds
16 = 16 MHz
20 = 20 MHz

Environmental
C = Plastic Standard

Example:

Z 86C61 16 P S C is a Z86C61, 16 MHz, DIP, 0° to +70°C, Plastic Standard Flow



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