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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	52
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9620psc

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C61/62/96 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART (Figures 1, 2, and 3).

Notes: All Signals with a preceding front slash, "/", are active Low. For example B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

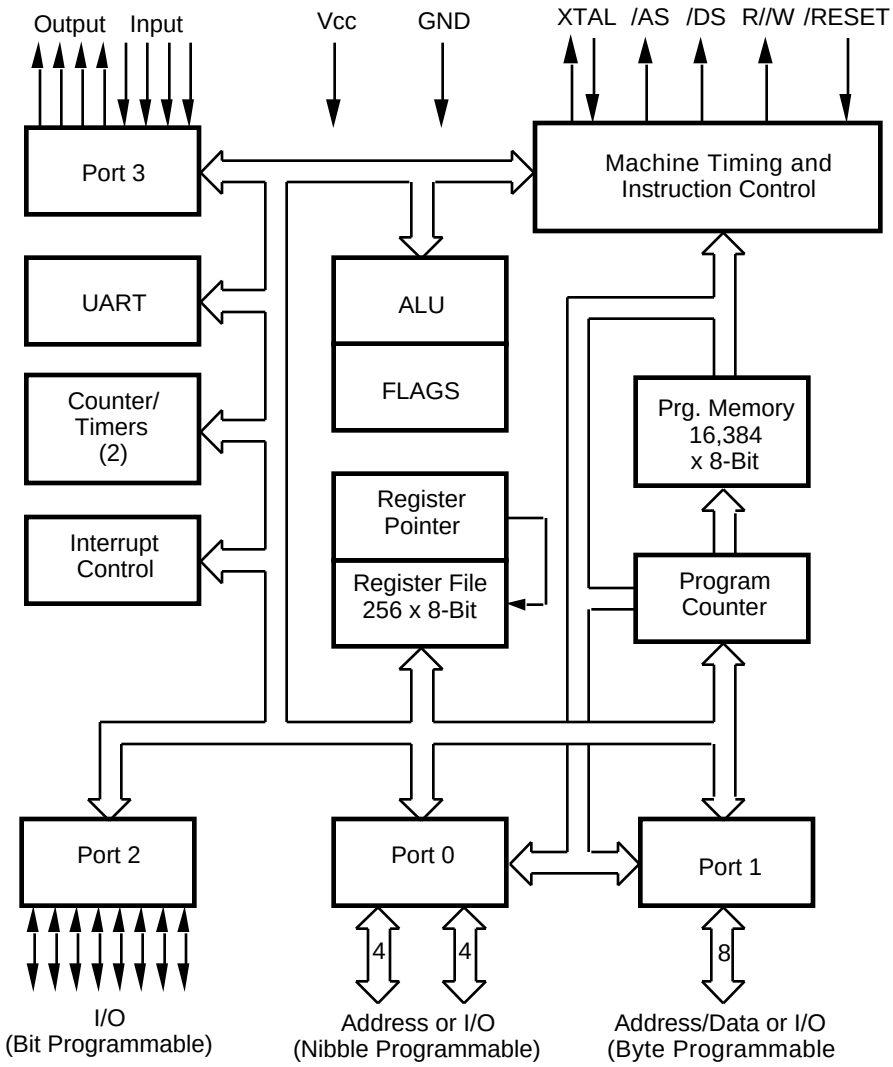


Figure 1. Z86C61 Functional Block Diagram

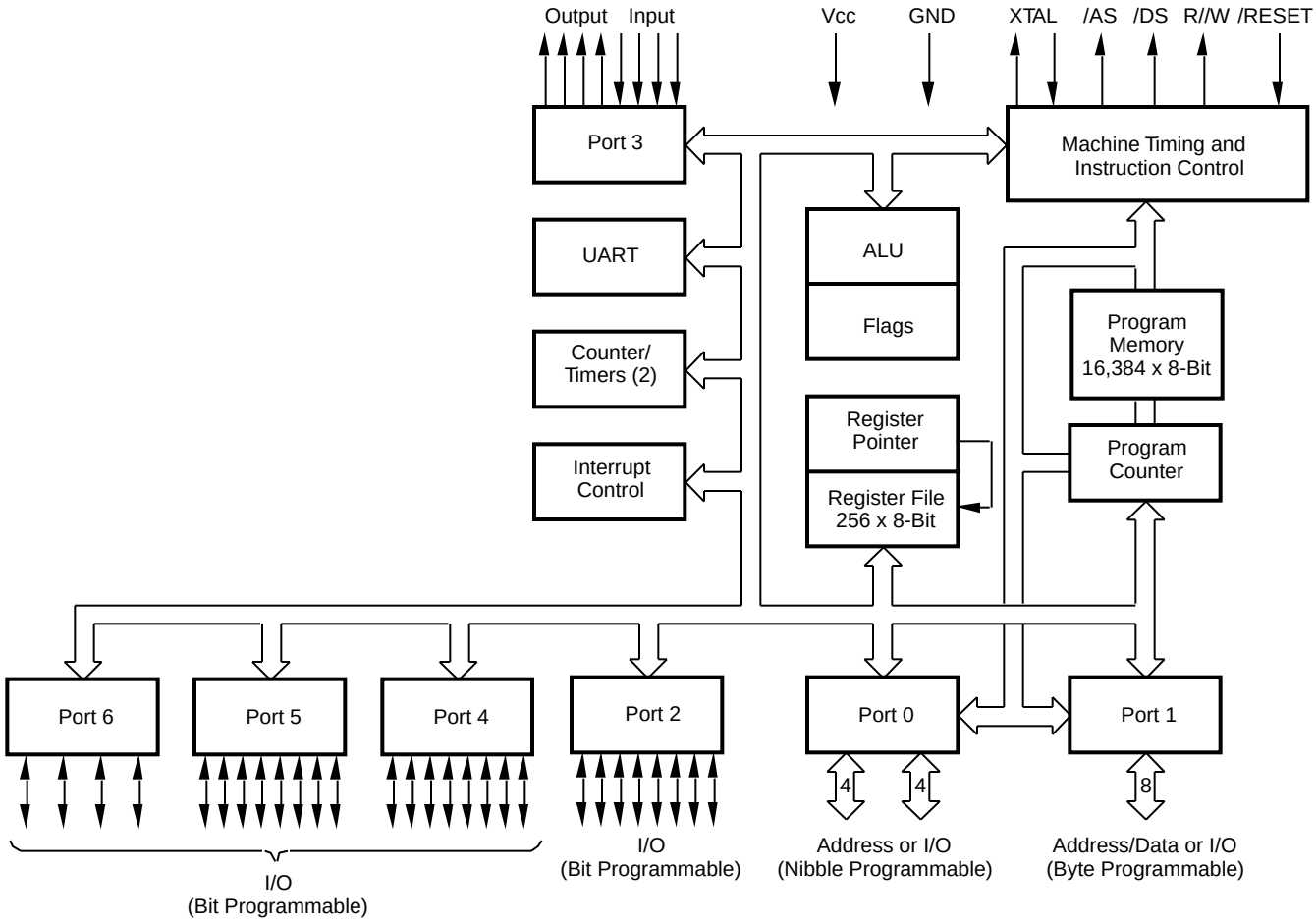


Figure 2. Z86C62 Functional Block Diagram

PIN DESCRIPTION (Continued)

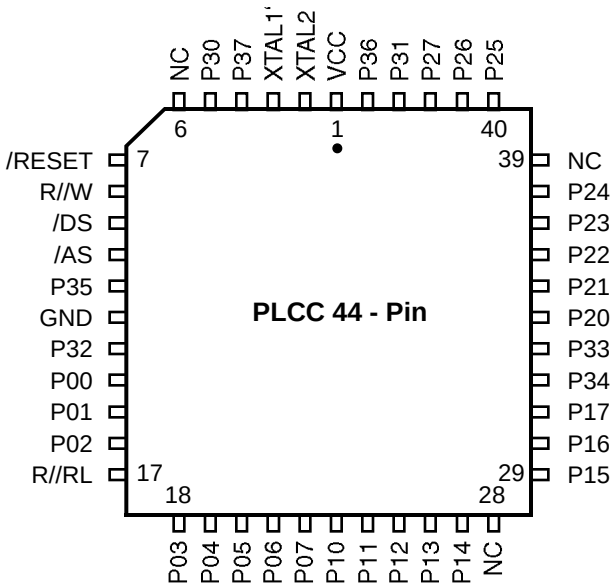


Figure 5. Z86C61 44-Pin PLCC Pin Assignments

Table 2. Z86C61 44-Pin PLCC Pin Assignments

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
17	R//RL	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output

Table 2. Z86C61 44-Pin PLCC Pin Assignments

Pin #	Symbol	Function	Direction
23-27	P14-P10	Port 1, Pins 0,1,2,3,4	In/Output
28	N/C	Not Connected	Input
29-31	P17-P15	Port 1, Pins 5,6,7	In/Output
32	P34	Port 3, Pin 4	Output
33	P33	Port 3, Pin 3	Input
34-38	P24-P20	Port 2, Pins 0,1,2,3,4	In/Output
39	N/C	Not Connected	Input
40-42	P25-P27	Port 2, Pins 5,6,7	In/Output
43	P31	Port 3, Pin 1	Input
44	P36	Port 3, Pin 6	Output

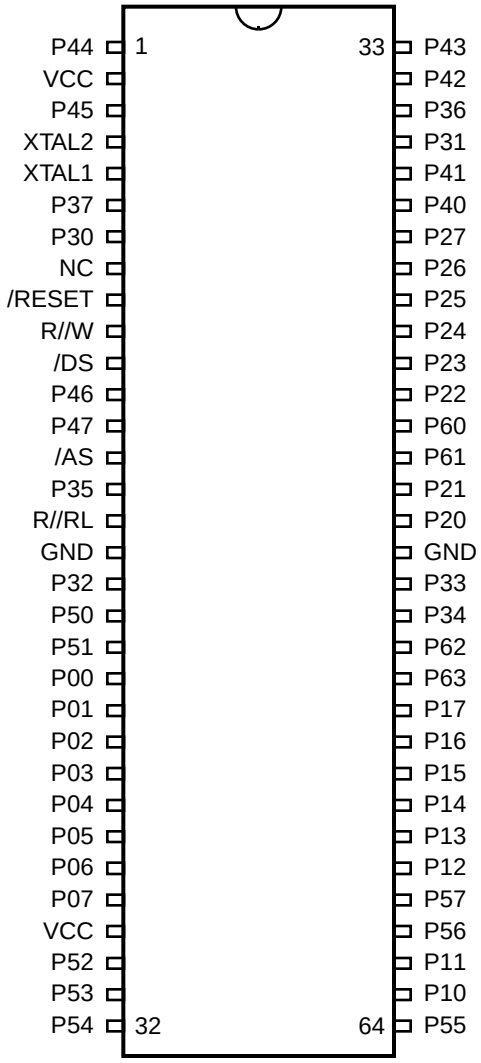


Figure 6. Z86C62/C96 64-Pin DIP Pin Assignments

Table 3. Z86C62/C96 64-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	P44	Port 4, Pin 4	In/Output
2	V_{CC}	Power Supply	Input
3	P45	Port 4, Pin 5	In/Output
4	XTAL2	Crystal, Oscillator Clock	Output
5	XTAL1	Crystal, Oscillator Clock	Input
6	P37	Port 3, Pin 7	Output
7	P30	Port 3, Pin 0	Input
8	N/C	Not Connected	Input
9	/RESET	Reset	Input
10	R//W	Read/Write	Output
11	/DS	Data Strobe	Output
12-13	P47-P46	Port 4, Pin 6,7	In/Output
14	/AS	Address Strobe	Output
15	P35	Port 3, Pin 5	Output
16	R//RL	ROM/ROMless control	Input
17	GND	Ground	Input
18	P32	Port 3, Pin 2	Input
19-20	P51-P50	Port 5, Pin 0,1	In/Output
21-28	P07-P00	Port 0, Pins 0,1,2,3,4,5,6,7	In/Output
29	V_{CC}	Power Supply	Input
30-33	P52-P55	Port 5, Pins 2,3,4,5	In/Output
34-35	P11-P10	Port 1, Pins 0,1	In/Output
36-37	P57-P56	Port 5, Pins 6,7	In/Output
38-43	P17-P12	Port 1, Pins 2,3,4,5,6,7	In/Output
44-45	P63-P62	Port 6, Pins 3,2	In/Output
46	P34	Port 3, Pin 4	Output
47	P33	Port 3, Pin 3	Input
48	GND	Ground	Input
49-50	P21-P20	Port 2, Pins 0,1	In/Output
51-52	P61-P60	Port 6, Pins 1,0	In/Output
53-58	P27-P22	Port 2, Pins 2,3,4,5,6,7	In/Output
59-60	P41-P40	Port 4, Pins 0,1	In/Output
61	P31	Port 3, Pin 1	Input
62	P36	Port 3, Pin 6	Output
63	P42	Port 4, Pin 2	In/Output
64	P43	Port 4, Pin 3	In/Output

ABSOLUTE MAXIMUM RATINGS

Sym	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
*Voltages on all pins with respect to GND.
†See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 4).

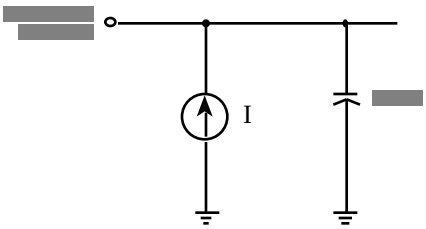


Figure 8. Test Load Diagram

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (20 MHz)

			T_A = 0°C to +70°C		T_A = -40°C to +105°C			
			20 MHz		20 MHz			
No	Sym	Parameter	Min	Max	Min	Max	Units	Notes
1	TdA(AS)	Address Valid to /AS rise Delay	15		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	25		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		120		120	ns	1,2,3
4	TwAS	/AS Low Width	30		30		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		105		105	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	65		65		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	55		55		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	40		40		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	25		25		ns	2,3
12	TdR/W(AS)	R//W Valid to /AS rise Delay	20		20		ns	2,3
13	TdDS(R/W)	/DS rise to R//W Not Valid	25		25		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	20		20		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	25		25		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		150		150	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	35		35		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	15		15		ns	2,3

Notes:
1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

AC CHARACTERISTICS

Additional Timing Diagram

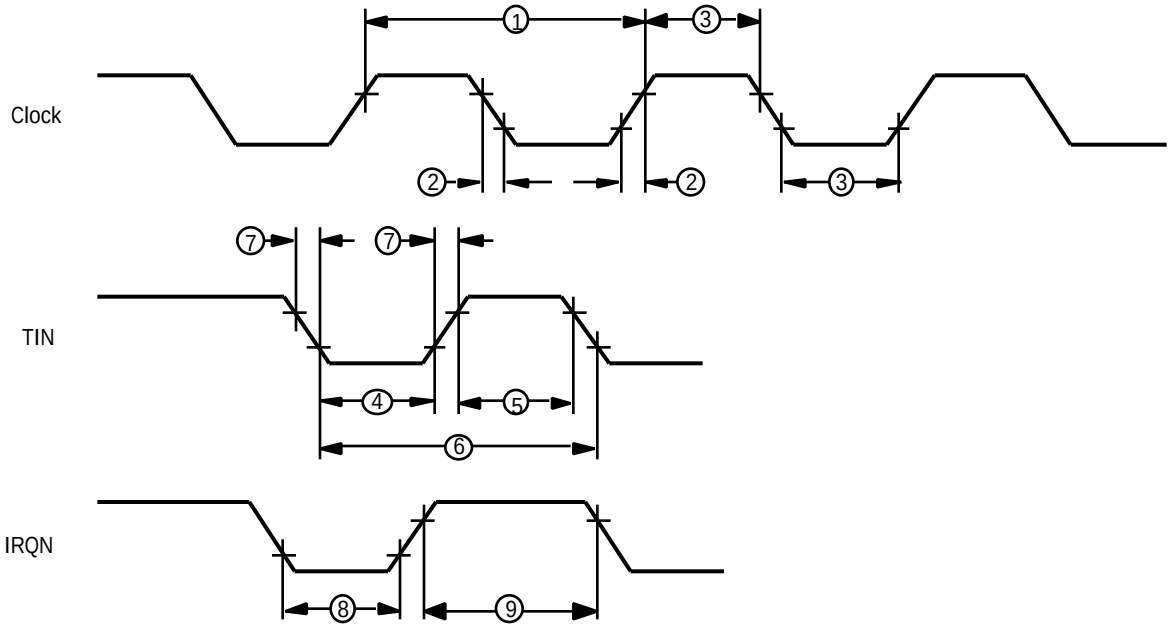


Figure 10. Additional Timing

AC CHARACTERISTICS

Additional Timing Table
Z86C61/62/96

			T_A = 0°C to +70°C 20/16 MHz		TA = -40°C to +105°C 20/16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	1
3	TwC	Input Clock Width	25		25		ns	1
4	TwTinL	Timer Input Low Width	75		75		ns	2
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	2
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	2
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	2
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	2,4
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	2,5
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	2,3

Notes:
1. Clock timing references use $0.8V_{CC}$ for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request through Port 3.
4. Interrupt request through Port 3 (P33-P31).
5. Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Diagrams

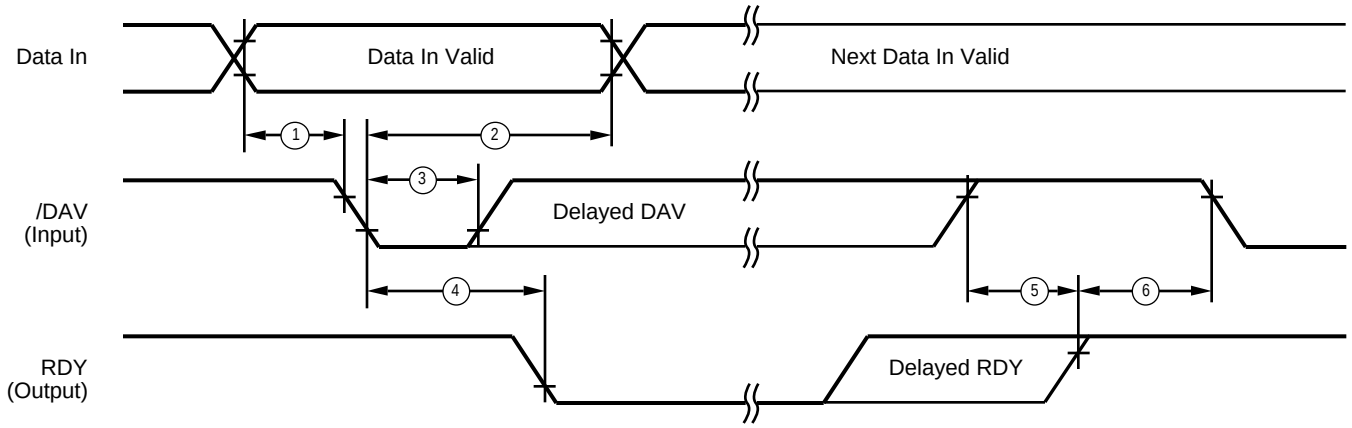


Figure 11. Input Handshake Timing

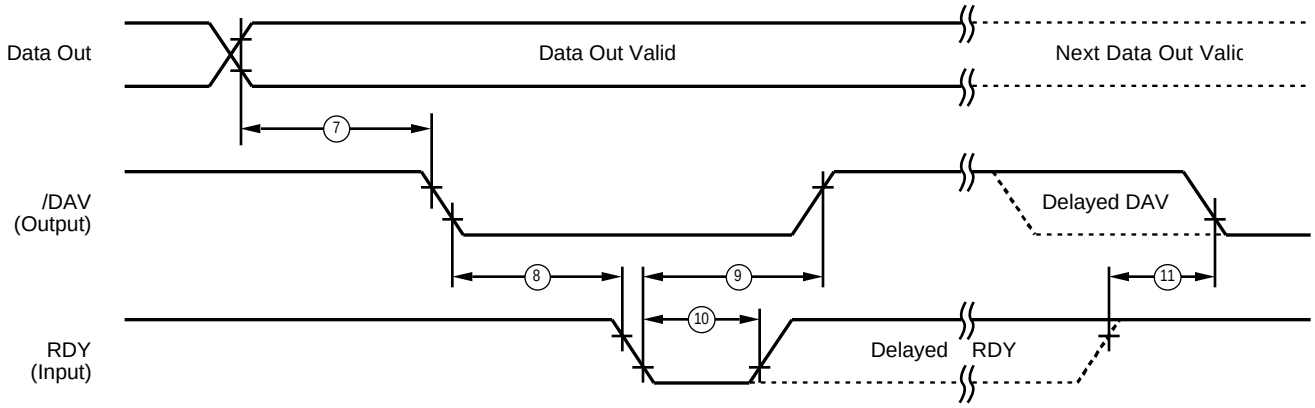


Figure 12. Output Handshake Timing

PIN FUNCTIONS

R//RL (input, active Low). This pin when connected to GND disables the internal ROM and forces the device to function as a Z86C96 ROMless Z8. (Note: When left unconnected or pulled High to VCC the part functions as a normal Z86C61/62 ROM version.) This pin is only available on the 44-pin version of the Z86C61, and both versions of the Z86C62.

/DS (output, active Low). Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available prior to the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

/AS (output, active Low). Address Strobe is pulsed once at the beginning of each machine cycle. Address out-put is through Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS can be placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

XTAL1, XTAL2 Crystal 1, Crystal 2 (time-based input and output, respectively). These pins connect a parallel-resonant crystal, ceramic resonator, LC, or any external single-phase clock to the on-chip oscillator and buffer.

R//W (output, write Low). The Read/Write signal is Low when the MCU is writing to the external program or data memory.

/RESET (input, active Low). To avoid asynchronous and noisy reset problems, the Z86C61/62/96 is equipped with a reset filter of four external clocks (4TpC). If the external /RESET signal is less than 4TpC in duration, no reset occurs.

On the fifth clock after the /RESET is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks, or for the duration of the external /RESET, whichever is longer. During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. When /RESET is deactivated, program execution begins at location 000C (HEX). Reset time must be held Low for 50 ms, or until VCC is stable, whichever is longer.

/P0DS Port 0 Data Strobe (output, active Low). Signal used to emulate Port 0 when in ROMless mode.

/P1DS Port 1 Data Strobe (output, active Low). Signal used to emulate Port 1 when in ROMless mode.

/DTIMERS Disable Timers (input, active Low). All timers are stopped by the Low level at this pin. This pin has an internal pull up resistor.

SCLK (output). System clock pin.

/SYNC Instruction SYNC Signal (output, active Low). This signal indicates the last clock of the current executing instruction.

Port 0 (P07-P00). Port 0 is an 8-bit, nibble programmable, bidirectional, TTL compatible port. These eight I/O lines can be configured under software control as a nibble I/O port, or as an address port for interfacing external memory. When used as an I/O port, Port 0 may be placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0 (Data Available and Ready). Handshake signal assignment is dictated by the I/O direction of the upper nibble P07-P04. The lower nibble must have the same direction as the upper nibble to be under handshake control.

For external memory references, Port 0 can provide address bits A11-A8 (lower nibble) or A15-A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 Mode register.

In ROMless mode, after a hardware reset, Port 0 lines are defined as address lines A15-A8, and extended timing is set to accommodate slow memory access. The initialization routine includes reconfiguration to eliminate this extended timing mode (Figure 14).

PIN FUNCTIONS (Continued)

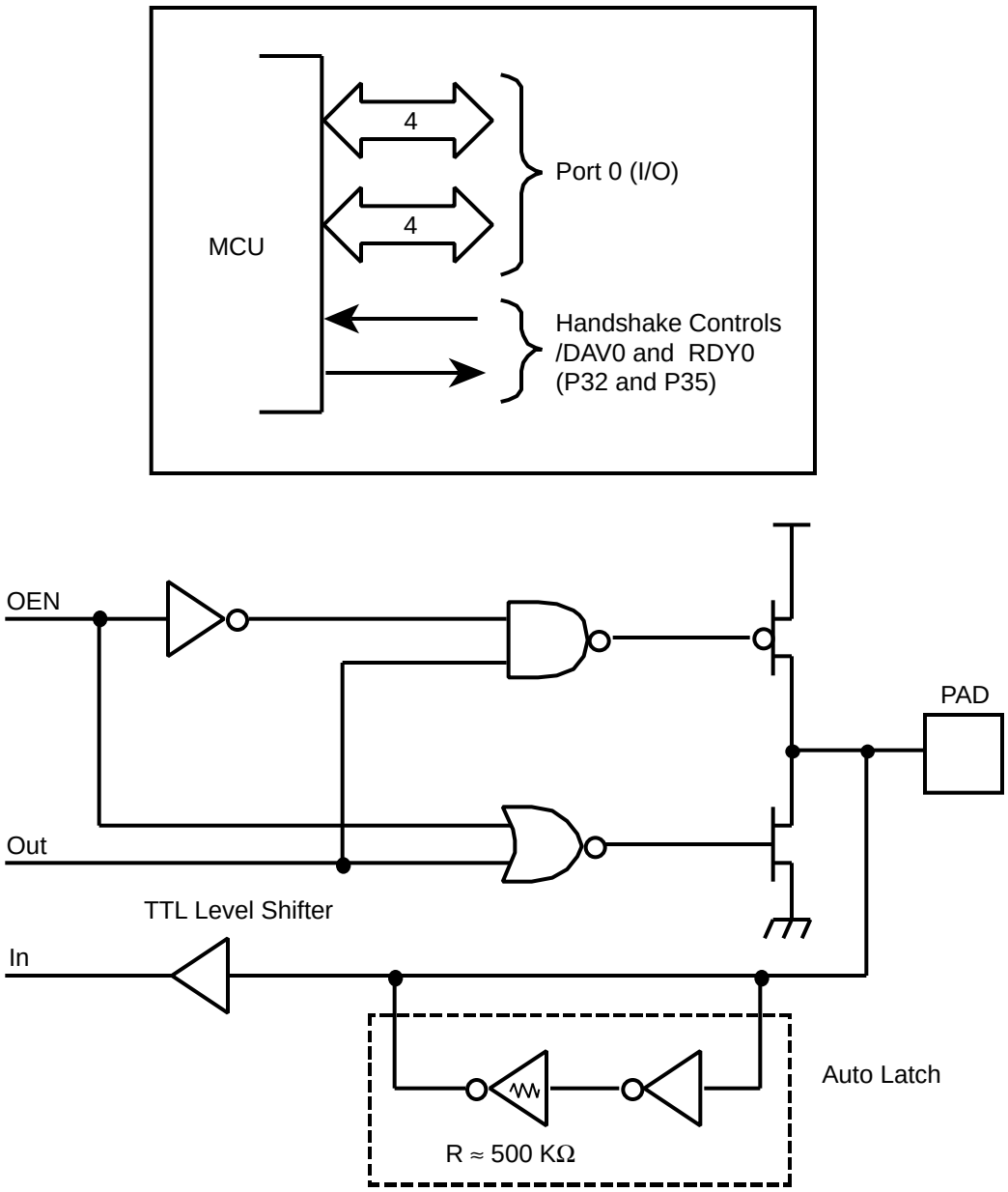


Figure 13. Port 0 Configuration

PIN FUNCTIONS (Continued)

Port 3 can be configured under software control to provide the following control functions: handshake for Ports 0 and 2 (/DAV and RDY); four external interrupt request signals (IRQ3-IRQ0); timer input and output signals (T_{IN} and T_{OUT}), and Data Memory Select (/DM).

Table 6. Port 3 Pin Assignments

Pin	I/O	CTC1	Int.	P0 HS	P1 HS	P2 HS	UART	Ext
P30	IN		IRQ3				Serial In	
P31	IN	T_{IN}	IRQ2			D/R		
P32	IN		IRQ0	D/R				
P33	IN		IRQ1		D/R			
P34	OUT				R/D			DM
P35	OUT			R/D				
P36	OUT	T_{OUT}				R/D		
P37	OUT						Serial Out	
T0			IRQ4					
T1			IRQ5					

Notes:
HS = Handshake Signals
D = Data Available
R = Ready

Uart Operation

Port 3 lines P30 and P37, can be programmed as serial I/O lines for full-duplex serial asynchronous receiver/transmitter operation. The bit rate is controlled by the Counter/Timer0.

The Z86C61/62/96 automatically adds a start bit and two stop bits to transmitted data (Figure 17). Odd parity is also available as an option. Eight data bits are always transmitted, regardless of parity selection. If parity is enabled, the eighth bit is the odd parity bit. An interrupt request (IRQ4) is generated on all transmitted characters.

Received data must have a start bit, eight data bits and at least one stop bit. If parity is on, bit 7 of the received data is replaced by a parity error flag. Received characters generate the IRQ3 interrupt request.

Note: UART function is only available in standard timing mode (i.e., P01M D5 = 0).

FUNCTIONAL DESCRIPTION

Address Space

Program Memory. The Z86C61/62 can address up to 48 KB of external program memory (Figure 19). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six 16-bit vectors that correspond to the six available interrupts. For ROM mode, byte 13 to byte 16383 consists of on-chip ROM. At addresses 16384 and greater, the Z86C61/62 executes external program memory fetches. The Z86C96, and the Z86C61/62 in ROMless mode, can address up to 64 KB of external program memory. Program execution begins at external location 000CH after a reset.

Data Memory (/DM). The ROM version can address up to 48 KB of external data memory space beginning at location 16384. The ROMless version can address up to 64 KB of external data memory. External data memory may be included with, or separated from, the external program memory space. /DM, an optional I/O function that can be programmed to appear on pin P34, is used to distinguish between data and program memory space (Figure 20). The state of the /DM signal is controlled by the type instruction being executed. An LDC opcode references PROGRAM (/DM inactive) memory, and an LDE instruction references DATA (/DM active Low) memory.

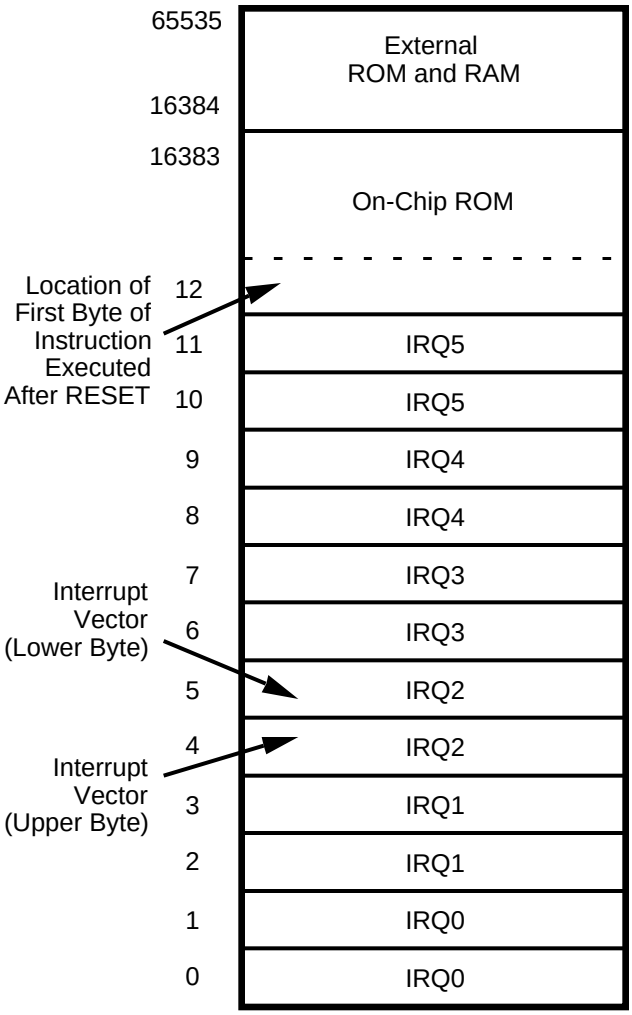


Figure 19. Program Memory Configuration

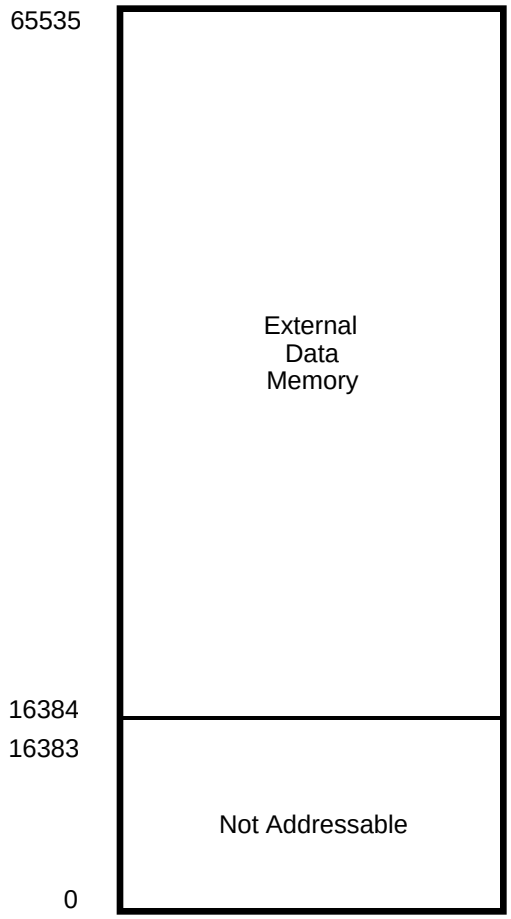


Figure 20. Data Memory Configuration

FUNCTIONAL DESCRIPTION (Continued)

Register File. The Register File consists of four I/O port registers, 236 general-purpose registers and 16 control and status registers (Figure 18). There are eight further registers for I/O ports 4, 5 and 6 in the Expanded Register File (Bank F, R9-R2) (Figure 20).

The instructions can access registers directly or indirectly through an 8-bit address field. The Z86C61/62/96 also allows short 4-bit register addressing using the Register Pointer (Figure 21). In the 4-bit mode, the Register File is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working-register group.

Note: Register Bank E0-EF can only be accessed through working registers and indirect addressing modes.

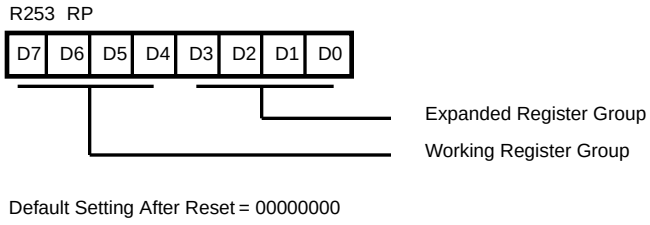


Figure 21. Register Pointer Register

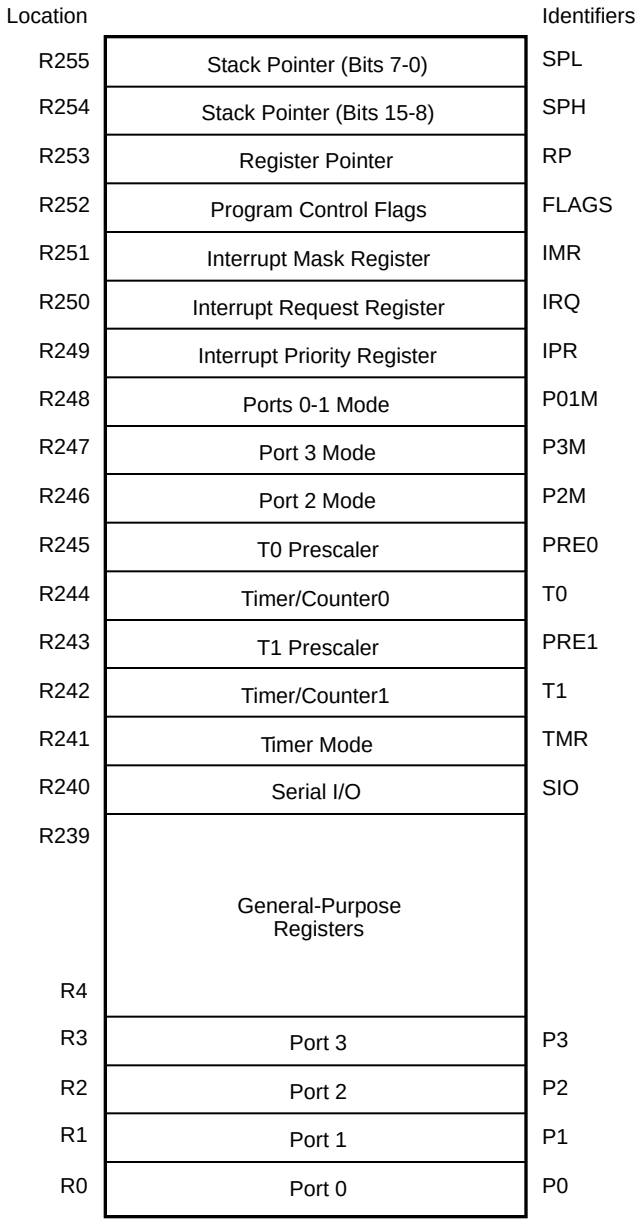


Figure 22. Register File

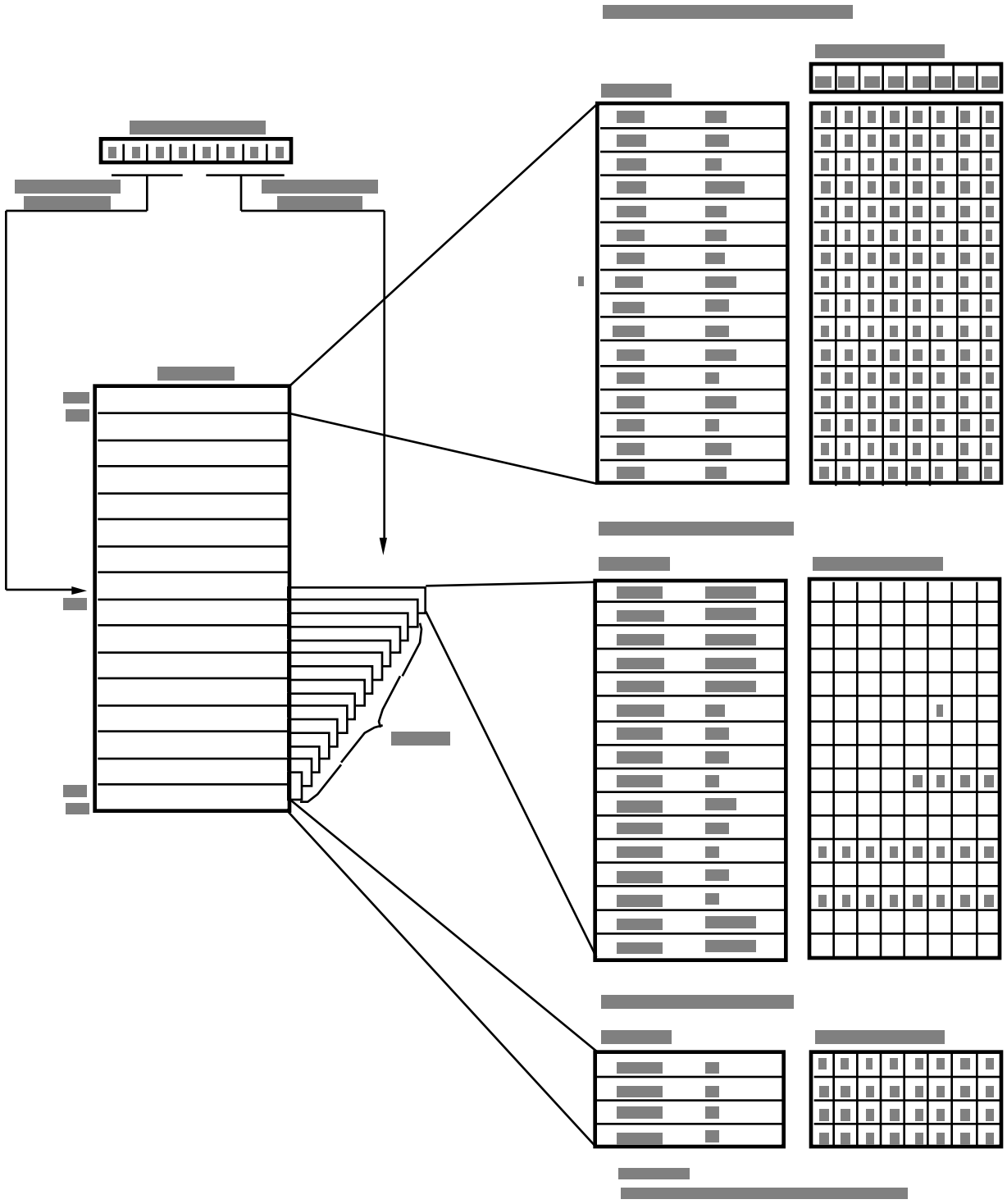


Figure 23. Expanded Register File Architecture

FUNCTIONAL DESCRIPTION (Continued)

Expanded Register File. The register file has been expanded to allow for additional system control registers, and for mapping of additional peripheral devices along with I/O ports into the register address area. The Z8 register address space R0 through R15 has now been implemented as 16 groups of 16 registers per group. These register groups are known as the ERF (Expanded Register File). Bits 7-4 of Register RP select the working register group. Bits 3-0 of Register RP select the expanded register group (Figure 21). Eight I/O port registers reside in the Expanded Register File at Bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

The upper nibble of the register pointer (Figure 20) selects which group of 16 bytes in the register file, out of the full 236, will be accessed. The lower nibble selects the expanded register file bank and in the case of the Z86C61/62/96, only Bank F is implemented. A 0H in the lower nibble will allow the normal register file to be addressed, but any other value from 1H to FH will exchange the lower 16 registers in favor of an expanded register group of 16 registers.

For example:

Z86C61: (See Figures 21 and 22)

R253 RP = 00H	R0 = Port 0	R2 = Port 2
	R1 = Port 1	R3 = Port 3

But If:

R253 RP = 0FH
R0 = Reserved
R1 = Reserved
R2 = Port 4
R3 = Port 4, Direction Register
R9 = Port 6, Mode Register

Further examples:

SRP #0FH	Set working group 0 and Bank F
LD R2, #10010110	Load value into Port 4 using working register addressing.
LD 2, #10010110	Load value into Port 4 using absolute addressing.
LD 9, #11110000	Load value into Port 6 mode.
SRP #1FH	Set working group 1 and Bank F
LD R2, #11010110	Load value into general purpose register 12H
LD 12H, #11010110	Load value into general purpose register 12H
LD 2, #10010110	Load value into Port 4

RAM Protect. The upper portion of the RAM's address spaces 80FH to EFH (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

ROM Protect. The first 16 Kbytes of program memory is mask programmable. A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC, LDCI, LDE, and LDEI instructions by external program memory when pointing to internal memory locations. Therefore these instructions can be used only when they are executed from internal memory, or if they are executed from external memory and pointing to external memory locations.

The ROM Protect option is mask-programmable, to be selected by the customer at the time when the ROM code is submitted.

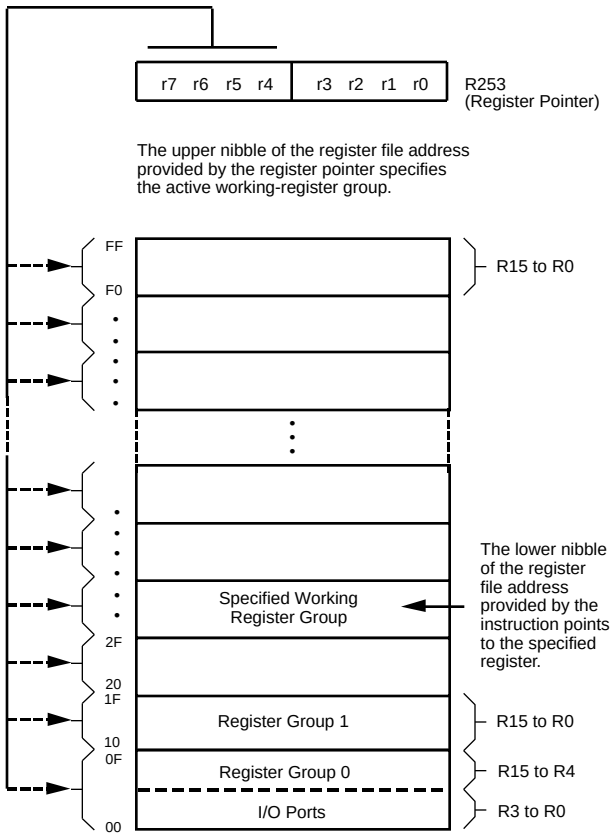


Figure 24. Register Pointer

Stack. The Z86C61/62/96 has a 16-bit Stack Pointer (R255-R254) used for external stack that resides anywhere in the data memory for the ROMless mode, but only from 16384 to 65535 in the ROM mode. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 236 general-purpose registers (R239-R4). The high byte of the Stack Pointer (SPH-Bit 8-15) can be used as a general purpose register when using internal stack only.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 22).

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When both the counters and prescaler reach the end of the count, a timer interrupt request, IRQ4 (T0) or IRQ5 (T1), is generated.

The counter can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counter, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input through Port 3. The Timer Mode register configures the external timer input (P31) as an external clock, a trigger input that can be retriggerable or non-retriggerable, or as a gate input for the internal clock. Port 3, line P36, also serves as a timer output (TOUT) through which T0, T1 or the internal clock can be output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Z8 CONTROL REGISTER DIAGRAMS

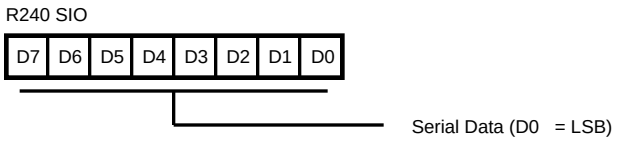


Figure 28. Serial I/O Register (F0H: Read/Writ e)

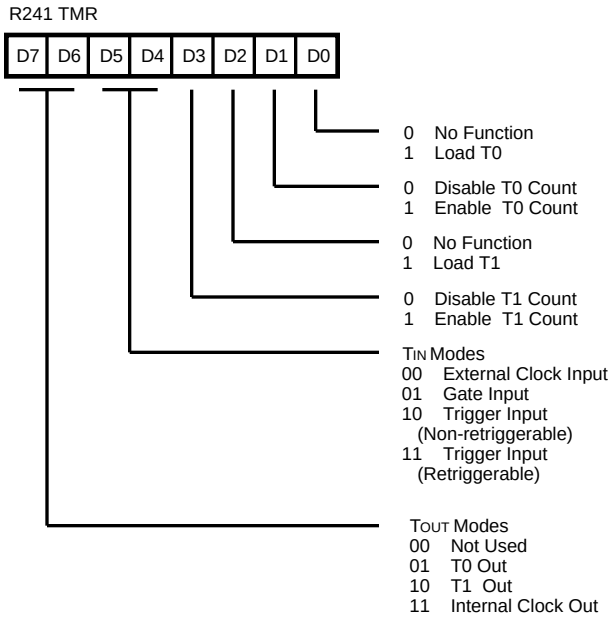


Figure 29. Timer Mode Register (F1H: Read/Writ e)

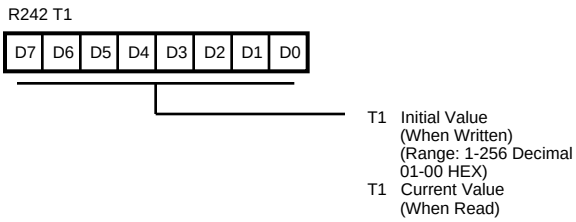


Figure 30. Counter/Timer1 Register (F2H: Read/Writ e)

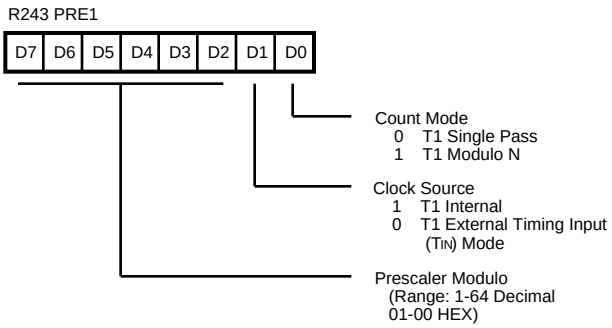


Figure 31. Prescaler 1 Register (F3H: Write Only)

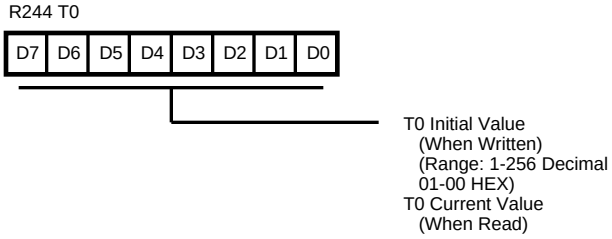


Figure 32. Counter/Timer 0 Register (F4H: Read/Writ e)

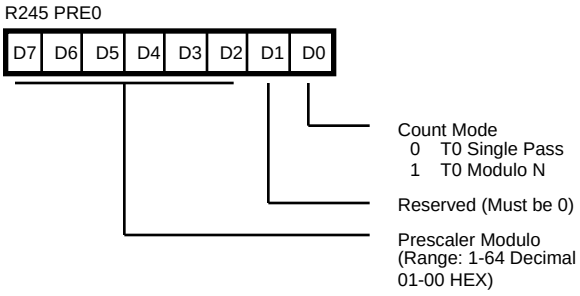


Figure 33. Prescaler 0 Register (F5H: Write Only)

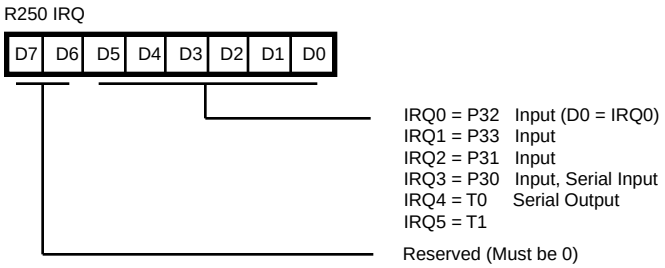


Figure 38. Interrupt Request Register (FAH: Read/Write)

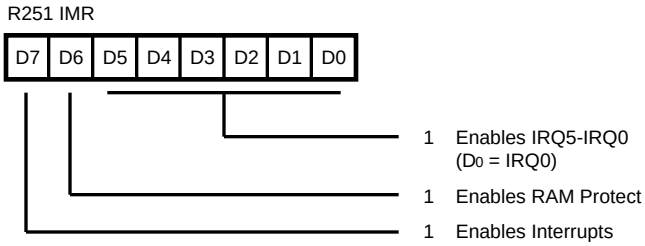


Figure 39. Interrupt Mask Register (FBH: Read/Write)

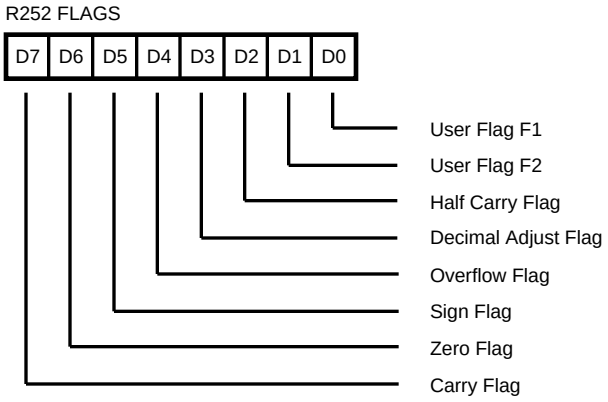


Figure 40. Flag Register (FCH: Read/Write)

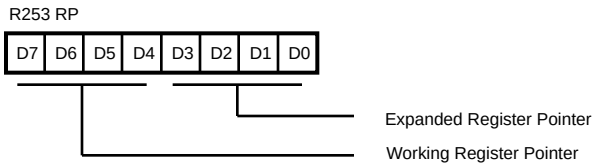


Figure 41. Register Pointer Register (FDH: Read/Write)

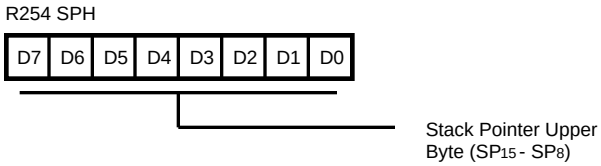


Figure 42. Stack Pointer Register (FEH: Read/Write)

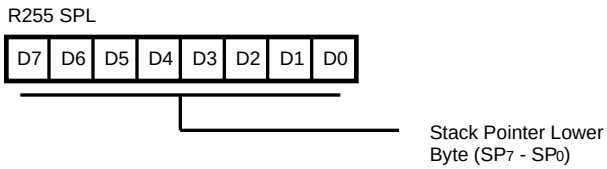
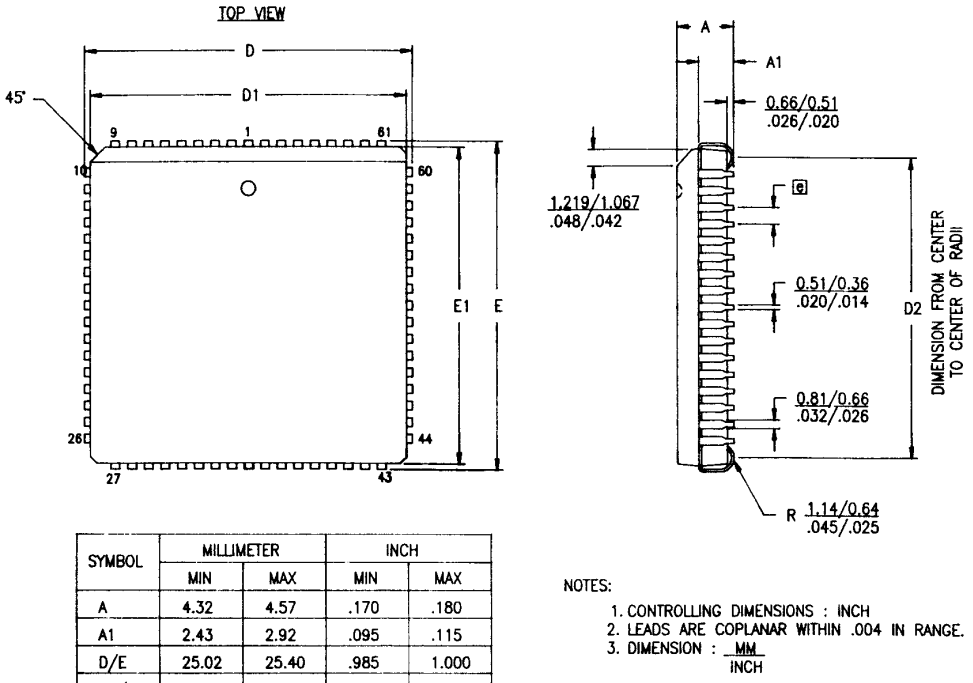


Figure 43. Stack Pointer Register (FFH: Read/Write)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.32	4.57	.170	.180
A1	2.43	2.92	.095	.115
D/E	25.02	25.40	.985	1.000
D1/E1	24.13	24.33	.950	.958
D2	22.86	23.62	.900	.930
e	1.27 TYP		.050 TYP	

NOTES:

1. CONTROLLING DIMENSIONS : INCH
2. LEADS ARE COPLANAR WITHIN .004 IN RANGE.
3. DIMENSION : MM / INCH

Figure 55. 68-Pin PLCC Package Diagram