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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8
Core Size	8-Bit
Speed	20MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	-
Number of I/O	52
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	236 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	64-DIP (0.750", 19.05mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z86c9620psg

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with the real-time tasks, such as counting/timing and serial data communication, the Z86C61/62/96 offers two on-chip counter/timers with a large number of user selectable modes, and an on-board UART (Figures 1, 2, and 3).

Notes: All Signals with a preceding front slash, "/", are active Low. For example B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

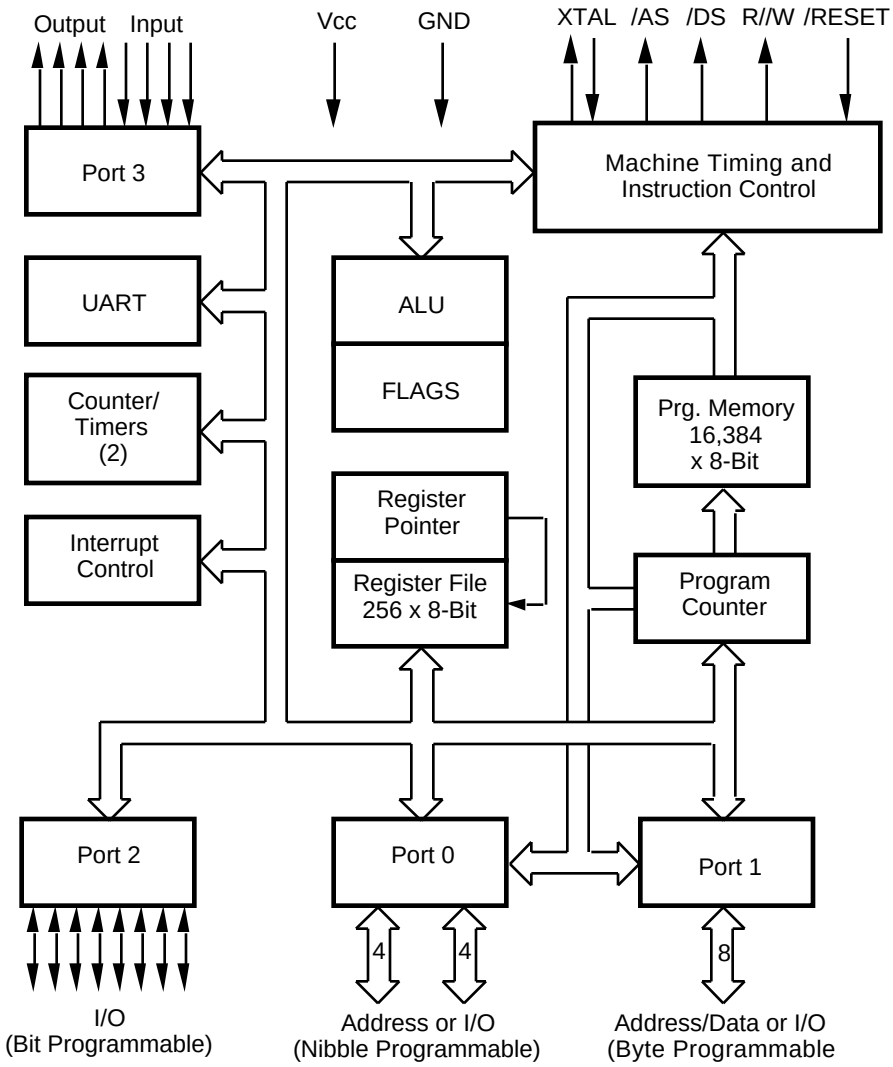

Figure 1. Z86C61 Functional Block Diagram

PIN DESCRIPTION (Continued)

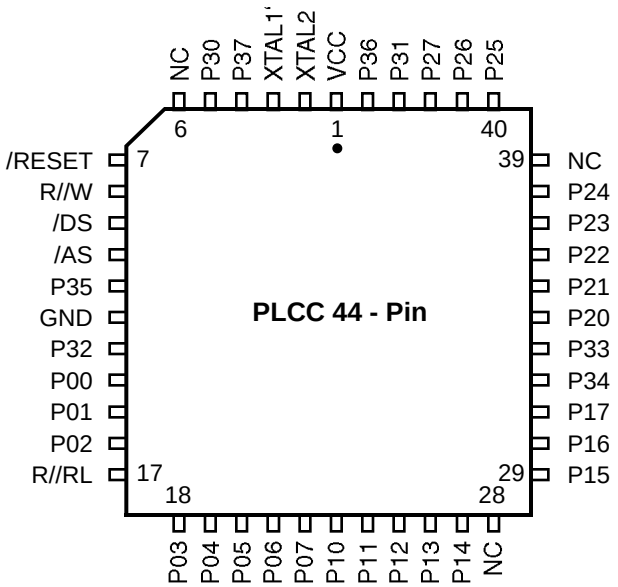

Figure 5. Z86C61 44-Pin PLCC Pin Assignments

Table 2. Z86C61 44-Pin PLCC Pin Assignments

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	P37	Port 3, Pin 7	Output
5	P30	Port 3, Pin 0	Input
6	N/C	Not Connected	Input
7	/RESET	Reset	Input
8	R//W	Read/Write	Output
9	/DS	Data Strobe	Output
10	/AS	Address Strobe	Output
11	P35	Port 3, Pin 5	Output
12	GND	Ground	Input
13	P32	Port 3, Pin 2	Input
14-16	P02-P00	Port 0, Pins 0,1,2	In/Output
17	R//RL	ROM/ROMless control	Input
18-22	P07-P03	Port 0, Pins 3,4,5,6,7	In/Output

DC ELECTRICAL CHARACTERISTICS

Z86C61/62/96

		T_A = 0°C to +70°C		T_A = -40°C to +105°C		Typical		
Sym	**Parameter**	**Min**	**Max**	**Min**	**Max**	**@ 25°C**	**Units**	**Conditions**
	Max Input Voltage		7		7		V	I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS} – 0.3	0.8	V_{SS} – 0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC} + 0.3	2	V_{CC} + 0.3		V	
V_{IL}	Input Low Voltage	V_{SS} – 0.3	0.2 V_{CC}	V_{SS} – 0.3	0.2 V_{CC}		V	
V_{OH}	Output High Voltage	2.4		2.4			V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC} – 100 mV		V_{CC} – 100 mV		V	I_{OH} = –100 µA
V_{OL}	Output Low Voltage		0.4		0.4		V	I_{OL} = +5.0 mA [3]
V_{OL}	Output Low Voltage		0.6		0.6		V	I_{OL} = +4.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85 V_{CC}	V_{CC} + 0.3	0.85 V_{CC}	V_{CC} + 0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2 V_{CC}	–0.3	0.2 V_{CC}		V	
I_{IL}	Input Leakage	–2	2	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2	–2	2		µA	V_{IN} = 0_V, V_{CC}
I_{IR}	Reset Input Current		–80		–80		µA	VRL = 0 V
I_{CC}	Supply Current		35		35	24	mA	[1] @ 16 MHz
I_{CC}	Supply Current		40		40	30	mA	[1] @ 20 MHz
I_{CC1}	Standby Current		15		15	4.5	mA	[1] HALT Mode V_{IN} = 0 V, V_{CC} @ 16 MHz
I_{CC2}	Standby Current		10		20	5	µA	[1] STOP Mode V_{IN} = 0 V, V_{CC}

Notes:

1. All inputs driven to either 0V or V_{CC}, outputs floating.
2. V_{CC} = 3.0V to 3.6V
3. V_{CC} = 4.5V to 5.5V

AC CHARACTERISTICS

External I/O or Memory Read and Write Timing
Z86C61/62/96 (16 MHz)

			T_A = 0°C to +70°C 16 MHz		T_A = -40°C to +105°C 16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TdA(AS)	Address Valid to /AS rise Delay	25		25		ns	2,3
2	TdAS(A)	/AS rise to Address Float Delay	35		35		ns	2,3
3	TdAS(DR)	/AS rise to Read Data Req'd Valid		150		150	ns	1,2,3
4	TwAS	/AS Low Width	40		40		ns	2,3
5	TdAZ(DS)	Address Float to /DS fall	0		0		ns	
6	TwDSR	/DS (Read) Low Width		135		135	ns	1,2,3
7	TwDSW	/DS (Write) Low Width	80		80		ns	1,2,3
8	TdDSR(DR)	/DS fall to Read Data Req'd Valid	75		75		ns	1,2,3
9	ThDR(DS)	Read Data to /DS rise Hold Time	0		0		ns	2,3
10	TdDS(A)	/DS rise to Address Active Delay	50		50		ns	2,3
11	TdDS(AS)	/DS rise to /AS fall Delay	35		35		ns	2,3
12	TdR/W(AS)	R//W Valid to /AS rise Delay	25		25		ns	2,3
13	TdDS(R/W)	/DS rise to R//W Not Valid	35		35		ns	2,3
14	TdDW(DSW)	Write Data Valid to /DS fall (Write) Delay	25		25		ns	2,3
15	TdDS(DW)	/DS rise to Write Data Not Valid Delay	35		35		ns	2,3
16	TdA(DR)	Address Valid to Read Data Req'd Valid		210		210	ns	1,2,3
17	TdAS(DS)	/AS rise to /DS fall Delay	45		45		ns	2,3
18	TdDM(AS)	/DM Valid to /AS rise Delay	25		25		ns	2,3

Notes:

1. When using extended memory timing add 2 TpC.
2. Timing numbers given are for minimum TpC.
3. See clock cycle dependent characteristics table.

Standard Test Load

All timing references use 2.0 V for a logic 1 and 0.8 V for a logic 0.

Table 5. Clock Dependent Formulas

Number	Symbol	Equation
1	TdA(AS)	0.40 TpC + 0.32
2	TdAS(A)	0.59 TpC – 3.25
3	TdAS(DR)	2.83 TpC + 6.14
4	TwAS	0.66 TpC – 1.65
6	TwDSR	2.33 TpC – 10.56
7	TwDSW	1.27 TpC + 1.67

Table 5. Clock Dependent Formulas

Number	Symbol	Equation
8	TdDSR(DR)	1.97 TpC – 42.5
10	TdDS(A)	0.8 TpC
11	TdDS(AS)	0.59 TpC – 3.14
12	TdR/W(AS)	0.4 TpC
13	TdDS(R/W)	0.8 TpC – 15
14	TdDW(DSW)	0.4 TpC
15	TdDS(DW)	0.88 TpC – 19
16	TdA(DR)	4 TpC – 20
17	TdAS(DS)	0.91 TpC – 10.7
18	TdDM(AS)	0.9 TpC – 26.3

AC CHARACTERISTICS

Additional Timing Table
Z86C61/62/96

			T_A = 0°C to +70°C 20/16 MHz		TA = -40°C to +105°C 20/16 MHz			
No	**Symbol**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
1	TpC	Input Clock Period	50/62.5	1000	50/62.5	1000	ns	1
2	TrC,TfC	Clock Input Rise & Fall Times		10	10		ns	1
3	TwC	Input Clock Width	25		25		ns	1
4	TwTinL	Timer Input Low Width	75		75		ns	2
5	TwTinH	Timer Input High Width	5 TpC		5 TpC		ns	2
6	TpTin	Timer Input Period	8 TpC		8 TpC		ns	2
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		100		ns	2
8a	TwIL	Interrupt Request Input Low Times	70		50		ns	2,4
8b	TwIL	Interrupt Request Input Low Times	5 TpC		5 TpC		ns	2,5
9	TwIH	Interrupt Request Input High Times	5 TpC		5 TpC		ns	2,3

Notes:
1. Clock timing references use $0.8V_{CC}$ for a logic 1 and 0.8V for a logic 0.
2. Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
3. Interrupt references request through Port 3.
4. Interrupt request through Port 3 (P33-P31).
5. Interrupt request through Port 30.

AC CHARACTERISTICS

Handshake Timing Table
Z86C61/62/96

			T_A = 0°C to +70°C		T_A = –40°C to +105°C		
			20/16 MHz		20/16 MHZ		Data
No	Symbol	Parameter	Min	Max	Min	Max	Direction
1	TsDI(DAV)	Data In Setup Time	0		0		IN
2	ThDI(DAV)	Data In Hold Time	145		145		IN
3	TwDAV	Data Available Width	110		110		IN
4	TdDAVI(RDY)	DAV fall to RDY fall Delay	115		115		IN
5	TdDAVId(RDY)	DAV rise to RDY rise Delay	115		115		IN
6	TdRDY0(DAV)	RDY rise to DAV fall Delay	0		0		IN
7	TdDO(DAV)	Data Out to DAV fall Delay	TpC		TpC		OUT
8	TdDAV0(RDY)	DAV fall to RDY fall Delay	0		0		OUT
9	TdRDY0(DAV)	RDY fall to DAV rise Delay	115		115		OUT
10	TwRDY	RDY Width	110		110		OUT
11	TdRDY0d(DAV)	RDY rise to DAV fall Delay	115		115		OUT