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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f630t-i-ml

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2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1 — PERIPHERAL INTERRUPT REGISTER 1 (ADDRESS: 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
EEIF	ADIF	—	—	CMIF	—	—	TMR1IF
bit 7				bit 0			

- bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
 1 = The write operation completed (must be cleared in software)
 0 = The write operation has not completed or has not been started
- bit 6 **ADIF:** A/D Converter Interrupt Flag bit (PIC16F676 only)
 1 = The A/D conversion is complete (must be cleared in software)
 0 = The A/D conversion is not complete
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 **CMIF:** Comparator Interrupt Flag bit
 1 = Comparator input has changed (must be cleared in software)
 0 = Comparator input has not changed
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
 1 = TMR1 register overflowed (must be cleared in software)
 0 = TMR1 register did not overflow

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

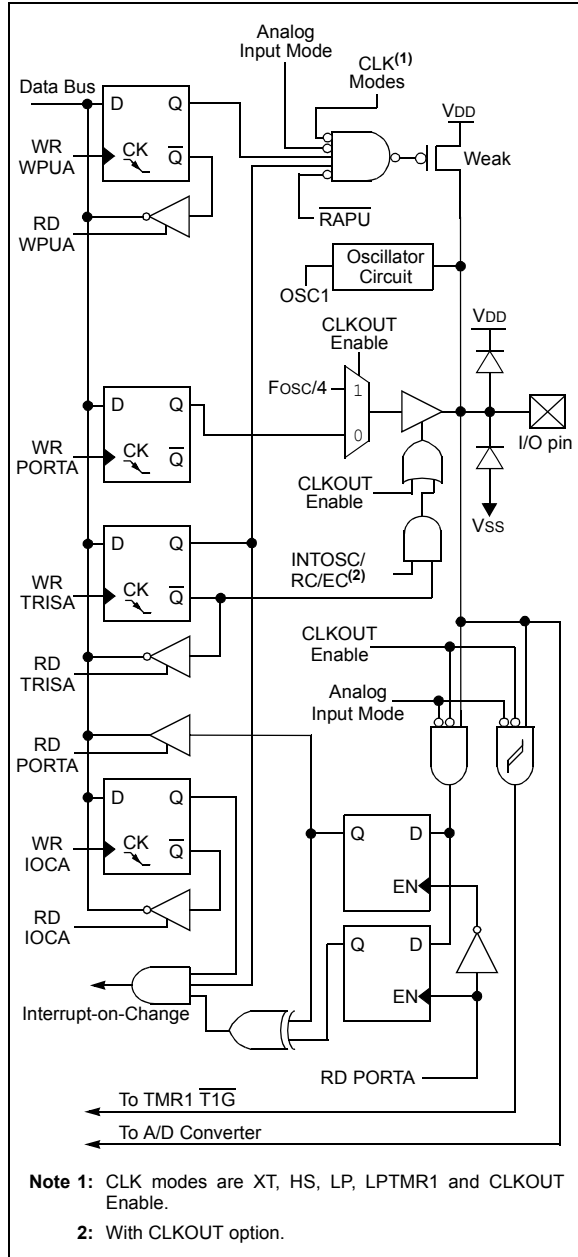
PIC16F630/676

3.2.3.5 RA4/AN3/T1G/OSC2/CLKOUT

Figure 3-4 shows the diagram for this pin. The RA4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC16F676 only)
- a TMR1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 3-4: BLOCK DIAGRAM OF RA4

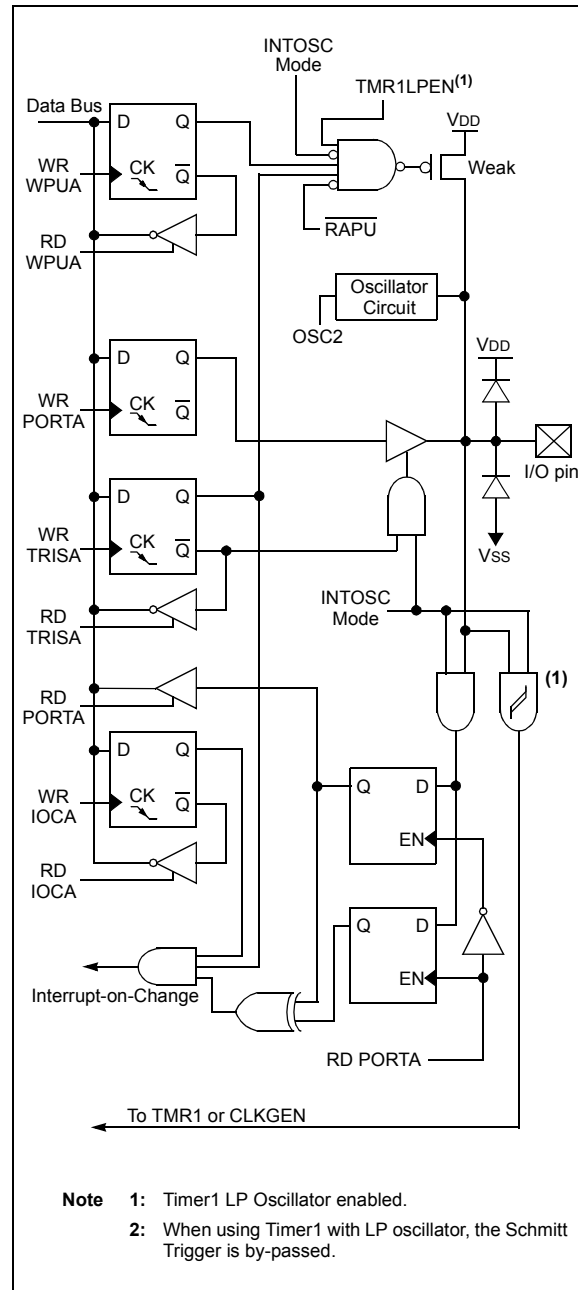


3.2.3.6 RA5/T1CKI/OSC1/CLKIN

Figure 3-5 shows the diagram for this pin. The RA5 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 3-5: BLOCK DIAGRAM OF RA5



REGISTER 3-5: PORTC — PORTC REGISTER (ADDRESS: 07h)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	
—	—	RC5	RC4	RC3	RC2	RC1	RC0	
bit 7								bit 0

bit 7-6: **Unimplemented:** Read as '0'

bit 5-0: **PORTC<5:0>:** General Purpose I/O pin bits

1 = Port pin is >V_{IH}

0 = Port pin is <V_{IL}

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 3-6: TRISC — PORTC TRI-STATE REGISTER (ADDRESS: 87h)

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0
bit 7		bit 0					

bit 7-6: **Unimplemented:** Read as '0'

bit 5-0: **TRISC<5:0>:** PORTC Tri-State Control bits

1 = PORTC pin configured as an input (tri-stated)

0 = PORTC pin configured as an output

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

TABLE 3-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
07h	PORTC	—	—	RC5	RC4	RC3	RC2	RC1	RC0	--xx xxxx	--uu uuuu
87h	TRISC	—	—	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	--11 1111	--11 1111
91h	ANSEL ⁽¹⁾	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	1111 1111	1111 1111

Note 1: PIC16F676 only.

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.

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4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and

a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

Note: The ANSEL (91h) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

REGISTER 4-1: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RAPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

- bit 7 **RAPU:** PORTA Pull-up Enable bit
1 = PORTA pull-ups are disabled
0 = PORTA pull-ups are enabled by individual PORT latch values
- bit 6 **INTEDG:** Interrupt Edge Select bit
1 = Interrupt on rising edge of RA2/INT pin
0 = Interrupt on falling edge of RA2/INT pin
- bit 5 **T0CS:** TMR0 Clock Source Select bit
1 = Transition on RA2/T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)
- bit 4 **T0SE:** TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on RA2/T0CKI pin
0 = Increment on low-to-high transition on RA2/T0CKI pin
- bit 3 **PSA:** Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module
- bit 2-0 **PS2:PS0:** Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
- n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

6.1 Comparator Operation

A single comparator is shown in Figure 6-1, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 6-1 represent the uncertainty due to input offsets and response time.

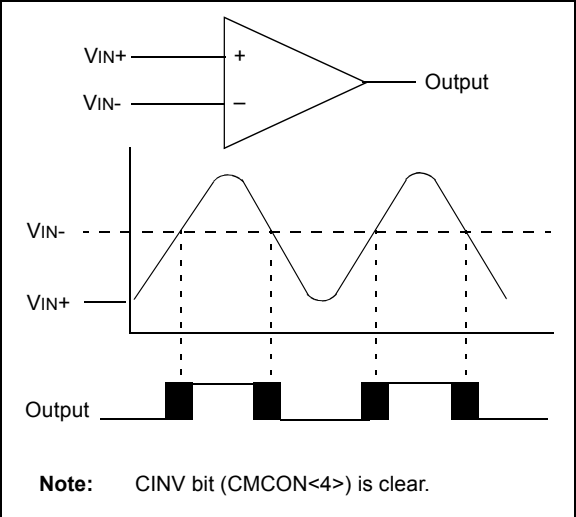
Note: To use CIN+ and CIN- pins as analog inputs, the appropriate bits must be programmed in the CMCON (19h) register.

The polarity of the comparator output can be inverted by setting the CINV bit (CMCON<4>). Clearing CINV results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 6-1.

TABLE 6-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	CINV	COUT
VIN- > VIN+	0	0
VIN- < VIN+	0	1
VIN- > VIN+	1	1
VIN- < VIN+	1	0

FIGURE 6-1: SINGLE COMPARATOR



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REGISTER 7-3: ANSEL — ANALOG SELECT REGISTER (ADDRESS: 91h) (PIC16F676 ONLY)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7				bit 0			

bit 7-0: **ANS<7:0>**: Analog Select between analog or digital function on pins AN<7:0>, respectively.
1 = Analog input. Pin is assigned as analog input.⁽¹⁾
0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

7.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 7-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the impedance

is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the PIC® Mid-Range Reference Manual (DS33023).

EQUATION 7-1: ACQUISITION TIME

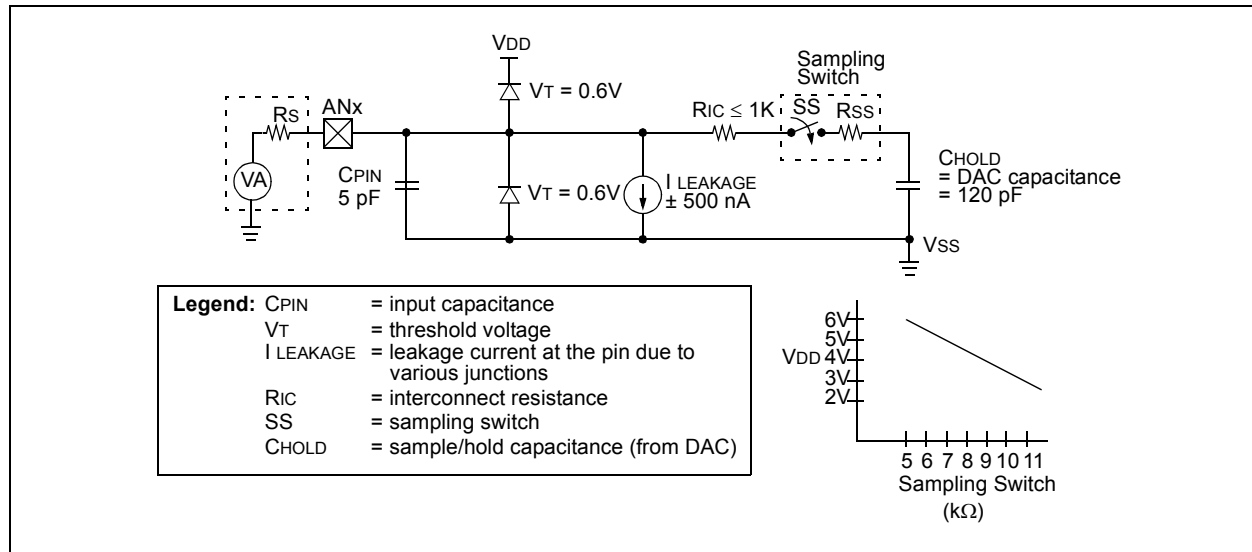
$$\begin{aligned}
 T_{ACQ} &= \text{Amplifier Settling Time} + \\
 &\quad \text{Hold Capacitor Charging Time} + \\
 &\quad \text{Temperature Coefficient} \\
 &= T_{AMP} + T_C + T_{COFF} \\
 &= 2\mu s + T_C + [(\text{Temperature} - 25^\circ\text{C})(0.05\mu s/^\circ\text{C})] \\
 T_C &= \text{CHOLD} (R_{IC} + R_{SS} + R_S) \ln(1/2047) \\
 &= -120\text{pF} (1\text{k}\Omega + 7\text{k}\Omega + 10\text{k}\Omega) \ln(0.0004885) \\
 &= 16.47\mu s \\
 T_{ACQ} &= 2\mu s + 16.47\mu s + [(50^\circ\text{C} - 25^\circ\text{C})(0.05\mu s/^\circ\text{C})] \\
 &= 19.72\mu s
 \end{aligned}$$

Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

FIGURE 7-3: ANALOG INPUT MODEL



8.3 READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>), as shown in Example 8-1. The data is available in the very next cycle in the EEDATA register. Therefore, it can be read in the next instruction. EEDATA holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 8-1: DATA EEPROM READ

```
BSF    STATUS,RP0    ;Bank 1
MOVLW  CONFIG_ADDR   ;
MOVWF  EEADR         ;Address to read
BSF    EECON1,RD      ;EE Read
MOVF   EEDATA,W       ;Move data to W
```

8.4 WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 8-2.

EXAMPLE 8-2: DATA EEPROM WRITE

Required Sequence	BSF	STATUS,RP0	;Bank 1
	BSF	EECON1,WREN	;Enable write
	BCF	INTCON,GIE	;Disable INTs
	MOVLW	55h	;Unlock write
	MOVWF	EECON2	;
	MOVLW	AAh	;
	MOVWF	EECON2	;
	BSF	EECON1,WR	;Start the write
	BSF	INTCON,GIE	;Enable INTs

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR<7>) register must be cleared by software.

8.5 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the data EEPROM should be verified (see Example 8-3) to the desired value to be written.

EXAMPLE 8-3: WRITE VERIFY

```
BCF    STATUS,RP0    ;Bank 0
:      ;Any code
BSF    STATUS,RP0    ;Bank 1 READ
MOVF   EEDATA,W       ;EEDATA not changed
                        ;from previous write
BSF    EECON1,RD      ;YES, Read the
                        ;value written
XORWF  EEDATA,W
BTFS   STATUS,Z        ;Is data the same
GOTO   WRITE_ERR      ;No, handle error
:      ;Yes, continue
```

8.5.1 USING THE DATA EEPROM

The data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). Frequently changing values will typically be updated more often than specifications D120 or D120A. If this is not the case, an array refresh must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in Flash program memory.

8.6 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the user may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- brown-out
- power glitch
- software malfunction

10.0 INSTRUCTION SET SUMMARY

The PIC16F630/676 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the PIC® Mid-Range Reference Manual (DS33023).

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the W register. If 'd' is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator, which selects the bit affected by the operation, while 'f' represents the address of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8-bit or 11-bit constant, or literal value

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 µs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note: To maintain upward compatibility with future products, do not use the **OPTION** and **TRIS** instructions.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

10.1 READ-MODIFY-WRITE OPERATIONS

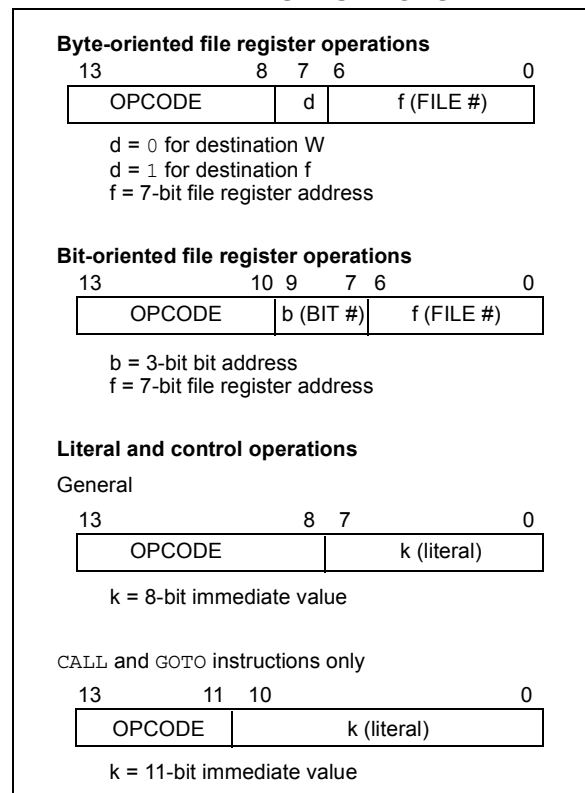
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

For example, a **CLRF PORTA** instruction will read PORTA, clear all the data bits, then write the result back to PORTA. This example would have the unintended result of clearing the condition that set the RAIF flag.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS



PIC16F630/676

TABLE 10-2: PIC16F630/676 INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRWF	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECf	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDt	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF PORTA, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- Note 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- Note 3:** If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the PIC® Mid-Range MCU Family Reference Manual (DS33023).

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CALL Call Subroutine

Syntax: `[label] CALL k`
Operands: $0 \leq k \leq 2047$
Operation: $(PC)+1 \rightarrow TOS$,
 $k \rightarrow PC<10:0>$,
 $(PCLATH<4:3>) \rightarrow PC<12:11>$
Status Affected: None
Description: Call Subroutine. First, return address $(PC + 1)$ is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits $<10:0>$. The upper bits of the PC are loaded from PCLATH. `CALL` is a two-cycle instruction.

CLRWDTClear Watchdog Timer

Syntax: `[label] CLRWDTClear Watchdog Timer`
Operands: None
Operation: $00h \rightarrow WDT$
 $0 \rightarrow WDT \text{ prescaler}$,
 $1 \rightarrow \overline{TO}$
 $1 \rightarrow \overline{PD}$
Status Affected: \overline{TO} , \overline{PD}
Description: `CLRWDTClear Watchdog Timer` instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits \overline{TO} and \overline{PD} are set.

CLRF Clear f

Syntax: `[label] CLRF f`
Operands: $0 \leq f \leq 127$
Operation: $00h \rightarrow (f)$
 $1 \rightarrow Z$
Status Affected: Z
Description: The contents of register 'f' are cleared and the Z bit is set.

COMF Complement f

Syntax: `[label] COMF f,d`
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(\bar{f}) \rightarrow (\text{destination})$
Status Affected: Z
Description: The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.

CLRWClear W

Syntax: `[label] CLRW`
Operands: None
Operation: $00h \rightarrow (W)$
 $1 \rightarrow Z$
Status Affected: Z
Description: W register is cleared. Zero bit (Z) is set.

DECF Decrement f

Syntax: `[label] DECF f,d`
Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
Operation: $(f) - 1 \rightarrow (\text{destination})$
Status Affected: Z
Description: Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

DECFSZ Decrement f, Skip if 0

Syntax: `[label] DECFSZ f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - 1 \rightarrow (\text{destination});$
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.
If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2-cycle instruction.

INCFSZ Increment f, Skip if 0

Syntax: `[label] INCFSZ f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination}),$
skip if result = 0

Status Affected: None

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.
If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2-cycle instruction.

GOTO Unconditional Branch

Syntax: `[label] GOTO k`

Operands: $0 \leq k \leq 2047$

Operation: $k \rightarrow \text{PC}<10:0>$
 $\text{PCLATH}<4:3> \rightarrow \text{PC}<12:11>$

Status Affected: None

Description: GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW Inclusive OR Literal with W

Syntax: `[label] IORLW k`

Operands: $0 \leq k \leq 255$

Operation: $(W) .OR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF Increment f

Syntax: `[label] INCF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) + 1 \rightarrow (\text{destination})$

Status Affected: Z

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

IORWF Inclusive OR W with f

Syntax: `[label] IORWF f,d`

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .OR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

12.2 DC Characteristics: PIC16F630/676-I (Industrial)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)	—	9	16	μA	2.0	Fosc = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011		—	110	150	μA	2.0	Fosc = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012		—	220	280	μA	2.0	Fosc = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013		—	70	110	μA	2.0	Fosc = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014		—	180	250	μA	2.0	Fosc = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015		—	340	450	μA	2.0	Fosc = 4 MHz INTOSC Mode
		—	500	780	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016		—	180	250	μA	2.0	Fosc = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017		—	2.1	2.95	mA	4.5	Fosc = 20 MHz
		—	2.4	3.0	mA	5.0	HS Oscillator Mode

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; MCLR = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

12.4 DC Characteristics: PIC16F630/676-E (Extended)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010E	Supply Current (IDD)	—	9	16	μA	2.0	Fosc = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011E		—	110	150	μA	2.0	Fosc = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012E		—	220	280	μA	2.0	Fosc = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013E		—	70	110	μA	2.0	Fosc = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014E		—	180	250	μA	2.0	Fosc = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015E		—	340	450	μA	2.0	Fosc = 4 MHz INTOSC Mode
		—	500	780	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016E		—	180	250	μA	2.0	Fosc = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017E		—	2.1	2.95	mA	4.5	Fosc = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all I_{DD} measurements in Active Operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD}; MCLR = V_{DD}; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

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12.5 DC Characteristics: PIC16F630/676-E (Extended)

		Standard Operating Conditions (unless otherwise stated)					
		Operating temperature		-40°C ≤ TA ≤ +125°C for extended			
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D020E	Power-down Base Current (IPD)	—	0.00099	3.5	μA	2.0	WDT, BOD, Comparators, VREF, and T1OSC disabled
		—	0.0012	4.0	μA	3.0	
		—	0.0029	8.0	μA	5.0	
D021E		—	0.3	6.0	μA	2.0	WDT Current ⁽¹⁾
		—	1.8	9.0	μA	3.0	
		—	8.4	20	μA	5.0	
D022E		—	58	70	μA	3.0	BOD Current ⁽¹⁾
		—	109	130	μA	5.0	
D023E		—	3.3	10	μA	2.0	Comparator Current ⁽¹⁾
		—	6.1	13	μA	3.0	
		—	11.5	24	μA	5.0	
D024E		—	58	70	μA	2.0	CVREF Current ⁽¹⁾
		—	85	100	μA	3.0	
		—	138	165	μA	5.0	
D025E		—	4.0	10	μA	2.0	T1 Osc Current ⁽¹⁾
		—	4.6	12	μA	3.0	
		—	6.0	20	μA	5.0	
D026E		—	0.0012	6.0	μA	3.0	A/D Current ⁽¹⁾
		—	0.0022	8.5	μA	5.0	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

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12.7 DC Characteristics: PIC16F630/676-I (Industrial), PIC16F630/676-E (Extended) (Cont.)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	Cio	All I/O pins	—	—	50*	pF	
D120	Ed	Data EEPROM Memory Byte Endurance	100K	1M	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $+85^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ Using EECON to read/write V_{MIN} = Minimum operating voltage Provided no other specifications are violated $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
D120A	Ed	Byte Endurance	10K	100K	—	E/W	
D121	VDRW	VDD for Read/Write	V_{MIN}	—	5.5	V	
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽¹⁾	1M	10M	—	E/W	
D130	EP	Program Flash Memory Cell Endurance	10K	100K	—	E/W	$-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ $+85^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ V_{MIN} = Minimum operating voltage Provided no other specifications are violated
D130A	ED	Cell Endurance	1K	10K	—	E/W	
D131	VPR	VDD for Read	V_{MIN}	—	5.5	V	
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See Section 8.5.1 for additional information.

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FIGURE 12-10: PIC16F676 A/D CONVERSION TIMING (NORMAL MODE)

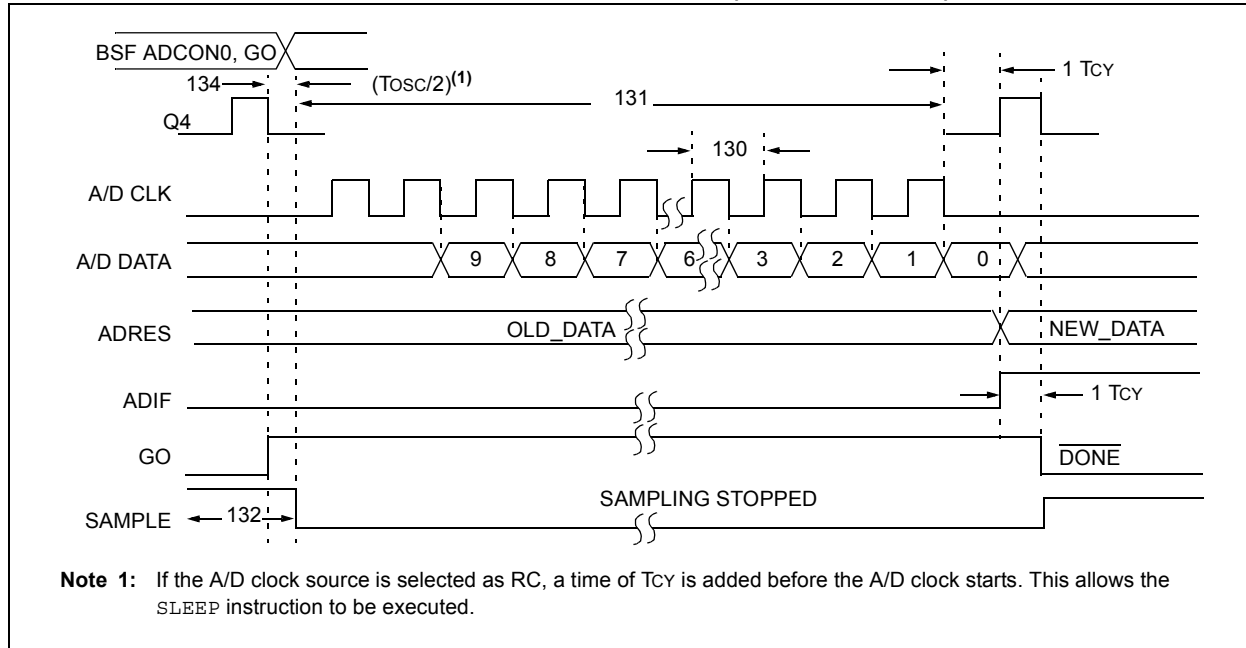


TABLE 12-9: PIC16F676 A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6	—	—	μs	TOSC based, VREF ≥ 3.0V
130	TAD	A/D Internal RC Oscillator Period	3.0*	—	—	μs	TOSC based, VREF full range
			3.0*	6.0	9.0*	μs	ADCS<1:0> = 11 (RC mode) At VDD = 2.5V
			2.0*	4.0	6.0*	μs	At VDD = 5.0V
131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	Set GO bit to new data in A/D result register
132	TACQ	Acquisition Time	(Note 2)	11.5	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
			5*	—	—	μs	
134	TGo	Q4 to A/D Clock Start	—	Tosc/2	—	—	If the A/D clock source is selected as RC, a time of T _{cy} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{cy} cycle.

Note 2: See Table 7-1 for minimum conditions.

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