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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	12
Program Memory Size	1.75KB (1K x 14)
Program Memory Type	FLASH
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-VQFN Exposed Pad
Supplier Device Package	16-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f676-i-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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NOTES:

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC16F630/676 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h-03FFh) for the PIC16F630/676 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The Reset vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).





2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose Registers and the Special Function Registers. The Special Function Registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose Registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected
- Note: The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as '0's.
- 2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC16F630/676 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4 "Indirect Addressing, INDF and FSR Registers").

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

- TMR0/WDT prescaler
- External RA2/INT interrupt
- TMR0
- Weak pull-ups on PORTA

REGISTER 2-2: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1					
	RAPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0					
	bit 7							bit 0					
bit 7	RAPU: PORTA Pull-up Enable bit 1 = PORTA pull-ups are disabled 0 = PORTA pull-ups are enabled by individual PORT latch values												
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RA2/INT pin 0 = Interrupt on falling edge of RA2/INT pin												
bit 5	TOCS: TMR0 Clock Source Select bit 1 = Transition on RA2/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)												
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA2/T0CKI pin 0 = Increment on low-to-high transition on RA2/T0CKI pin												
bit 3	PSA: Pres 1 = Presca 0 = Presca	scaler Assigi aler is assigi aler is assigi	nment bit ned to the W ned to the Ti	DT mer0 module	e								
bit 2-0	PS2:PS0:	Prescaler R	ate Select b	its									
		Bit Value 1	MR0 Rate	WDT Rate									
		000 001 010 011 100 101 110 111	1:2 1:4 1:8 1:16 1:32 1:64 1:128 1:256	1 : 1 1 : 2 1 : 4 1 : 8 1 : 16 1 : 32 1 : 64 1 : 128									
	[

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' (OPTION<3>). See Section 4.4 "Prescaler".

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- · Internal or external clock select
- · Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 4-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note:	Additional	information	on	the	Timer0					
	module is available in the PIC® Mid-Range									
	Reference Manual, (DS33023).									

4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin RA2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note:	Counter mode has specific external clock requirements. Additional information on								
	these requirements is available in the PIC®								
	Mid-Range Reference Manua								
	(DS33023).								

4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module Interrupt Service Routine before reenabling this interrupt. The Timer0 interrupt cannot wake the processor from Sleep since the timer is shut-off during Sleep.





5.4 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{T1SYNC}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.4.1).

Note: The ANSEL (91h) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC16F676.

5.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PIC[®] Mid-Range MCU Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

5.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 32 kHz. It will continue to run during Sleep. It is primarily intended for a 32 kHz crystal. Table 9-2 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up.

TRISA5 and TRISA4 bits are set when the Timer1 oscillator is enabled. RA5 and RA4 read as '0' and TRISA5 and TRISA4 bits read as '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

5.6 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine on an overflow.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Valu POR,	Value on POR, BOD		e on other sets
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	RAIE	T0IF	INTF	RAIF	0000	0000	0000	000u
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	_	_	TMR1IF	00	00	00	00
0Eh	TMR1L	Holding	g Register f	or the Least	t Significant	Byte of the	16-bit TM	R1 Registe	r	XXXX	XXXX	uuuu	uuuu
0Fh	TMR1H	Holding	g Register f	or the Most	Significant	Byte of the	16-bit TMF	R1 Register		XXXX	XXXX	uuuu	uuuu
10h	T1CON	_	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR10N	-000	0000	-uuu	uuuu
8Ch	PIE1	EEIE	ADIE	_	_	CMIE	_	_	TMR1IE	00	00	00	00

 TABLE 5-1:
 REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

6.5 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight Comparator modes. The VRCON register, Register 6-2, controls the voltage reference module shown in Figure 6-5.

6.5.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equations determine the output voltages:

$VRR = 1$ (low range): $CVREF = (VR3: VR0 / 24) \times VDD$
VRR = 0 (high range): $CVREF = (VDD / 4) + (VR3:VR0 x)$
VDD / 32)

6.5.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of VSS to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 6-5) keep CVREF from approaching VSS or VDD. The Voltage Reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in **Section 12.0 "Electrical Specifications"**.





6.6 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-7).

6.7 Operation During Sleep

Both the comparator and voltage reference, if enabled before entering Sleep mode, remain active during Sleep. This results in higher Sleep currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in Sleep mode, turn off the comparator, CM2:CM0 = 111, and voltage reference, VRCON<7> = 0. While the comparator is enabled during Sleep, an interrupt will wake-up the device. If the device wakes up from Sleep, the contents of the CMCON and VRCON registers are not affected.

6.8 Effects of a Reset

A device Reset forces the CMCON and VRCON registers to their Reset states. This forces the comparator module to be in the Comparator Reset mode, CM2:CM0 = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.

REGISTER 7-3:	ANSEL—ANALOG SELECT REGISTER (ADRESS: 91h) (PIC16F676 ONLY)
---------------	---

| R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ANS7 | ANS6 | ANS5 | ANS4 | ANS3 | ANS2 | ANS1 | ANS0 |
| bit 7 | | | | | | | bit 0 |

bit 7-0: **ANS<7:0>**: Analog Select between analog or digital function on pins AN<7:0>, respectively. 1 = Analog input. Pin is assigned as analog input.⁽¹⁾

0 = Digital I/O. Pin is assigned to port or special function.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change if available. The corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.0 SPECIAL FEATURES OF THE CPU

Certain special circuits that deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC16F630/676 family has a host of such features intended to:

- maximize system reliability
- minimize cost through elimination of external components
- provide power-saving operating modes and offer code protection

These features are:

- · Oscillator selection
- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- Sleep
- Code protection
- · ID Locations
- In-Circuit Serial Programming[™]

The PIC16F630/676 has a Watchdog Timer that is controlled by Configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in Reset while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can provide at least a 72 ms Reset. With these three functions on-chip, most applications need no external Reset circuitry.

The Sleep mode is designed to offer a very low current Power-down mode. The user can wake-up from Sleep through:

- · External Reset
- · Watchdog Timer wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options (see Register 9-1).

9.1 Configuration Bits

The Configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations, as shown in Register 9-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h-3FFFh), which can be accessed only during programming. See PIC16F630/676 Programming Specification for more information.

REGISTER 9-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1		
BG1	BG0			_	CPD	CP	BODEN	MCLRE	PWRTE	WDTE	F0SC2	F0SC1	F0SC0		
bit 13							-		· · · ·				bit 0		
bit 13-'	 BG1:BG0: Bandgap Calibration bits for BOD and POR voltage⁽¹⁾ 00 = Lowest bandgap voltage 11 = Highest bandgap voltage 														
bit 11-9) <u>U</u>	Unimplemented: Read as '0'													
bit 8	1 0	CPD : Data Code Protection bit ⁽²⁾ 1 = Data memory code protection is disabled 0 = Data memory code protection is enabled													
bit 7	1 0	CP : Code Protection bit ⁽³⁾ 1 = Program Memory code protection is disabled 0 = Program Memory code protection is enabled													
bit 6	B 1 0	BODEN: Brown-out Detect Enable bit ⁽⁴⁾ 1 = BOD enabled 0 = BOD disabled													
bit 5	1 0	MCLRE: RA3/MCLR pin function select bit ⁽⁵⁾ 1 = RA3/MCLR pin function is MCLR 0 = RA3/MCLR pin function is digital I/O, MCLR internally tied to VDD													
bit 4	P 1 0	WRTE : = PWR = PWR	Power-up T disabled T enabled	Timer E J	nable bit	:									
bit 3	N 1 0	/DTE : W = WDT = WDT	Vatchdog 7 enabled disabled	ſimer En	able bit										
bit 2-0	F 1 1 1 1 0 0 0 0 0	0 = WD1 disabled FOSC2:FOSC0 : Oscillator Selection bits 111 = RC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN 110 = RC oscillator: I/O function on RA4/OSC2/CLKOUT pin, RC on RA5/OSC1/CLKIN 101 = INTOSC oscillator: CLKOUT function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN 100 = INTOSC oscillator: I/O function on RA4/OSC2/CLKOUT pin, I/O function on RA5/OSC1/CLKIN 101 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN 011 = EC: I/O function on RA4/OSC2/CLKOUT pin, CLKIN on RA5/OSC1/CLKIN 010 = HS oscillator: High speed crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN 001 = XT oscillator: Crystal/resonator on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN 000 = LP oscillator: Low power crystal on RA4/OSC2/CLKOUT and RA5/OSC1/CLKIN													
	N	 Note 1: The Bandgap Calibration bits are factory programmed and must be read and saved prior to erasing the device as specified in the PIC16F630/676 Programming Specification. These bits are reflected in an export of the Configuration Word. Microchip Development Tools maintain all calibration bits to factory settings. 2: The entire data EEPROM will be erased when the code protection is turned off. 3: The entire program memory will be erased, including OSCCAL value, when the code protection is turned off. 4: Enabling Brown-out Detect does not automatically enable Power-up Timer. 5: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled 													
		egend:	rammed i												
	- F	₹ = Rea	dable bit	Sing ioc	v v	v = Writa	uble bit	U =	Unimpler	nented b	oit. read a	as '0'			
	-	n = Valu	le at POR		1	= bit is s	set	0 = 1	bit is clea	red	x = bi	t is unkn	lown		

TADLE 3-7.				
Register	Address	Power-on Reset	 MCLR Reset WDT Reset Brown-out Detect⁽¹⁾ 	 Wake-up from Sleep through interrupt Wake-up from Sleep through WDT time-out
W	—	XXXX XXXX	นนนน นนนน	นนนน นนนน
INDF	00h/80h	—	—	—
TMR0	01h	XXXX XXXX	นนนน นนนน	นนนน นนนน
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	XXXX XXXX	นนนน นนนน	uuuu uuuu
PORTA	05h	xx xxxx	uu uuuu	uu uuuu
PORTC	07h	xx xxxx	uu uuuu	uu uuuu
PCLATH	0Ah/8Ah	0 0000	0 0000	u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 000u	uuuu uuqq ⁽²⁾
PIR1	0Ch	00 00	00 00	qq qq ^(2,5)
T1CON	10h	-000 0000	-uuu uuuu	-uuu uuuu
CMCON	19h	-0-0 0000	-0-0 0000	-u-u uuuu
ADRESH	1Eh	XXXX XXXX	นนนน นนนน	นนนน นนนน
ADCON0	1Fh	00-0 0000	00-0 0000	นน-น นนนน
OPTION_REG	81h	1111 1111	1111 1111	นนนน นนนน
TRISA	85h	11 1111	11 1111	uu uuuu
TRISC	87h	11 1111	11 1111	uu uuuu
PIE1	8Ch	00 00	00 00	uu uu
PCON	8Eh	0x	(1,6)	uu
OSCCAL	90h	1000 00	1000 00	uuuu uu
ANSEL	91h	1111 1111	1111 1111	นนนน นนนน
WPUA	95h	11 -111	11 -111	uuuu uuuu
IOCA	96h	00 0000	00 0000	uu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDATA	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	-000 0000	-000 0000	-นนน นนนน
EECON1	9Ch	x000	q000	uuuu
EECON2	9Dh			
ADRESL	9Eh	XXXX XXXX	นนนน นนนน	นนนน นนนน
ADCON1	9Fh	-000	-000	-uuu

TABLE 9-7: INITIALIZATION CONDITION FOR REGISTERS

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

- Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.
 2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
 - **3:** When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
 - 4: See Table 9-6 for Reset value for specific condition.
 - 5: If wake-up was due to data EEPROM write completing, bit 7 = 1; A/D conversion completing, bit 6 = 1; Comparator input changing, bit 3 = 1; or Timer1 rolling over, bit 0 = 1. All other interrupts generating a wake-up will cause these bits to = u.
 - **6:** If Reset was due to brown-out, then bit 0 = 0. All other Resets will cause bit 0 = u.

FIGURE 9-10: INTERRUPT LOGIC





Note 1: T0SE, T0CS, PSA, PS0-PS2 are bits in the OPTION register.

TABLE 9-9: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other Resets
81h	OPTION_REG	RAPU	INTEDG	TOCS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
2007h	Config. bits	CP	BODEN	MCLRE	PWRTE	WDTE	F0SC2	F0SC1	F0SC0	uuuu uuuu	uuuu uuuu

Legend: u = Unchanged, shaded cells are not used by the Watchdog Timer.

SWAPF	Swap Nibbles in f
Syntax:	[<i>label</i>] SWAPF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	$(f<3:0>) \rightarrow (destination<7:4>),$ $(f<7:4>) \rightarrow (destination<3:0>)$
Status Affected:	None
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.

XORWF	Exclusive OR W with f
Syntax:	[<i>label</i>] XORWF f,d
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$
Operation:	(W) .XOR. (f) \rightarrow (destination)
Status Affected:	Z
Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

XORLW	Exclusive OR Literal with W
Syntax:	[<i>label</i>] XORLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .XOR. $k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

11.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit[™] 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit[™] 2 enables in-circuit debugging on most PIC[®] microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

11.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

11.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM[™] and dsPICDEM[™] demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ[®] security ICs, CAN, IrDA[®], PowerSmart battery management, SEEVAL[®] evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.











FIGURE 13-10: TYPICAL IPD WITH A/D ENABLED vs. VDD OVER TEMP (+85°C)



14.2 Package Details

The following sections give the technical details of the packages.

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES	
Dimensio	on Limits	MIN	NOM	MAX
Number of Pins	Ν		14	
Pitch	е		.100 BSC	
Top to Seating Plane	Α	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	Е	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	С	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	_	_	.430

Notes:

- 1. Pin 1 visual index feature may vary, but must be located with the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	x <u>xx xxx</u>	Examples:
Device 1	emperature Package Pattern Range	 a) PIC16F630 - E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301 b) PIC16F676 - I/SL = Industrial Temp., SOIC
Device:	: Standard VDD range T: (Tape and Reel)	package, 20 MHz
Temperature Range:	$I = -40^{\circ}C \text{ to } +85^{\circ}C$ $E = -40^{\circ}C \text{ to } +125^{\circ}C$	
Package:	P = PDIP SL = SOIC (Gull wing, 3.90 mm body) ST = TSSOP(4.4 mm)	
Pattern:	3-Digit Pattern Code for QTP (blank otherwise)	

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.