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Details

Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VFQFN Exposed Pad
Supplier Device Package	44-VQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atmega644p-20mq

32-pin TQFP/ QFN/ MLF Pin #	40-pin PDIP Pin #	PAD	EXTINT	PCINT	ADC/AC	OSC	T/C # 0	T/C # 1	USART	I2C	SPI	JTAG
35	38	PA[2]		PCINT2	ADC2							
36	39	PA[1]		PCINT1	ADC1							
37	40	PA[0]		PCINT0	ADC0							
38	-	VCC								SDA1		
39	-	GND								SCL1		
40	1	PB[0]		PCINT8			T0		XCK0			
41	2	PB[1]		PCINT9		CLKO		T1				
42	3	PB[2]	INT2	PCINT10	AIN0							
43	4	PB[3]		PCINT11	AIN1		OC0A					
44	5	PB[4]		PCINT12			OC0B				SS	
-	-	GND										
-	-	GND										
-	-	GND										
-	-	GND										
-	-	GND										

Table 10-8. Capacitance for Low-Frequency Oscillator

32kHz Osc. Type	Cap. (XTAL1/TOSC1)	Cap. (XTAL2/TSOC2)
System Osc.	18pF	8pF
Timer Osc.	6pF	6pF

The capacitance (Ce+Ci) needed at each TOSC pin can be calculated by using:

$$C = 2CL - C_s$$

where:

- Ce - is optional external capacitors as described in [Figure 10-2](#).
- Ci - is the pin capacitance in the above table.
- CL - is the load capacitance for a 32.768kHz crystal specified by the crystal vendor.
- Cs - is the total stray capacitance for one TOSC pin.

Crystals specifying a load capacitance (CL) higher than 6pF require external capacitors applied as described in [Low Power Crystal Oscillator](#).

When this oscillator is selected, start-up times are determined by the SUT Fuses and CKSEL0 as shown in the following table.

Table 10-9. Start-up Times for the Low Frequency Crystal Oscillator Clock Selection

Power Conditions	Start-up Time from Power-down and Power-save	Additional Delay from Reset (V _{CC} = 5.0V)	CKSEL[0]	SUT[1:0]
BOD enabled	1K CK	14CK ⁽¹⁾	0	00
Fast rising power	1K CK	14CK + 4.1 ms ⁽¹⁾	0	01
Slowly rising power	1K CK	14CK + 65 ms ⁽¹⁾	0	10
Reserved			0	11
BOD enabled	32K CK	14CK	1	00
Fast rising power	32K CK	14CK + 4.1 ms	1	01
Slowly rising power	32K CK	14CK + 65 ms	1	10
Reserved			1	11

Note:

1. This option should only be used if frequency stability at start-up is not important for the application.

Related Links

[Clock Source Connections](#) on page 45

[Timer/Counter Oscillator](#) on page 52

10.6. Calibrated Internal RC Oscillator

By default, the Internal RC Oscillator provides an 8.0MHz clock. Though voltage and temperature dependent, this clock can be very accurately calibrated by the user. The device is shipped with the CKDIV8 Fuse programmed.

Note:

1. The 128kHz oscillator is a very low power clock source, and is not designed for high accuracy.

When this clock source is selected, start-up times are determined by the SUT Fuses:

Table 10-13. Start-Up Times for the 128kHz Internal Oscillator

Power Conditions	Start-Up Time from Power-down and Power-save	Additional Delay from Reset	SUT[1:0]
BOD enabled	6 CK	14CK	00
Fast rising power	6 CK	14CK + 4ms	01
Slowly rising power	6 CK	14CK + 64ms	10
Reserved			11

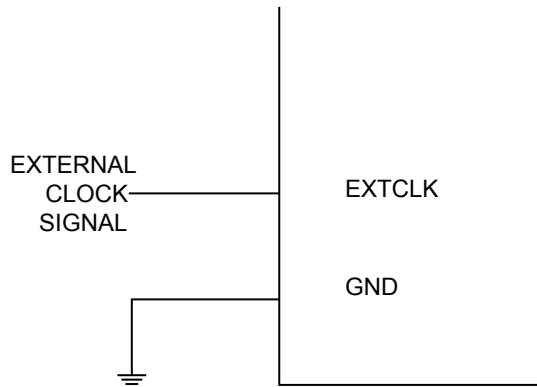
10.8. External Clock

To drive the device from an external clock source, EXTCLK should be driven as shown in the Figure below. To run the device on an external clock, the CKSEL Fuses must be programmed to '0000':

Table 10-14. External Clock Frequency

Frequency	CKSEL[3:0]
0 - 20MHz	0000

Figure 10-3. External Clock Drive Configuration



When this clock source is selected, start-up times are determined by the SUT Fuses:

Table 10-15. Start-Up Times for the External Clock Selection - SUT

Power Conditions	Start-Up Time from Power-down and Power-save	Additional Delay from Reset ($V_{CC} = 5.0V$)	SUT[1:0]
BOD enabled	6 CK	14CK	00
Fast rising power	6 CK	14CK + 4.1ms	01
Slowly rising power	6 CK	14CK + 65ms	10
Reserved			11

14.1.2.3. External Interrupt Flag Register

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

The device is a complex microcontroller with more peripheral units than can be supported within the 64 locations reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Name: EIFR

Offset: 0x3C

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x1C

Bit	7	6	5	4	3	2	1	0
						INTF2	INTF1	INTF0
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – INTF2: External Interrupt Flag 2

When an edge or logic change on the INT2 pin triggers an interrupt request, INTF2 will be set. If the I-bit in SREG and the INT2 bit in EIMSK are set, the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing '1' to it. This flag is always cleared when INT2 is configured as a level interrupt.

Bit 1 – INTF1: External Interrupt Flag 1

When an edge or logic change on the INT1 pin triggers an interrupt request, INTF1 will be set. If the I-bit in SREG and the INT1 bit in EIMSK are set, the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing '1' to it. This flag is always cleared when INT1 is configured as a level interrupt.

Bit 0 – INTF0: External Interrupt Flag 0

When an edge or logic change on the INT0 pin triggers an interrupt request, INTF0 will be set. If the I-bit in SREG and the INT0 bit in EIMSK are set, the MCU will jump to the corresponding Interrupt Vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing '1' to it. This flag is always cleared when INT0 is configured as a level interrupt.

15.4.12. Port D Data Direction Register

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

The device is a complex microcontroller with more peripheral units than can be supported within the 64 locations reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Name: DDRD

Offset: 0x2A

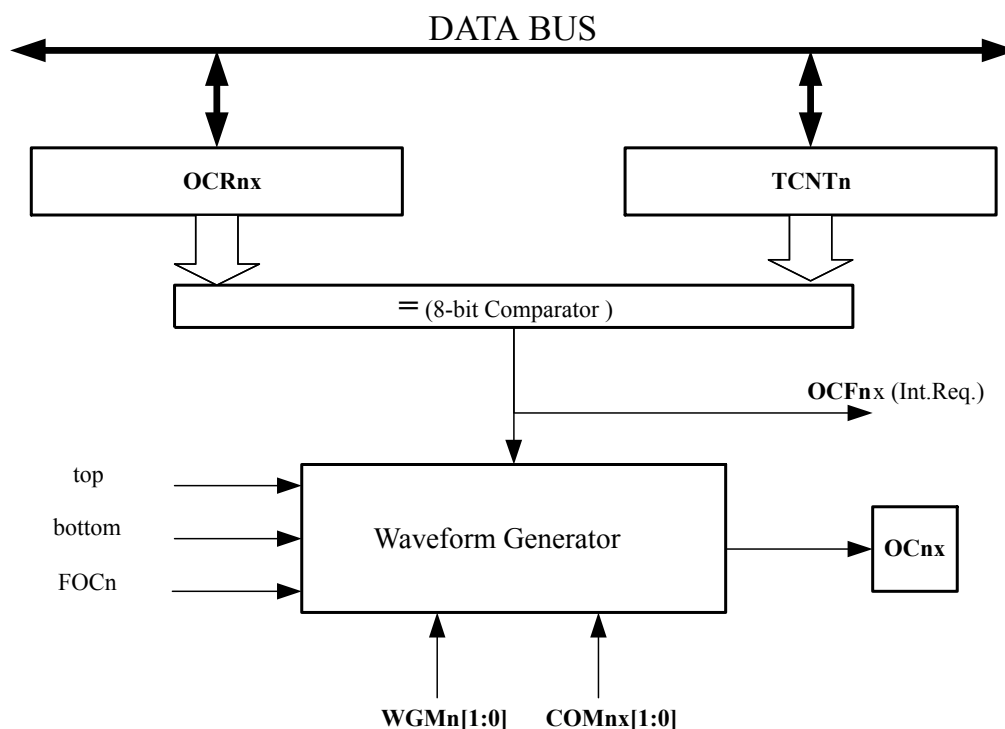
Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x0A

Bit	7	6	5	4	3	2	1	0
	DDRD7	DDRD6	DDRD5	DDRD4	DDRD3	DDRD2	DDRD1	DDRD0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – DDRDn: Port D Data Direction [n = 7:0]

Figure 16-3. Output Compare Unit, Block Diagram



Note: The “n” in the register and bit names indicates the device number (n = 0 for Timer/Counter 0), and the “x” indicates Output Compare unit (A/B).

The OCR0x Registers are double buffered when using any of the Pulse Width Modulation (PWM) modes. When double buffering is enabled, the CPU has access to the OCR0x Buffer Register. The double buffering synchronizes the update of the OCR0x Compare Registers to either top or bottom of the counting sequence. The synchronization prevents the occurrence of odd-length, non-symmetrical PWM pulses, thereby making the output glitch-free.

The double buffering is disabled for the normal and Clear Timer on Compare (CTC) modes of operation, and the CPU will access the OCR0x directly.

16.5.1. Force Output Compare

In non-PWM waveform generation modes, the match output of the comparator can be forced by writing a '1' to the Force Output Compare (TCCR0C.FOC0x) bit. Forcing compare match will not set the OCF0x Flag or reload/clear the timer, but the OC0x pin will be updated as if a real compare match had occurred (the TCCR0A.COM0x[1:0] bits define whether the OC0x pin is set, cleared or toggled).

16.5.2. Compare Match Blocking by TCNT0 Write

All CPU write operations to the TCNT0 Register will block any compare match that occur in the next timer clock cycle, even when the timer is stopped. This feature allows OCR0x to be initialized to the same value as TCNT0 without triggering an interrupt when the Timer/Counter clock is enabled.

16.5.3. Using the Output Compare Unit

Since writing TCNT0 in any mode of operation will block all compare matches for one timer clock cycle, there are risks involved when changing TCNT0 when using the Output Compare Unit, independently of whether the Timer/Counter is running or not. If the value written to TCNT0 equals the OCR0x value, the compare match will be missed, resulting in incorrect waveform generation. Similarly, do not write the TCNT0 value equal to BOTTOM when the counter is down counting.

16.9.7. TC0 Output Compare Register B

When addressing I/O Registers as data space using LD and ST instructions, the provided offset must be used. When using the I/O specific commands IN and OUT, the offset is reduced by 0x20, resulting in an I/O address offset within 0x00 - 0x3F.

The device is a complex microcontroller with more peripheral units than can be supported within the 64 locations reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Name: OCR0B

Offset: 0x48

Reset: 0x00

Property: When addressing as I/O Register: address offset is 0x28

Bit	7	6	5	4	3	2	1	0
	OCR0B[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR0B[7:0]: Output Compare 0 B

The Output Compare Register B contains an 8-bit value that is continuously compared with the counter value (TCNT0). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC0B pin.

Table 17-1. Definitions

Constant	Description
BOTTOM	The counter reaches the BOTTOM when it becomes zero (0x00 for 8-bit counters, or 0x0000 for 16-bit counters).
MAX	The counter reaches its Maximum when it becomes 0xFF (decimal 255, for 8-bit counters) or 0xFFFF (decimal 65535, for 16-bit counters).
TOP	The counter reaches the TOP when it becomes equal to the highest value in the count sequence. The TOP value can be assigned to be the fixed value MAX or the value stored in the OCR1A Register. The assignment is dependent on the mode of operation.

17.5. Registers

The Timer/Counter (TCNT1), Output Compare Registers (OCRA/B), and Input Capture Register (ICR1) are all 16-bit registers. Special procedures must be followed when accessing the 16-bit registers. These procedures are described in section [Accessing 16-bit Registers](#).

The Timer/Counter Control Registers (TCCR1A/B/C) are 8-bit registers and have no CPU access restrictions. Interrupt requests (abbreviated to Int.Req. in the block diagram) signals are all visible in the Timer Interrupt Flag Register (TIFR1). All interrupts are individually masked with the Timer Interrupt Mask Register (TIMSK1). TIFR1 and TIMSK1 are not shown in the figure.

The Timer/Counter can be clocked internally, via the prescaler, or by an external clock source on the T1 pin. The Clock Select logic block controls which clock source and edge the Timer/Counter uses to increment (or decrement) its value. The Timer/Counter is inactive when no clock source is selected. The output from the Clock Select logic is referred to as the timer clock (clk_{T1}).

The double buffered Output Compare Registers (OCR1A/B) are compared with the Timer/Counter value at all time. The result of the compare can be used by the Waveform Generator to generate a PWM or variable frequency output on the Output Compare pin (OC1A/B). See [Output Compare Units](#). The compare match event will also set the Compare Match Flag (OCF1A/B) which can be used to generate an Output Compare interrupt request.

The Input Capture Register can capture the Timer/Counter value at a given external (edge triggered) event on either the Input Capture pin (ICP1) or on the Analog Comparator pins. The Input Capture unit includes a digital filtering unit (Noise Canceler) for reducing the chance of capturing noise spikes.

The TOP value, or maximum Timer/Counter value, can in some modes of operation be defined by either the OCR1A Register, the ICR1 Register, or by a set of fixed values. When using OCR1A as TOP value in a PWM mode, the OCR1A Register can not be used for generating a PWM output. However, the TOP value will in this case be double buffered allowing the TOP value to be changed in run time. If a fixed TOP value is required, the ICR1 Register can be used as an alternative, freeing the OCR1A to be used as PWM output.

17.6. Accessing 16-bit Registers

The TCNT1, OCR1A/B, and ICR1 are 16-bit registers that can be accessed by the AVR CPU via the 8-bit data bus. The 16-bit register must be accessed byte-wise, using two read or write operations. Each 16-bit timer has a single 8-bit TEMP register for temporary storing of the high byte of the 16-bit access. The same temporary register is shared between all 16-bit registers within each 16-bit timer.

19.11.5. TC2 Output Compare Register B

Name: OCR2B
Offset: 0xB4
Reset: 0x00
Property: -

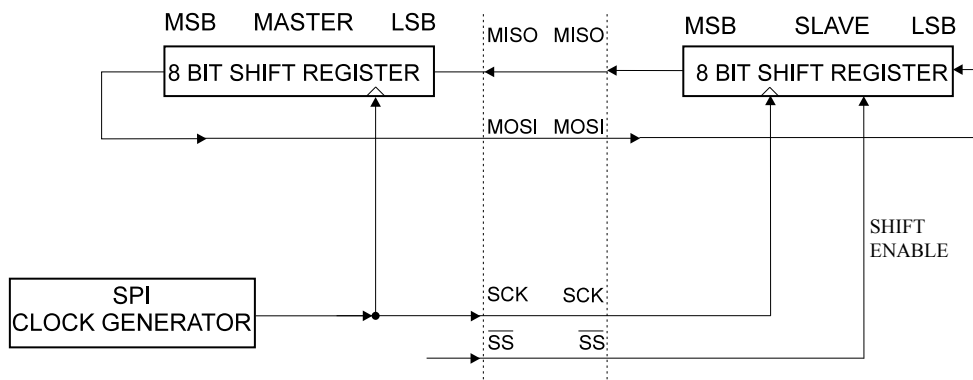
Bit	7	6	5	4	3	2	1	0
	OCR2B[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OCR2B[7:0]: Output Compare 2 B

The Output Compare Register B contains an 8-bit value that is continuously compared with the counter value (TCNT2). A match can be used to generate an Output Compare interrupt, or to generate a waveform output on the OC2B pin.

data to be sent into SPDR before reading the incoming data. The last incoming byte will be kept in the Buffer Register for later use.

Figure 20-2. SPI Master-slave Interconnection



The system is single buffered in the transmit direction and double buffered in the receive direction. This means that bytes to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received character must be read from the SPI Data Register before the next character has been completely shifted in. Otherwise, the first byte is lost.

In SPI Slave mode, the control logic will sample the incoming signal of the SCK pin. To ensure correct sampling of the clock signal, the minimum low and high periods should be longer than two CPU clock cycles.

When the SPI is enabled, the data direction of the MOSI, MISO, SCK, and \overline{SS} pins is overridden according to the table below. For more details on automatic port overrides, refer to the IO Port description.

Table 20-1. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
\overline{SS}	User Defined	Input

Note: 1. See the IO Port description for how to define the SPI pin directions.

The following code examples show how to initialize the SPI as a Master and how to perform a simple transmission. `DDR_SPI` in the examples must be replaced by the actual Data Direction Register controlling the SPI pins. `DD_MOSI`, `DD_MISO` and `DD_SCK` must be replaced by the actual data direction bits for these pins. E.g. if MOSI is placed on pin PB5, replace `DD_MOSI` with `DDB5` and `DDR_SPI` with `DDRB`.

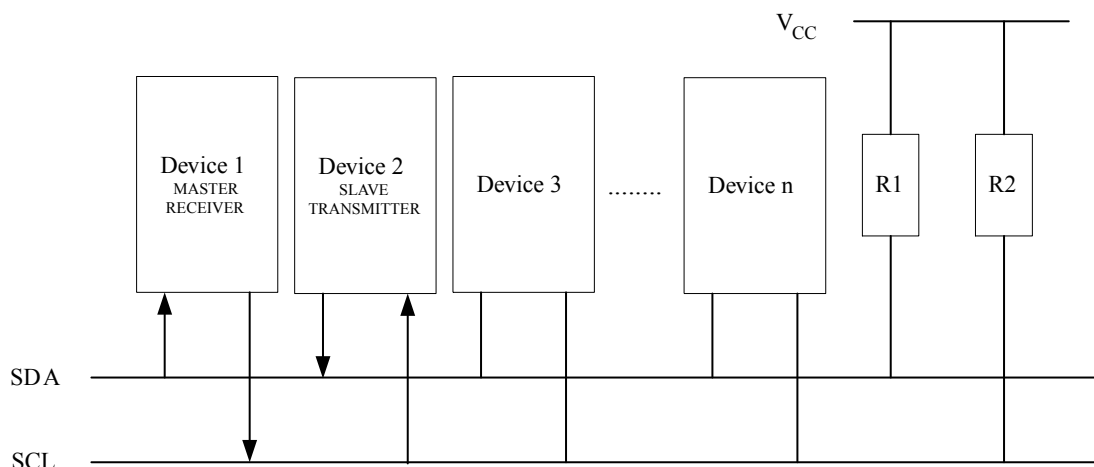
Assembly Code Example

```

SPI_MasterInit:
; Set MOSI and SCK output, all others input
ldi    r17, (1<<DD_MOSI) | (1<<DD_SCK)
out    DDR_SPI, r17
; Enable SPI, Master, set clock rate fck/16
ldi    r17, (1<<SPE) | (1<<MSTR) | (1<<SPR0)
out    SPCR, r17
ret

```

Figure 23-13. Data Transfer in Master Receiver Mode



A START condition is sent by writing to the TWI Control register (TWCRn) a value of the type TWCRn=1x10x10x:

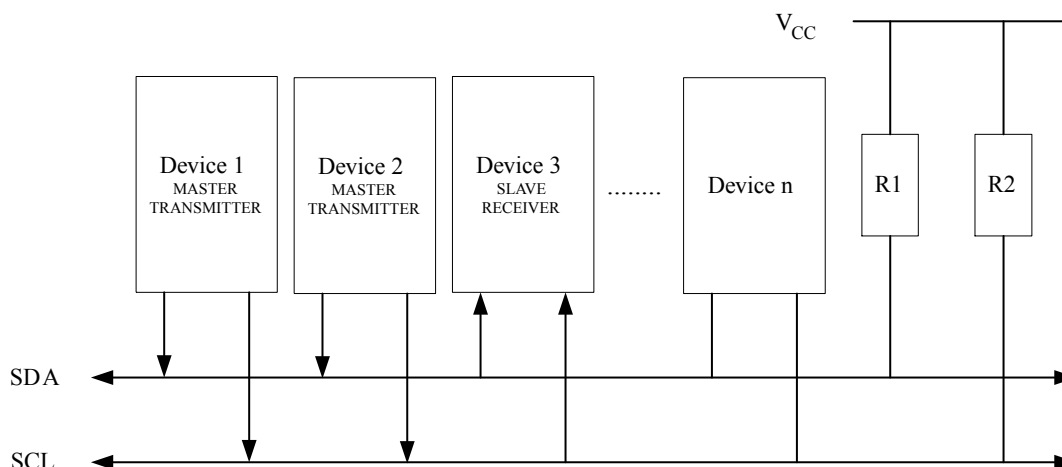
- TWCRn.TWEN must be written to '1' to enable the 2-wire Serial Interface
- TWCRn.TWSTA must be written to '1' to transmit a START condition
- TWCRn.TWINT must be cleared by writing a '1' to it.

The TWI will then test the 2-wire Serial Bus and generate a START condition as soon as the bus becomes free. After a START condition has been transmitted, the TWINT Flag is set by hardware, and the status code in TWSRn will be 0x08 (see Status Code table below). In order to enter MR mode, SLA+R must be transmitted. This is done by writing SLA+R to TWDR. Thereafter, the TWINT flag should be cleared (by writing '1' to it) to continue the transfer. This is accomplished by writing the a value to TWCRn of the type TWCRn=1x00x10x.

When SLA+R have been transmitted and an acknowledgment bit has been received, TWINT is set again and a number of status codes in TWSRn are possible. Possible status codes in Master mode are 0x38, 0x40, or 0x48. The appropriate action to be taken for each of these status codes is detailed in the table below. Received data can be read from the TWDR Register when the TWINT Flag is set high by hardware. This scheme is repeated until the last byte has been received. After the last byte has been received, the MR should inform the ST by sending a NACK after the last received data byte. The transfer is ended by generating a STOP condition or a repeated START condition. A repeated START condition is sent by writing to the TWI Control register (TWCRn) a value of the type TWCRn=1x10x10x again. A STOP condition is generated by writing TWCRn=1x01x10x:

After a repeated START condition (status code 0x10) the 2-wire Serial Interface can access the same Slave again, or a new Slave without transmitting a STOP condition. Repeated START enables the Master to switch between Slaves, Master Transmitter mode and Master Receiver mode without losing control over the bus.

Figure 23-20. An Arbitration Example

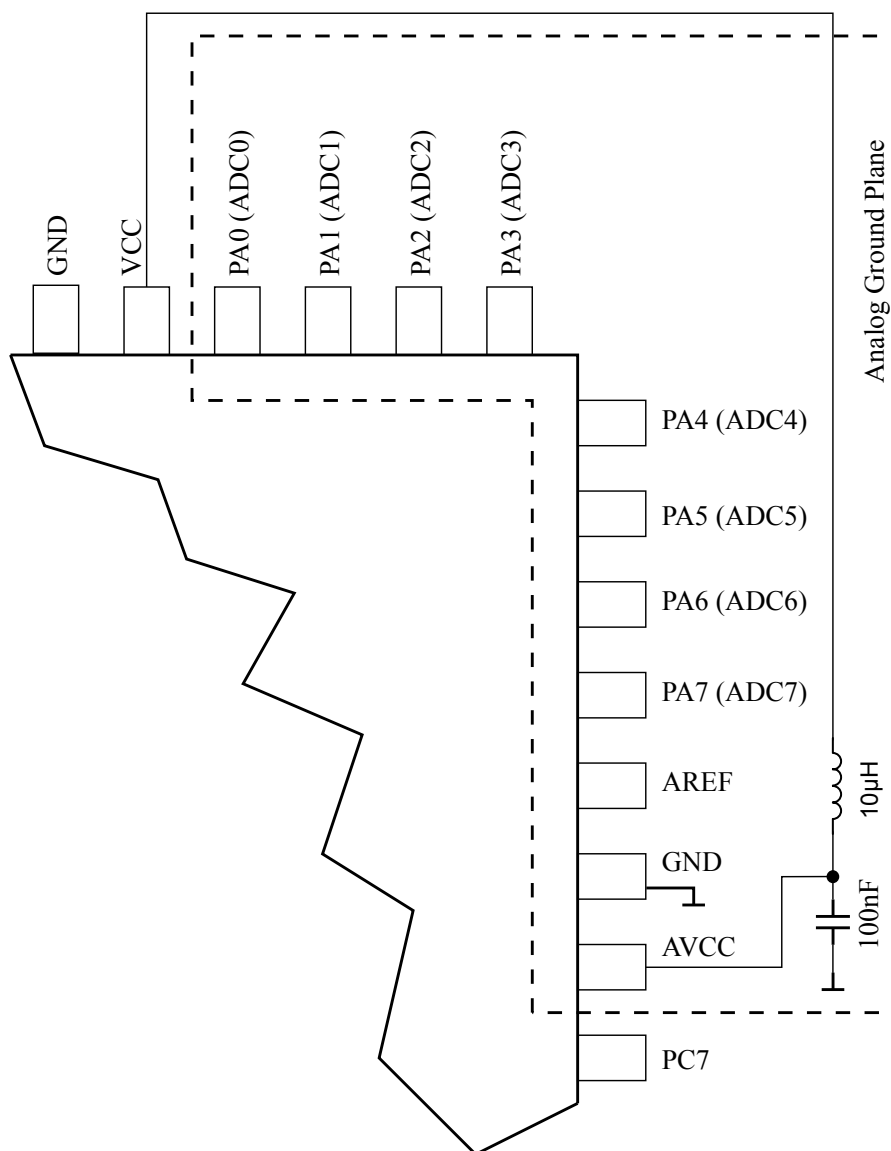


Several different scenarios may arise during arbitration, as described below:

- Two or more masters are performing identical communication with the same Slave. In this case, neither the Slave nor any of the masters will know about the bus contention.
- Two or more masters are accessing the same Slave with different data or direction bit. In this case, arbitration will occur, either in the READ/WRITE bit or in the data bits. The masters trying to output a '1' on SDA while another Master outputs a zero will lose the arbitration. Losing masters will switch to not addressed Slave mode or wait until the bus is free and transmit a new START condition, depending on application software action.
- Two or more masters are accessing different slaves. In this case, arbitration will occur in the SLA bits. Masters trying to output a '1' on SDA while another Master outputs a zero will lose the arbitration. Masters losing arbitration in SLA will switch to Slave mode to check if they are being addressed by the winning Master. If addressed, they will switch to SR or ST mode, depending on the value of the READ/WRITE bit. If they are not being addressed, they will switch to not addressed Slave mode or wait until the bus is free and transmit a new START condition, depending on application software action.

This is summarized in the next figure. Possible status values are given in circles.

Figure 25-9. ADC Power Connections



25.6.3. Offset Compensation Schemes

The gain stage has a built-in offset cancellation circuitry that nulls the offset of differential measurements as much as possible. The remaining offset in the analog path can be measured directly by selecting the same channel for both differential inputs. This offset residue can be then subtracted in software from the measurement results. Using this kind of software based offset correction, offset on any channel can be reduced below one LSB.

25.6.4. ADC Accuracy Definitions

An n-bit single-ended ADC converts a voltage linearly between GND and V_{REF} in 2^n steps (LSBs). The lowest code is read as 0, and the highest code is read as $2^n - 1$.

Several parameters describe the deviation from the ideal behavior:

- Offset: The deviation of the first transition (0x000 to 0x001) compared to the ideal transition (at 0.5 LSB). Ideal value: 0 LSB.

25.8.2. ADC Control and Status Register A

Name: ADCSRA

Offset: 0x7A

Reset: 0x00

Property: -

Bit	7	6	5	4	3	2	1	0
	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – ADEN: ADC Enable

Writing this bit to one enables the ADC. By writing it to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress, will terminate this conversion.

Bit 6 – ADSC: ADC Start Conversion

In Single Conversion mode, write this bit to one to start each conversion. In Free Running mode, write this bit to one to start the first conversion. The first conversion after ADSC has been written after the ADC has been enabled, or if ADSC is written at the same time as the ADC is enabled, will take 25 ADC clock cycles instead of the normal 13. This first conversion performs initialization of the ADC.

ADSC will read as one as long as a conversion is in progress. When the conversion is complete, it returns to zero. Writing zero to this bit has no effect.

Bit 5 – ADATE: ADC Auto Trigger Enable

When this bit is written to one, Auto Triggering of the ADC is enabled. The ADC will start a conversion on a positive edge of the selected trigger signal. The trigger source is selected by setting the ADC Trigger Select bits, ADTS in ADCSRB.

Bit 4 – ADIF: ADC Interrupt Flag

This bit is set when an ADC conversion completes and the Data Registers are updated. The ADC Conversion Complete Interrupt is executed if the ADIE bit and the I-bit in SREG are set. ADIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ADIF is cleared by writing a logical one to the flag. Beware that if doing a Read-Modify-Write on ADCSRA, a pending interrupt can be disabled. This also applies if the SBI and CBI instructions are used.

Bit 3 – ADIE: ADC Interrupt Enable

When this bit is written to one and the I-bit in SREG is set, the ADC Conversion Complete Interrupt is activated.

Bits 2:0 – ADPSn: ADC Prescaler Select [n = 2:0]

These bits determine the division factor between the system clock frequency and the input clock to the ADC.

Table 25-5. Input Channel Selection

ADPS[2:0]	Division Factor
000	2
001	2

26.14. ATmega644P Boundary-scan Order

The table below shows the Scan order between TDI and TDO when the Boundary-scan Chain is selected as data path. Bit 0 is the LSB; the first bit scanned in, and the first bit scanned out. The scan order follows the pin-out order as far as possible. Therefore, the bits of Port A are scanned in the opposite bit order of the other ports.

Exceptions from the rules are the scan chains for the analog circuits, which constitute the most significant bits of the scan chain regardless of which physical pin they are connected to. In [Figure 26-5](#), PXn. Data corresponds to FF0, PXn. Control corresponds to FF1, and PXn. Pullup_enable corresponds to FF2. Bit 2, 3, 4, and 5 of Port C is not in the scan chain, since these pins constitute the TAP pins when the JTAG is enabled.

Table 26-3. ATmega644P Boundary-scan Order (TBD)

Bit Number	Signal Name	Module
56	PB0.Data	Port B
55	PB0.Control	
54	PB1.Data	
53	PB1.Control	
52	PB2.Data	
51	PB2.Control	
50	PB3.Data	
49	PB3.Control	
48	PB4.Data	
47	PB4.Control	
46	PB5.Data	
45	PB5.Control	
44	PB6.Data	
43	PB6.Control	
42	PB7.Data	
41	PB7.Control	
40	RSTT	Reset Logic (Observe Only)


```
ret
```

27.8.14. ATmega644P Boot Loader Parameters

In the following tables, the parameters used in the description of the self programming are given.

Table 27-7. Boot Size Configuration, ATmega644P

BOOTSZ1	BOOTSZ0	Boot Size	Pages	Application Flash Section	Boot Loader Flash Section	End Application Section	Boot Reset Address (Start Boot Loader Section)
1	1	512 words	4	0x0000 - 0x7DFF	0x7E00 - 0x7FFF	0x7DFF	0x7E00
1	0	1024 words	8	0x0000 - 0x7BFF	0x7C00 - 0x7FFF	0x7BFF	0x7C00
0	1	2048 words	16	0x0000 - 0x77FF	0x7800 - 0x7FFF	0x77FF	0x7800
0	0	4096 words	32	0x0000 - 0x7FFF	0x7000 - 0x3FFF	0x6FFF	0x7000

Note: The different BOOTSZ Fuse configurations are shown in [Figure 27-2](#)

Table 27-8. Read-While-Write Limit, ATmega644P

Section	Pages	Address
Read-While-Write section (RWW)	224	0x0000 - 0x6FFF
No Read-While-Write section (NRWW)	32	0x7000 - 0x7FFF

Note: For details about these two section, see [NRWW – No Read-While-Write Section](#) and [RWW – Read-While-Write Section](#).

Table 27-9. Explanation of Different Variables used in Figure and the Mapping to the Z-pointer, ATmega644P

Variable		Corresponding Variable ⁽¹⁾	Description
PCMSB	14		Most significant bit in the Program Counter. (The Program Counter is 15 bits PC[14:0])
PAGEMSB	6		Most significant bit which is used to address the words within one page (128 words in a page requires 7 bits PC [6:0]).
ZPCMSB		Z15	Bit in Z-register that is mapped to PCMSB. Because Z0 is not used, the ZPCMSB equals PCMSB + 1.
ZPAGEMSB		Z7	Bit in Z-register that is mapped to PAGEMSB. Because Z0 is not used, the ZPAGEMSB equals PAGEMSB + 1.

1. Values are guidelines only.
2. The Power-on Reset will not work unless the supply voltage has been below V_{POT} (falling)

Table 29-8. BODLEVEL Fuse Coding

BODLEVEL [2:0] Fuses	Min. V_{BOT}	Typ V_{BOT}	Max V_{BOT}	Units
111	BOD Disabled			V
110	1.7	1.8	2.0	
101	2.5	2.7	2.9	
100	4.1	4.3	4.5	
011	Reserved			
010				
001				
000				

1. V_{BOT} may be below nominal minimum operating voltage for some devices. For devices where this is the case, the device is tested down to $V_{CC} = V_{BOT}$ during the production test. This guarantees that a Brown-Out Reset will occur before V_{CC} drops to a voltage where correct operation of the microcontroller is no longer guaranteed. The test is performed using BODLEVEL = 110 and 101 .

29.6. External interrupts characteristics

Table 29-9. Asynchronous external interrupt characteristics.

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{INT}	Minimum pulse width for asynchronous external interrupt	-	50	-	ns

30.9. Pin Threshold and Hysteresis

Figure 30-25. I/O Pin Input Threshold vs. V_{CC} (V_{IH} , I/O Pin Read as '1')

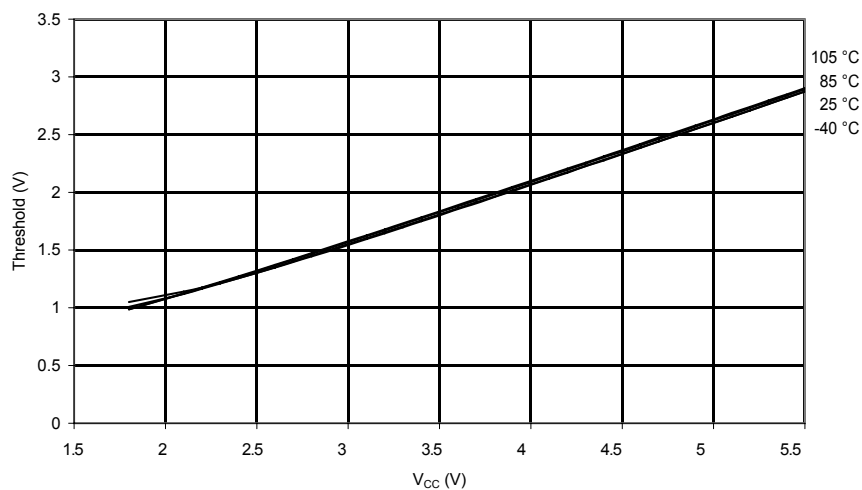


Figure 30-26. I/O Pin Input Threshold vs. V_{CC} (V_{IL} , I/O Pin Read as '0')

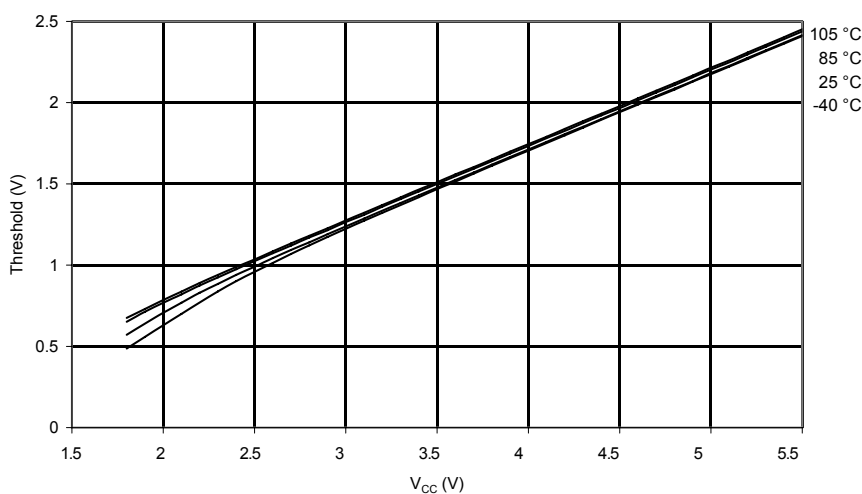


Figure 30-32. BOD Threshold vs. Temperature ($V_{CC} = 2.7V$)

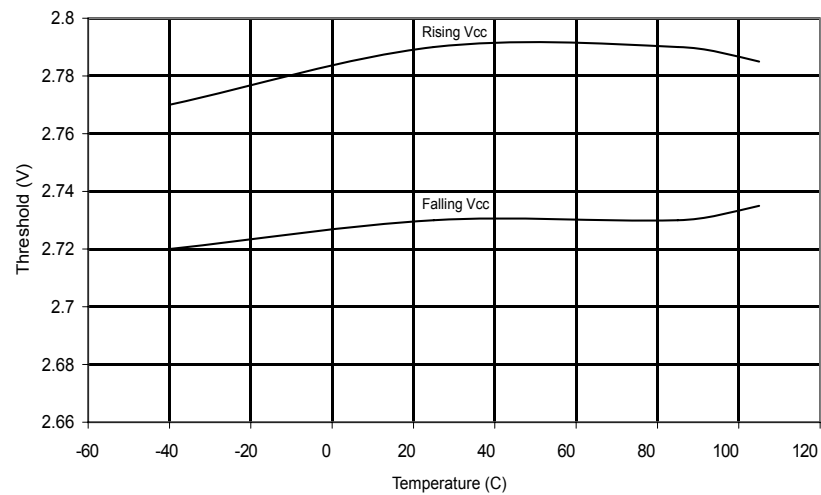
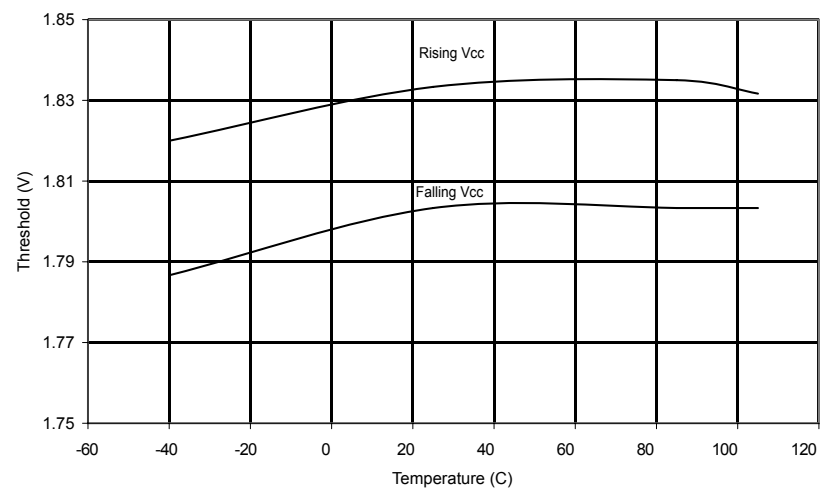


Figure 30-33. BOD Threshold vs. Temperature ($V_{CC} = 1.8V$)



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