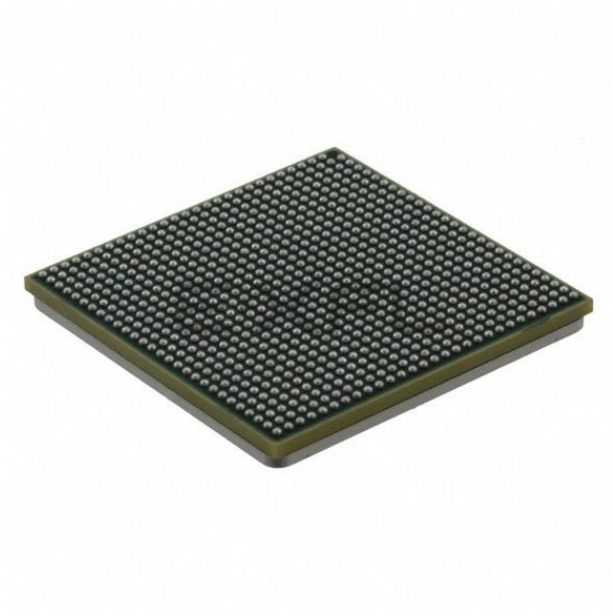

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e500 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 1.067GHz |
| Co-Processors/DSP | Signal Processing; SPE |
| RAM Controllers | DDR, DDR2, SDRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544avtarj |

  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

- Dual $I^2C$ controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave $I^2C$ mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the $I^2C$ interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended $I^2C$ addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Two protocol engines available on a per chip select basis:

  - General-purpose chip select machine (GPCM)
  - Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

- Two enhanced three-speed Ethernet controllers (eTSECs)
  - Three-speed support (10/100/1000 Mbps)
  - Two IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
  - Support for various Ethernet physical interfaces:
    - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, SGMII, and RGMII.
    - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
  - Flexible configuration for multiple PHY interface configurations.
  - TCP/IP acceleration and QoS features available
    - IP v4 and IP v6 header recognition on receive
    - IP v4 header checksum verification and generation
    - TCP and UDP checksum verification and generation
    - Per-packet configurable acceleration
    - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
    - Supported in all FIFO modes
  - Quality of service support:
    - Transmission from up to eight physical queues
    - Reception to up to eight physical queues
  - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
    - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
  - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
  - VLAN insertion and deletion
    - Per-frame VLAN control word or default VLAN for each eTSEC
    - Extracted VLAN control word passed to software separately
  - Retransmission following a collision
  - CRC generation and verification of inbound/outbound frames
  - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
  - MAC address recognition:
    - Exact match on primary and virtual 48-bit unicast addresses
    - VRRP and HSRP support for seamless router fail-over
    - Up to 16 exact-match MAC addresses supported

**Table 25. DC Receiver Electrical Characteristics (continued)**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| Input differential voltage | LSTS = 0 | $V_{rx\_diffpp}$ | 100 | — | 1200 | mV | 2, 4 |
| | LSTS = 1 | | 175 | — | | | |
| Loss of signal threshold | LSTS = 0 | $VI_{os}$ | 30 | — | 100 | mV | 3, 4 |
| | LSTS = 1 | | 65 | — | 175 | | |
| Input AC common mode voltage | | $V_{cm\_acpp}$ | — | — | 100 | mV | 5. |
| Receiver differential input impedance | | Zrx_diff | 80 | — | 120 | Ω | — |
| Receiver common mode input impedance | | Zrx_cm | 20 | — | 35 | Ω | — |
| Common mode input voltage | | Vcm | xcorevss | — | xcorevss | V | 6 |

**Notes:**
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
4. The LSTS shown in this table refers to the LSTS**CD** bit field of MPC8544E SerDes 2 control register 1.
5. $V_{CM\_ACp\text{-}p}$ is also referred to as peak-to-peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

## 8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (SD2_TX[n] and $\overline{\text{SD2\_TX}}$[n]) or at the receiver inputs (SD2_RX[n] and $\overline{\text{SD2\_RX}}$[n]) as depicted in Figure 10, respectively.

### 8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

**Table 26. SGMII Transmit AC Timing Specifications**

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic jitter | $J_D$ | — | — | 0.17 | UI p-p | — |
| Total jitter | $J_T$ | — | — | 0.35 | UI p-p | — |
| Unit interval | $U_I$ | 799.92 | 800 | 800.08 | ps | 2 |
| $V_{OD}$ fall time (80%–20%) | $t_{fall}$ | 50 | — | 120 | ps | — |
| $V_{OD}$ rise time (20%–80%) | $t_{rise}$ | 50 | — | 120 | ps | — |

**Notes;**
1. Source synchronous clock is not supported.
2. Each UI value is 800 ps ± 100 ppm.

### 8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

**Table 27. SGMII Receiver AC Timing Specifications**

At recommended operating conditions with XVDD_SRDS2 = 1.0 V ± 5%.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Deterministic jitter tolerance | $J_D$ | 0.37 | — | — | UI p-p | 1 |
| Combined deterministic and random jitter tolerance | $J_{DR}$ | 0.55 | — | — | UI p-p | 1 |
| Sinusoidal jitter tolerance | Jsin | 0.1 | — | — | UI p-p | 1 |
| Total jitter tolerance | $J_T$ | 0.65 | — | — | UI p-p | 1 |
| Bit error ratio | BER | — | — | $10^{-12}$ | — | — |
| Unit interval | UI | 799.92 | 800 | 800.08 | ps | 2 |
| AC coupling capacitor | $C_{TX}$ | 5 | — | 200 | nF | 3 |

**Notes:**
1. Measured at receiver.
2. Each UI value is 800 ps ± 100 ppm.
3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.

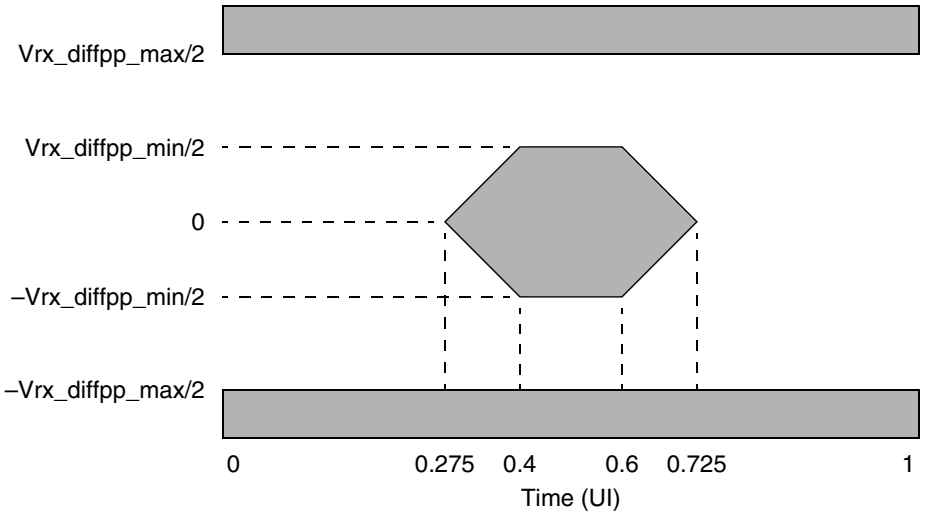



**Figure 9. Receive Input Compliance Mask**

### 8.5.2.2 GMII Receive AC Timing Specifications

Table 31 provides the GMII receive AC timing specifications.

**Table 31. GMII Receive AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| RX_CLK clock period | $t_{GRX}$ | — | 8.0 | — | ns | — |
| RX_CLK duty cycle | $t_{GRXH}/t_{GRX}$ | 35 | — | 65 | % | — |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{GRDVKH}$ | 2.0 | — | — | ns | — |
| RX_CLK to RXD[7:0], RX_DV, RX_ER hold time | $t_{GRDXKH}$ | 0.5 | — | — | ns | — |
| RX_CLK clock rise (20%–80%) | $t_{GRXR}$ | — | — | 1.0 | ns | — |
| RX_CLK clock fall time (80%–20%) | $t_{GRXF}$ | — | — | 1.0 | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{GRDVKH}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the $t_{RX}$ clock reference (K) going to the high state (H) or setup time. Also, $t_{GRDXKL}$ symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{GRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{GRX}$ represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 provides the AC test load for eTSEC.

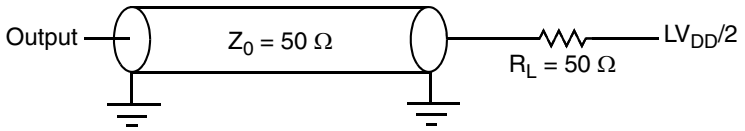



**Figure 14. eTSEC AC Test Load**

Figure 15 shows the GMII receive AC timing diagram.

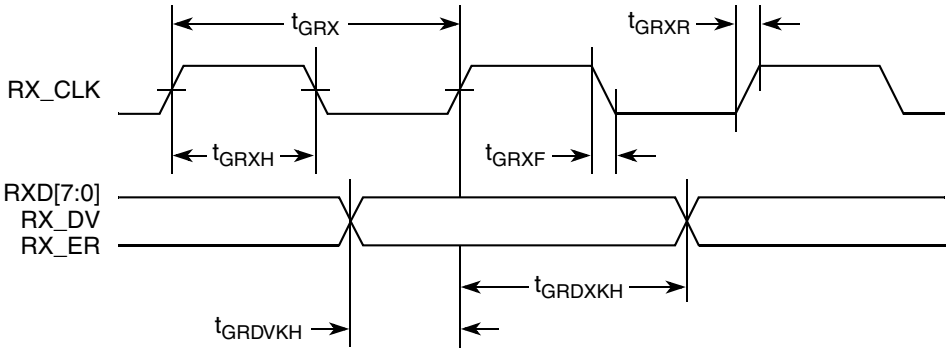



**Figure 15. GMII Receive AC Timing Diagram**

## 8.6 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

### 8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

**Table 34. TBI Transmit AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns | — |
| GTX_CLK to TCG[9:0] delay time | $t_{TTKHDX}$ | 0.2 | — | 5.0 | ns | 2 |
| GTX_CLK rise (20%–80%) | $t_{TTXR}$ | — | — | 1.0 | ns | — |
| GTX_CLK fall time (80%–20%) | $t_{TTXF}$ | — | — | 1.0 | ns | — |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state )(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TTKHDV}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, $t_{TTKHDX}$ symbolizes the TBI transmit timing (TT) with respect to the time from $t_{TTX}$ (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TTX}$ represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. Data valid $t_{TTKHDV}$ to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 19 shows the TBI transmit AC timing diagram.

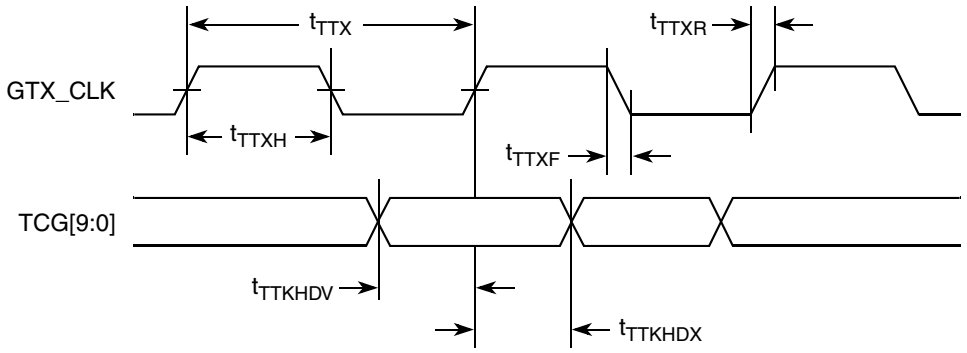



**Figure 19. TBI Transmit AC Timing Diagram**

### 8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

**Table 35. TBI Receive AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PMA_RX_CLK[0:1] clock period | $t_{TRX}$ | — | 16.0 | — | ns | — |
| PMA_RX_CLK[0:1] skew | $t_{SKTRX}$ | 7.5 | — | 8.5 | ns | — |

A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

**Table 36. TBI Single-Clock Mode Receive AC Timing Specification**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| RX_CLK clock period | $t_{TRR}$ | 7.5 | 8.0 | 8.5 | ns | — |
| RX_CLK duty cycle | $t_{TRRH}$ | 40 | 50 | 60 | % | — |
| RX_CLK peak-to-peak jitter | $t_{TRRJ}$ | — | — | 250 | ps | — |
| Rise time RX_CLK (20%–80%) | $t_{TRRR}$ | — | — | 1.0 | ns | — |
| Fall time RX_CLK (80%–20%) | $t_{TRRF}$ | — | — | 1.0 | ns | — |
| RCG[9:0] setup time to RX_CLK rising edge | $t_{TRRDV}$ | 2.0 | — | — | ns | — |
| RCG[9:0] hold time to RX_CLK rising edge | $t_{TRRDX}$ | 1.0 | — | — | ns | — |

A timing diagram for TBI receive appears in Figure 21.

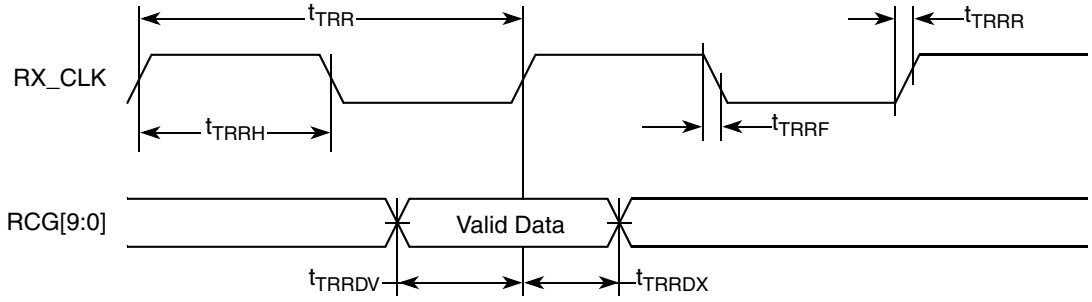



**Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram**

## 8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

**Table 37. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with $L/TV_{DD}$ of 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Data to clock output skew (at transmitter) | $t_{SKRGT\_TX}$ | –500 | 0 | 500 | ps | 5 |
| Data to clock input skew (at receiver) | $t_{SKRGT\_RX}$ | 1.0 | — | 2.8 | ns | 2 |
| Clock period duration | $t_{RGT}$ | 7.2 | 8.0 | 8.8 | ns | 3 |
| Duty cycle for 10BASE-T and 100BASE-TX | $t_{RGTH}/t_{RGT}$ | 40 | 50 | 60 | % | 3, 4 |
| Rise time (20%–80%) | $t_{RGTR}$ | — | — | 0.75 | ns | — |

# 9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC), MII Management."

## 9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 40.

**Table 40. MII Management DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply voltage (3.3 V) | $OV_{DD}$ | 3.135 | 3.465 | V | — |
| Output high voltage ($OV_{DD}$ = Min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.10 | 3.60 | V | — |
| Output low voltage ($OV_{DD}$ = Min, $I_{OL}$ = 1.0 mA) | $V_{OL}$ | GND | 0.50 | V | — |
| Input high voltage | $V_{IH}$ | 1.95 | — | V | — |
| Input low voltage | $V_{IL}$ | — | 0.90 | V | — |
| Input high current ($OV_{DD}$ = Max, $V_{IN}$ = 2.1 V) | $I_{IH}$ | — | 40 | μA | 1 |
| Input low current ($OV_{DD}$ = Max, $V_{IN}$ = 0.5 V) | $I_{IL}$ | –600 | — | μA | — |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1 and Table 2.

## 9.2 MII Management AC Electrical Specifications

Table 41 provides the MII management AC timing specifications.

**Table 41. MII Management AC Timing Specifications**

At recommended operating conditions with $OV_{DD}$ is 3.3 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC frequency | $f_{MDC}$ | — | 2.5 | — | MHz | 2 |
| MDC period | $t_{MDC}$ | — | 400 | — | ns | — |
| MDC clock pulse width high | $t_{MDCH}$ | 32 | — | — | ns | — |
| MDC to MDIO delay | $t_{MDKHDX}$ | $(16 \times t_{plb\_clk}) - 3$ | — | $(16 \times t_{plb\_clk}) + 3$ | ns | 3, 4 |
| MDIO to MDC setup time | $t_{MDDVKH}$ | 5 | — | — | ns | — |
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |
| MDC rise time | $t_{MDCR}$ | — | — | 10 | ns | — |

**Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)**

| Parameter | Symbol[1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Local bus clock to data valid for LAD/LDP | $t_{LBKLOV2}$ | — | 1.6 | ns | 4 |
| Local bus clock to address valid for LAD, and LALE | $t_{LBKLOV3}$ | — | 1.6 | ns | 4 |
| Output hold from local bus clock (except LAD/LDP and LALE) | $t_{LBKLOX1}$ | –4.1 | — | ns | 4 |
| Output hold from local bus clock for LAD/LDP | $t_{LBKLOX2}$ | –4.1 | — | ns | 4 |
| Local bus clock to output high Impedance (except LAD/LDP and LALE) | $t_{LBKLOZ1}$ | — | 1.4 | ns | 7 |
| Local bus clock to output high impedance for LAD/LDP | $t_{LBKLOZ2}$ | — | 1.4 | ns | 7 |

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the $t_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, $t_{LBKHOX}$ symbolizes local bus timing (LB) for the $t_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by $t_{LBKHKT}$.
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of $t_{LBOTOT}$ is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

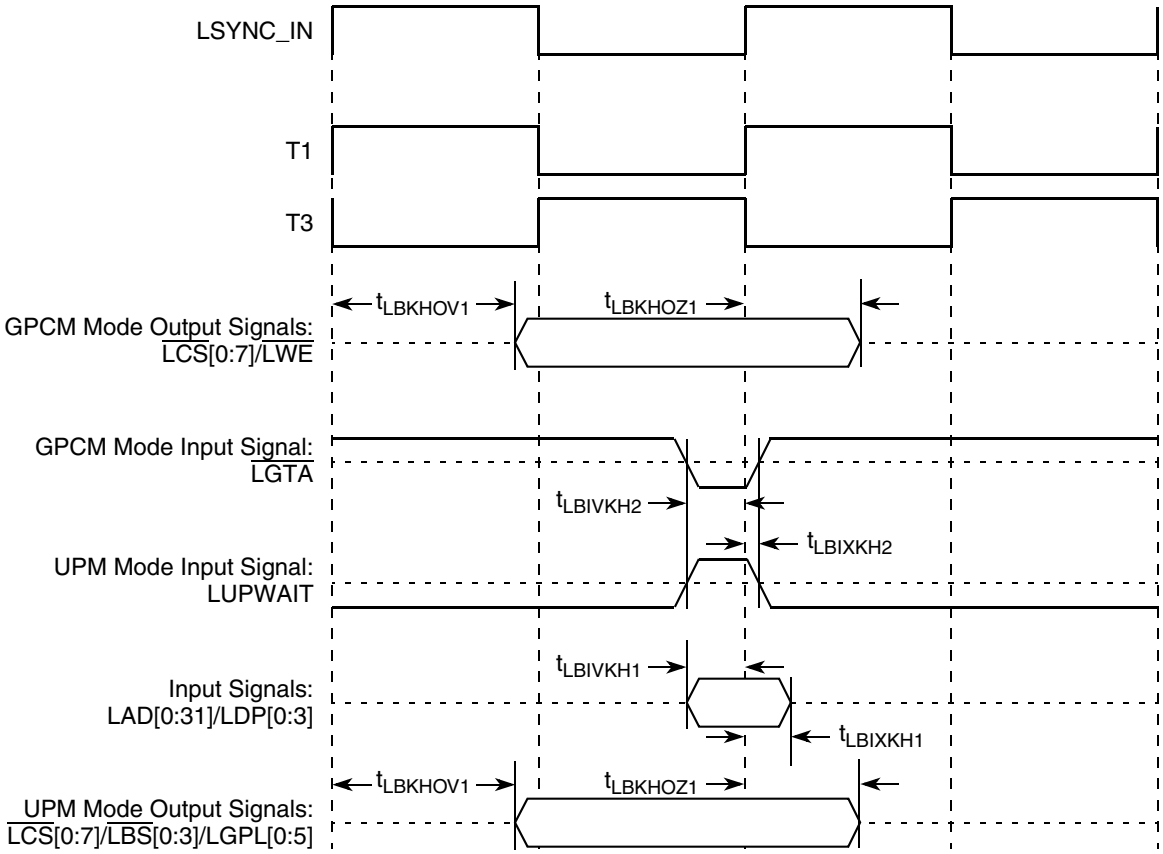



**Figure 30. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)**

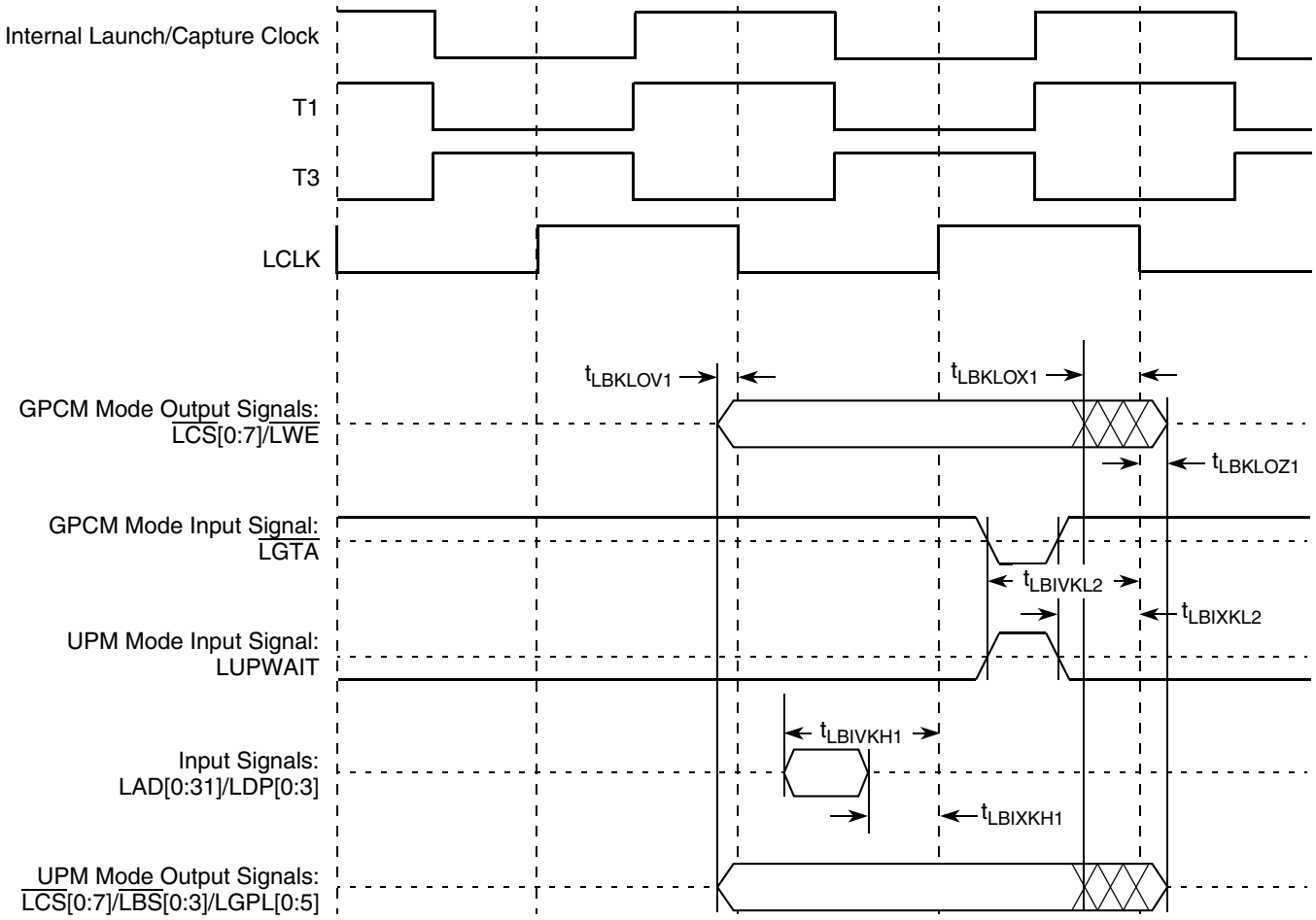
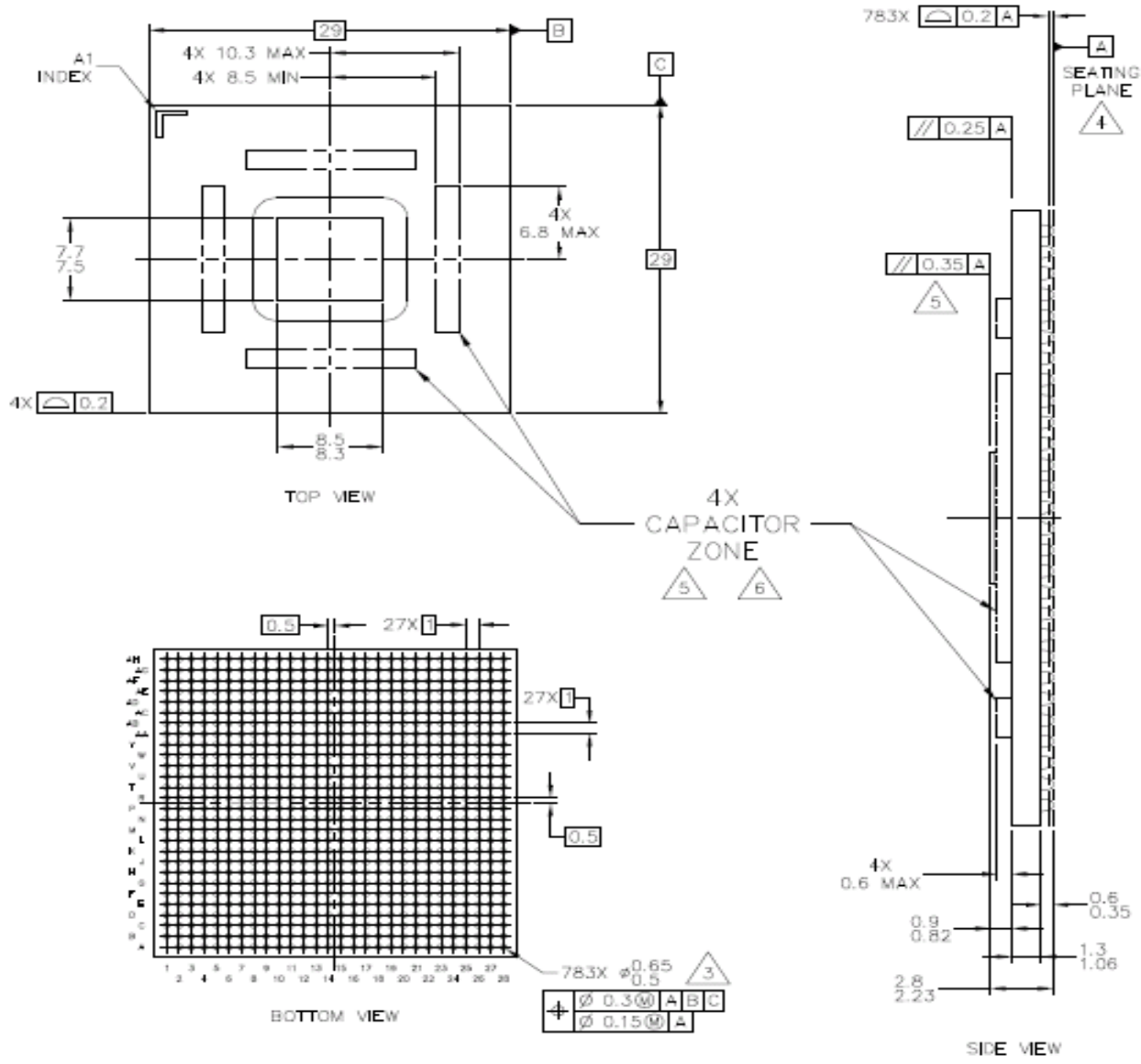



**Figure 31. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)**

## 18.2 Mechanical Dimensions of the MPC8544E FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8544E, 783 FC-PBGA package without a lid.




**Notes:**
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

**Figure 59. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8544E FC-PBGA without a Lid**

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Ethernet Management Interface** | | | | |
| EC_MDC | AC7 | O | $OV_{DD}$ | 4, 8, 14 |
| EC_MDIO | Y9 | I/O | $OV_{DD}$ | — |
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | T2 | I | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_RXD[7:0] | U10, U9, T10, T9, U8, T8, T7, T6 | I | $LV_{DD}$ | — |
| TSEC1_TXD[7:0] | T5, U5, V5, V3, V2, V1, U2, U1 | O | $LV_{DD}$ | 4, 8, 14 |
| TSEC1_COL | R5 | I | $LV_{DD}$ | — |
| TSEC1_CRS | T4 | I/O | $LV_{DD}$ | 16 |
| TSEC1_GTX_CLK | T1 | O | $LV_{DD}$ | — |
| TSEC1_RX_CLK | V7 | I | $LV_{DD}$ | — |
| TSEC1_RX_DV | U7 | I | $LV_{DD}$ | — |
| TSEC1_RX_ER | R9 | I | $LV_{DD}$ | 4, 8 |
| TSEC1_TX_CLK | V6 | I | $LV_{DD}$ | — |
| TSEC1_TX_EN | U4 | O | $LV_{DD}$ | 22 |
| TSEC1_TX_ER | T3 | O | $LV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 3)** | | | | |
| TSEC3_RXD[7:0] | P11, N11, M11, L11, R8, N10, N9, P10 | I | $LV_{DD}$ | — |
| TSEC3_TXD[7:0] | M7, N7, P7, M8, L7, R6, P6, M6 | O | $LV_{DD}$ | 4, 8, 14 |
| TSEC3_COL | M9 | I | $LV_{DD}$ | — |
| TSEC3_CRS | L9 | I/O | $LV_{DD}$ | 16 |
| TSEC3_GTX_CLK | R7 | O | $LV_{DD}$ | — |
| TSEC3_RX_CLK | P9 | I | $LV_{DD}$ | — |
| TSEC3_RX_DV | P8 | I | $LV_{DD}$ | — |
| TSEC3_RX_ER | R11 | I | $LV_{DD}$ | — |
| TSEC3_TX_CLK | L10 | I | $LV_{DD}$ | — |
| TSEC3_TX_EN | N6 | O | $LV_{DD}$ | 22 |
| TSEC3_TX_ER | L8 | O | $LV_{DD}$ | 4, 8 |
| **DUART** | | | | |
| $\overline{\text{UART\_CTS}}$[0:1] | AH8, AF6 | I | $OV_{DD}$ | — |
| $\overline{\text{UART\_RTS}}$[0:1] | AG8, AG9 | O | $OV_{DD}$ | — |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{SD2\_REF\_CLK}}$ | AF2 | I | $XV_{DD}$ | — |
| SD2_TST_CLK | AG4 | — | — | — |
| $\overline{\text{SD2\_TST\_CLK}}$ | AF4 | — | — | — |
| **General-Purpose Output** | | | | |
| GPOUT[0:7] | AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26 | O | $OV_{DD}$ | — |
| **General-Purpose Input** | | | | |
| GPIN[0:7] | AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20 | I | $OV_{DD}$ | — |
| **System Control** | | | | |
| $\overline{\text{HRESET}}$ | AG16 | I | $OV_{DD}$ | — |
| $\overline{\text{HRESET\_REQ}}$ | AG15 | O | $OV_{DD}$ | 21 |
| $\overline{\text{SRESET}}$ | AG19 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_IN}}$ | AH5 | I | $OV_{DD}$ | — |
| $\overline{\text{CKSTP\_OUT}}$ | AA12 | O | $OV_{DD}$ | 2, 4 |
| **Debug** | | | | |
| TRIG_IN | AC5 | I | $OV_{DD}$ | — |
| TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$ | AB5 | O | $OV_{DD}$ | 5, 8, 15, 21 |
| MSRCID[0:1] | Y7, W9 | O | $OV_{DD}$ | 4, 5, 8 |
| MSRCID[2:4] | AA9, AB6, AD5 | O | $OV_{DD}$ | 5, 15, 21 |
| MDVAL | Y8 | O | $OV_{DD}$ | 5 |
| CLK_OUT | AE16 | O | $OV_{DD}$ | 10 |
| **Clock** | | | | |
| RTC | AF15 | I | $OV_{DD}$ | — |
| SYSCLK | AH16 | I | $OV_{DD}$ | — |
| **JTAG** | | | | |
| TCK | AG28 | I | $OV_{DD}$ | — |
| TDI | AH28 | I | $OV_{DD}$ | 11 |
| TDO | AF28 | O | $OV_{DD}$ | 10 |
| TMS | AH27 | I | $OV_{DD}$ | 11 |
| $\overline{\text{TRST}}$ | AH22 | I | $OV_{DD}$ | 11 |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $V_{DD}$ | L16, L14, M13, M15, M17, N12, N14, N16, N18, P13, P15, P17, R12, R14, R16, R18, T13, T15, T17, U12, U14, U16, U18, | Power for core (1.0 V) | $V_{DD}$ | — |
| SVDD_SRDS | M27, N25, P28, R24, R26, T24, T27, U25, W24, W26, Y24, Y27, AA25, AB28, AD27 | Core power for SerDes 1 transceivers (1.0 V) | $SV_{DD}$ | — |
| SVDD_SRDS2 | AB1, AC26, AD2, AE26, AG2 | Core power for SerDes 2 transceivers (1.0 V) | $SV_{DD}$ | — |
| XVDD_SRDS | M21, N23, P20, R22, T20, U23, V21, W22, Y20 | Pad power for SerDes 1 transceivers (1.0 V) | $XV_{DD}$ | — |
| XVDD_SRDS2 | Y6, AA6, AA23, AF5, AG5 | Pad power for SerDes 2 transceivers (1.0 V) | $XV_{DD}$ | — |
| XGND_SRDS | M20, M24, N22, P21, R23, T21, U22, V20, W23, Y21 | — | — | — |
| XGND_SRDS2 | Y4, AA4, AA22, AD4, AE4, AH4 | — | — | — |
| SGND_SRDS | M28, N26, P24, P27, R25, T28, U24, U26, V24, W25, Y28, AA24, AA26, AB24, AB27, AC24, AD28 | — | — | — |
| AGND_SRDS | V27 | SerDes PLL GND | — | — |
| SGND_SRDS2 | Y2, AA1, AB3, AC2, AC3, AC25, AD3, AD24, AE3, AE1, AE25, AF3, AH2 | — | — | — |
| AGND_SRDS2 | AF1 | SerDes PLL GND | — | — |
| AVDD_LBIU | C28 | Power for local bus PLL (1.0 V) | — | 19 |
| AVDD_PCI1 | AH20 | Power for PCI PLL (1.0 V) | — | 19 |
| AVDD_CORE | AH14 | Power for e500 PLL (1.0 V) | — | 19 |
| AVDD_PLAT | AH18 | Power for CCB PLL (1.0 V) | — | 19 |

**Table 62. MPC8544E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|

6.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.2, "CCB/SYSCLK PLL Ratio."

7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."

8.Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.

9.For proper state of these signals during reset, $\overline{\text{DMA\_DACK}}$[1] must be pulled down to GND through a resistor. $\overline{\text{DMA\_DACK}}$[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on $\overline{\text{DMA\_DACK}}$[0].

10.This output is actively driven during reset rather than being three-stated during reset.

11.These JTAG pins have weak internal pull-up P-FETs that are always enabled.

12.These pins are connected to the $V_{DD}$/GND planes internally and may be used by the core power supply to improve tracking and regulation.

13.Anode and cathode of internal thermal diode.

14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.

15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.

16.This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18.These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to $OV_{DD}$ for normal machine operation.

19.Independent supplies derived from board $V_{DD}$.

20.Recommend a pull-up resistor (1 K~) be placed on this pin to $OV_{DD}$.

21.The following pins must not be pulled down during power-on reset: $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], and ASLEEP.

22.This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.

23.General-purpose POR configuration of user system.

24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.

25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected $GV_{DD}$ through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.

26.For SGMII mode.

27.Connect to GND.

28.For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.

### 19.6.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. Refer to Section 4.4, "Platform to FIFO Restrictions," for additional information.

**Table 69. FIFO Maximum Speed Restrictions**

| Platform Speed (MHz) | Maximum FIFO Speed for Reference Clocks TSEC*n*_TX_CLK, TSEC*n*_RX_CLK (MHz)[1] |
|---|---|
| 533 | 126 |
| 400 | 94 |

**Note:**
1. FIFO speed should be less than 24% of the platform speed.

# 20 Thermal

This section describes the thermal specifications of the MPC8544E.

## 20.1 Thermal Characteristics

Table 70 provides the package thermal characteristics.

**Table 70. Package Thermal Characteristics**

| Characteristic | JEDEC Board | Symbol | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction-to-ambient natural convection | Single layer board (1s) | $R_{\theta JA}$ | 26 | °C/W | 1, 2 |
| Junction-to-ambient natural convection | Four layer board (2s2p) | $R_{\theta JA}$ | 21 | °C/W | 1, 2 |
| Junction-to-ambient (@200 ft/min) | Single layer board (1s) | $R_{\theta JA}$ | 21 | °C/W | 1, 2 |
| Junction-to-ambient (@200 ft/min) | Four layer board (2s2p) | $R_{\theta JA}$ | 17 | °C/W | 1, 2 |
| Junction-to-board thermal | — | $R_{\theta JB}$ | 12 | °C/W | 3 |
| Junction-to-case thermal | — | $R_{\theta JC}$ | <0.1 | °C/W | 4 |

**Notes:**
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.
3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1°C/W.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

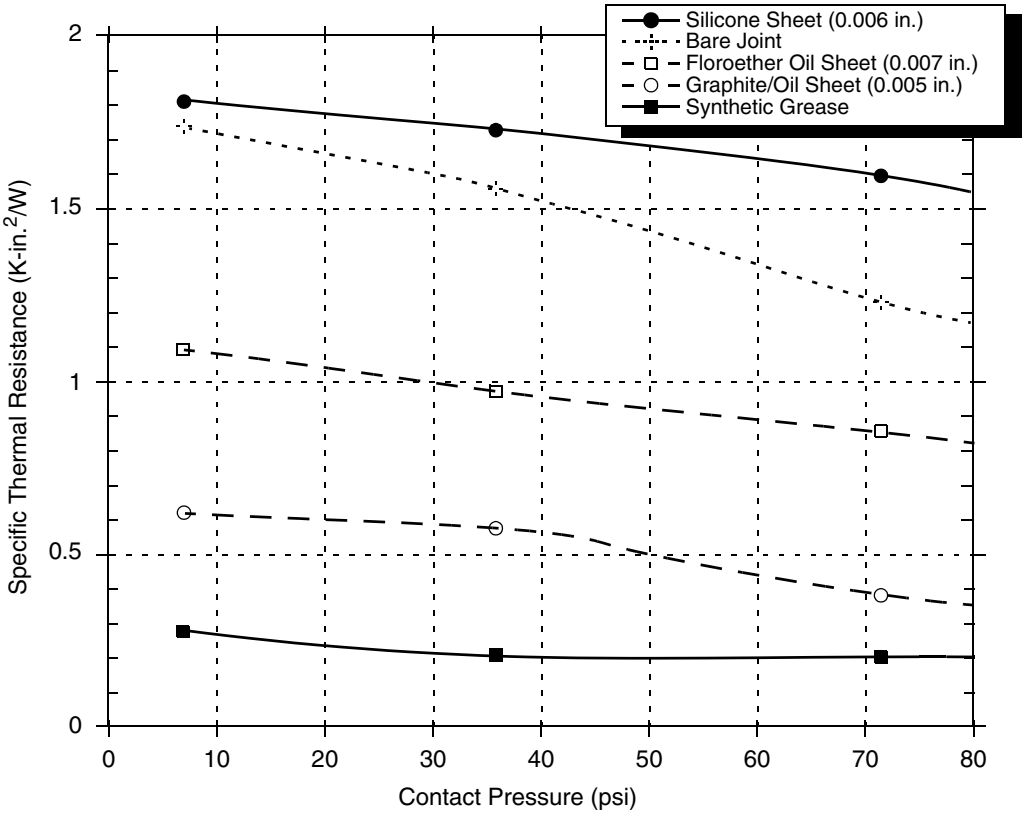



**Figure 63. Thermal Performance of Select Thermal Interface Materials**

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

resistance of the pull-up devices. $R_P$ and $R_N$ are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

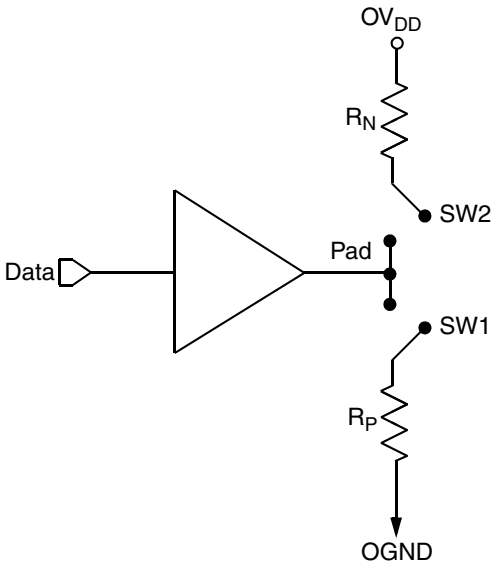



**Figure 67. Driver Impedance Measurement**

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 90°C.

**Table 73. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|
| $R_N$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |
| $R_P$ | 43 Target | 25 Target | 20 Target | $Z_0$ | W |

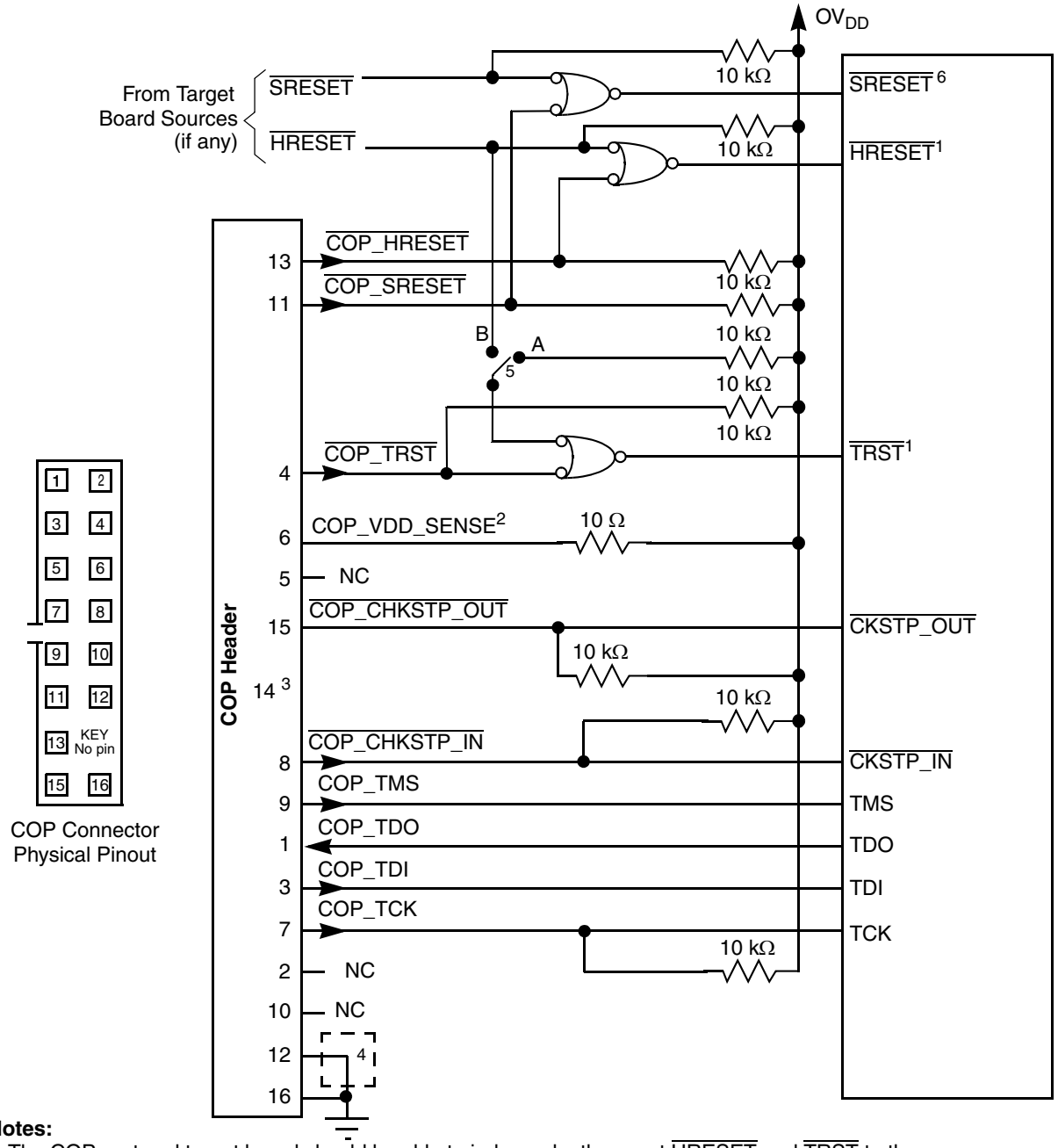
**Note:** Nominal supply voltages. See Table 1.

## 21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has

Figure 69 shows the JTAG interface connection.




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 69. JTAG Interface Connection**