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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544cvjaqga

- Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- 36-bit real addressing
- Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
- Enhanced hardware and software debug support
- Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
 - Flexible configuration
 - Full ECC support on 64-bit boundary in both cache and SRAM modes
 - Cache mode supports instruction caching, data caching, or both.
 - External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
 - 1, 2, or 4 ways can be configured for stashing only.
 - Eight-way set-associative cache organization (32-byte cache lines)
 - Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
 - Global locking and flash clearing done through writes to L2 configuration registers
 - Instruction and data locks can be flash cleared separately.
 - SRAM features include the following:
 - I/O devices access SRAM regions by marking transactions as snoopable (global).
 - Regions can reside at any aligned location in the memory map.
 - Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
 - Eight local access windows define mapping within local 36-bit address space.
 - Inbound and outbound ATMUs map to larger external address spaces.
 - Three inbound windows plus a configuration window on PCI and PCI Express
 - Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
 - Programmable timing supporting DDR and DDR2 SDRAM
 - 64-bit data interface

- General-purpose chip select machine (GPCM)
- Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Two enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Two IEEE Std 802.3™, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, SGMII, and RGMII.
 - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
 - Flexible configuration for multiple PHY interface configurations.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1™ virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported

4.5 Other Input Clocks

For information on the input clocks of other functional blocks of the platform such as SerDes, and eTSEC, see the specific section of this document.

5 RESET Initialization

This section describes the AC electrical specifications for the RESET initialization timing requirements of the MPC8544E. [Table 8](#) provides the RESET initialization AC timing specifications for the DDR SDRAM component(s).

Table 8. RESET Initialization Timing Specifications¹

Parameter/Condition	Min	Max	Unit	Notes
Required assertion time of $\overline{\text{HRESET}}$	100	—	μs	—
Minimum assertion time for $\overline{\text{SRESET}}$	3	—	SYCLKs	1
PLL input setup time with stable SYCLK before $\overline{\text{HRESET}}$ negation	100	—	μs	—
Input setup time for POR configs (other than PLL config) with respect to negation of $\overline{\text{HRESET}}$	4	—	SYCLKs	1
Input hold time for all POR configs (including PLL config) with respect to negation of $\overline{\text{HRESET}}$	2	—	SYCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{HRESET}}$	—	5	SYCLKs	1

Note:

1. SYCLK is the primary clock input for the MPC8544E.

[Table 9](#) provides the PLL lock times.

Table 9. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Notes
Core and platform PLL lock times	—	100	μs	—
Local bus PLL	—	50	μs	—
PCI bus lock time	—	50	μs	—

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8544E. Note that DDR SDRAM is $G_{V_{DD}}(\text{typ}) = 2.5 \text{ V}$ and DDR2 SDRAM is $G_{V_{DD}}(\text{typ}) = 1.8 \text{ V}$.

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Low-level output voltage ($OV_{DD} = \min, I_{OL} = 2 \text{ mA}$)	V_{OL}	—	0.4	V	—

Note:

- Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in [Table 1](#) and [Table 2](#).

7.2 DUART AC Electrical Specifications

[Table 20](#) provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:

- CCB clock refers to the platform clock.
- Actual attainable baud rate will be limited by the latency of interrupt processing.
- The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—SGMII/GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The SGMII interfaces follow the *Serial Gigabit Media-Independent Interface (SGMII) Specification Version 1.8*. The electrical characteristics for MDIO and MDC are specified in [Section 9, “Ethernet Management Interface Electrical](#)

Table 25. DC Receiver Electrical Characteristics (continued)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Input differential voltage	LSTS = 0	V_{RX_DIFFP}	100	—	1200	mV	2, 4
	LSTS = 1		175	—			
Loss of signal threshold	LSTS = 0	V_{LOS}	30	—	100	mV	3, 4
	LSTS = 1		65	—	175		
Input AC common mode voltage		V_{CM_ACPP}	—	—	100	mV	5.
Receiver differential input impedance		Z_{RX_DIFF}	80	—	120	Ω	—
Receiver common mode input impedance		Z_{RX_CM}	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Notes:

1. Input must be externally AC-coupled.
2. V_{RX_DIFFP} is also referred to as peak-to-peak input differential voltage
3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to [Section 17.4.3, "Differential Receiver \(RX\) Input Specifications,"](#) for further explanation.
4. The LSTS shown in this table refers to the LSTSCD bit field of MPC8544E SerDes 2 control register 1.
5. V_{CM_ACPP} is also referred to as peak-to-peak AC common mode voltage.
6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs ($SD2_TX[n]$ and $\overline{SD2_TX}[n]$) or at the receiver inputs ($SD2_RX[n]$ and $\overline{SD2_RX}[n]$) as depicted in [Figure 10](#), respectively.

8.4.1 SGMII Transmit AC Timing Specifications

[Table 26](#) provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with $XVDD_SRDS2 = 1.0\text{ V} \pm 5\%$.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit interval	U_I	799.92	800	800.08	ps	2
V_{OD} fall time (80%–20%)	t_{fall}	50	—	120	ps	—
V_{OD} rise time (20%–80%)	t_{rise}	50	—	120	ps	—

Notes;

1. Source synchronous clock is not supported.
2. Each UI value is $800\text{ ps} \pm 100\text{ ppm}$.

Figure 10 provides the AC test load for SGMII.

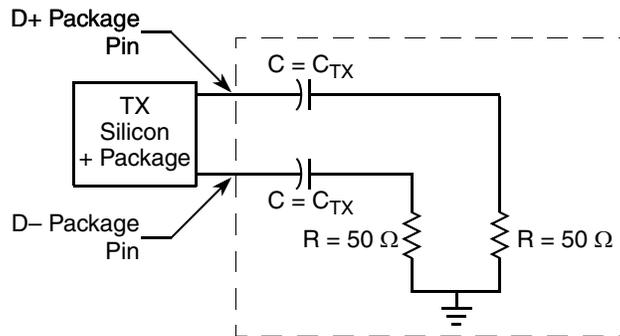


Figure 10. SGMII AC Test/Measurement Load

8.5 FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.5.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC n TSEC n _TX_CLK, while the receive clock must be applied to pin TSEC n _RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC n _GTX_CLK pin (while transmit data appears on TSEC n _TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC n _GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in [Table 28](#) and [Table 29](#).

Table 28. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—

8.6.1 MII Transmit AC Timing Specifications

Table 32 provides the MII transmit AC timing specifications.

Table 32. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

Note:

- The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 16 shows the MII transmit AC timing diagram.

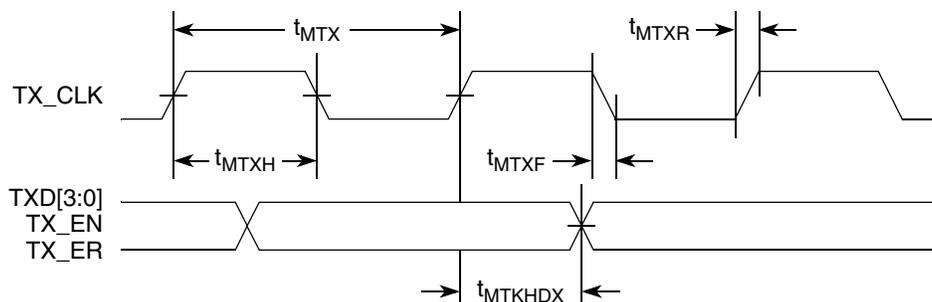


Figure 16. MII Transmit AC Timing Diagram

8.6.2 MII Receive AC Timing Specifications

Table 33 provides the MII receive AC timing specifications.

Table 33. MII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%. or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	—
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	—
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—

Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit	Notes
Fall time (20%–80%)	t _{RGTF}	—	—	0.75	ns	—

Notes:

1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.

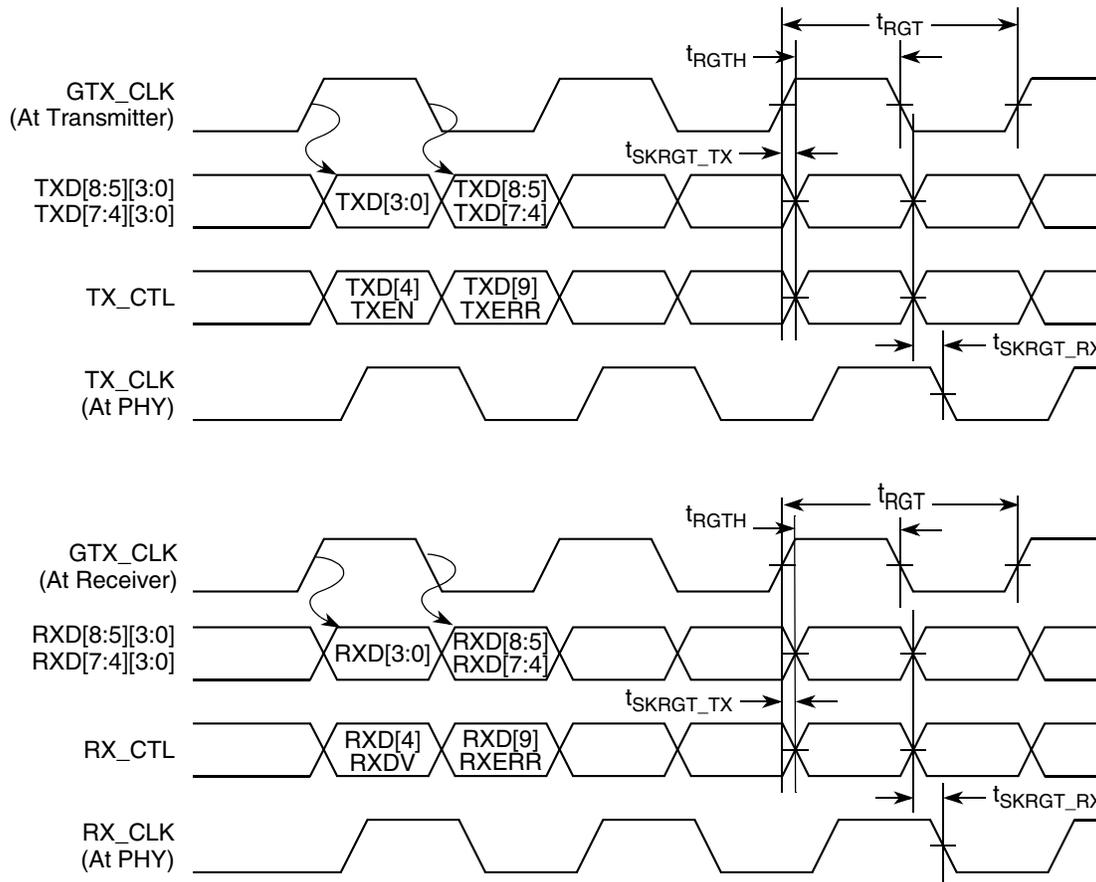


Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams

Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	$t_{LBKLOV2}$	—	1.6	ns	4
Local bus clock to address valid for LAD, and LALE	$t_{LBKLOV3}$	—	1.6	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKLOX1}$	-4.1	—	ns	4
Output hold from local bus clock for LAD/LDP	$t_{LBKLOX2}$	-4.1	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKLOZ1}$	—	1.4	ns	7
Local bus clock to output high impedance for LAD/LDP	$t_{LBKLOZ2}$	—	1.4	ns	7

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by t_{LBKHKT} .
3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at $BV_{DD}/2$.
4. All signals are measured from $BV_{DD}/2$ of the rising edge of local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.
5. Input timings are measured at the pin.
6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

17.4.1 Differential Transmitter (TX) Output

Table 59 defines the specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 59. Differential Transmitter (TX) Output Specifications

Symbol	Parameter	Min	Nom	Max	Unit	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps \pm 300 ppm. UI does not account for Spread Spectrum Clock dictated variations. See Note 1.
$V_{TX-DIFFp-p}$	Differential peak-to-peak output voltage	0.8	—	1.2	V	$V_{TX-DIFFp-p} = 2 * V_{TX-D+} - V_{TX-D-} $. See Note 2.
$V_{TX-DE-RATIO}$	De-emphasized differential output voltage (ratio)	-3.0	-3.5	-4.0	dB	Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 2.
T_{TX-EYE}	Minimum TX eye width	0.70	—	—	UI	The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI. See Notes 2 and 3.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between the jitter median and maximum deviation from the median.	—	—	0.15	UI	Jitter is defined as the measurement variation of the crossing points ($V_{TX-DIFFp-p} = 0$ V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2 and 3.
$T_{TX-RISE}, T_{TX-FALL}$	D+/D- TX output rise/fall time	0.125	—	—	UI	See Notes 2 and 5.
$V_{TX-CM-ACp}$	RMS AC peak common mode output voltage	—	—	20	mV	$V_{TX-CM-ACp} = \text{RMS}(IV_{TXD+} - V_{TXD-}/2 - V_{TX-CM-DC})$ $V_{TX-CM-DC} = DC_{(avg)}$ of $IV_{TX-D+} - V_{TX-D-}/2$ See Note 2.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during LO and electrical idle	0	—	100	mV	$ V_{TX-CM-DC}(\text{during LO}) - V_{TX-CM-Idle-DC}(\text{During Electrical Idle}) \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $IV_{TX-D+} - V_{TX-D-}/2$ [LO] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $IV_{TX-D+} - V_{TX-D-}/2$ [Electrical Idle] See Note 2.
$V_{TX-CM-DC-LINE-DELTA}$	Absolute delta of DC common mode between D+ and D-	0	—	25	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25$ mV $V_{TX-CM-DC-D+} = DC_{(avg)}$ of IV_{TX-D+} $V_{TX-CM-DC-D-} = DC_{(avg)}$ of IV_{TX-D-} See Note 2.
$V_{TX-IDLE-DIFFp}$	Electrical idle differential peak output voltage	0	—	20	mV	$V_{TX-IDLE-DIFFp} = V_{TX-IDLE-D+} - V_{TX-IDLE-D-} \leq 20$ mV See Note 2.

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in [Table 61](#).

Table 61. Package Parameters

Parameter	PBGA ¹
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Note:

1. (FC-PBGA) without a lid.

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DDR SDRAM Memory Interface				
MDQ[0:63]	A26, B26, C22, D21, D25, B25, D22, E21, A24, A23, B20, A20, A25, B24, B21, A21, E19, D19, E16, C16, F19, F18, F17, D16, B18, A18, A15, B14, B19, A19, A16, B15, D1, F3, G1, H2, E4, G5, H3, J4, B2, C3, F2, G2, A2, B3, E1, F1, L5, L4, N3, P3, J3, K4, N4, P4, J1, K1, P1, R1, J2, K2, N1, R2	I/O	GV _{DD}	—
MECC[0:7]	G12, D14, F11, C11, G14, F14, C13, D12	I/O	GV _{DD}	—
MDM[0:8]	C25, B23, D18, B17, G4, C2, L3, L2, F13	O	GV _{DD}	21
$\overline{\text{MDQS}}$ [0:8]	D24, B22, C18, A17, J5, C1, M4, M2, E13	I/O	GV _{DD}	—
MDQS[0:8]	C23, A22, E17, B16, K5, D2, M3, P2, D13	I/O	GV _{DD}	—
MA[0:15]	B7, G8, C8, A10, D9, C10, A11, F9, E9, B12, A5, A12, D11, F7, E10, F10	O	GV _{DD}	—
MBA[0:2]	A4, B5, B13	O	GV _{DD}	—
$\overline{\text{MWE}}$	B4	O	GV _{DD}	—
$\overline{\text{MCAS}}$	E7	O	GV _{DD}	—
$\overline{\text{MRAS}}$	C5	O	GV _{DD}	—
MCKE[0:3]	H10, K10, G10, H9	O	GV _{DD}	10
$\overline{\text{MCS}}$ [0:3]	D3, H6, C4, G6	O	GV _{DD}	—
MCK[0:5]	A9, J11, J6, A8, J13, H8	O	GV _{DD}	—
$\overline{\text{MCK}}$ [0:5]	B9, H11, K6, B8, H13, J8	O	GV _{DD}	—
MODT[0:3]	E5, H7, E6, F6	O	GV _{DD}	—
MDIC[0:1]	H15, K15	I/O	GV _{DD}	25
TEST_IN	A13	I	—	27
TEST_OUT	A6	O	—	17
Local Bus Controller Interface				
LAD[0:31]	K22, L21, L22, K23, K24, L24, L25, K25, L28, L27, K28, K27, J28, H28, H27, G27, G26, F28, F26, F25, E28, E27, E26, F24, E24, C26, G24, E23, G23, F22, G22, G21	I/O	BV _{DD}	23
LDP[0:3]	K26, G28, B27, E25	I/O	BV _{DD}	—
LA[27]	L19	O	BV _{DD}	4, 8
LA[28:31]	K16, K17, H17, G17	O	BV _{DD}	4, 6, 8
$\overline{\text{LCS}}$ [0:4]	K18, G19, H19, H20, G16	O	BV _{DD}	—
$\overline{\text{LCS5/DMA_DREQ2}}$	H16	I/O	BV _{DD}	1

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{SD2_REF_CLK}}$	AF2	I	XV _{DD}	—
SD2_TST_CLK	AG4	—	—	—
$\overline{\text{SD2_TST_CLK}}$	AF4	—	—	—
General-Purpose Output				
GPOUT[0:7]	AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26	O	OV _{DD}	—
General-Purpose Input				
GPIN[0:7]	AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20	I	OV _{DD}	—
System Control				
$\overline{\text{HRESET}}$	AG16	I	OV _{DD}	—
$\overline{\text{HRESET_REQ}}$	AG15	O	OV _{DD}	21
$\overline{\text{SRESET}}$	AG19	I	OV _{DD}	—
$\overline{\text{CKSTP_IN}}$	AH5	I	OV _{DD}	—
$\overline{\text{CKSTP_OUT}}$	AA12	O	OV _{DD}	2, 4
Debug				
TRIG_IN	AC5	I	OV _{DD}	—
TRIG_OUT/READY/ $\overline{\text{QUIESCE}}$	AB5	O	OV _{DD}	5, 8, 15, 21
MSRCID[0:1]	Y7, W9	O	OV _{DD}	4, 5, 8
MSRCID[2:4]	AA9, AB6, AD5	O	OV _{DD}	5, 15, 21
MDVAL	Y8	O	OV _{DD}	5
CLK_OUT	AE16	O	OV _{DD}	10
Clock				
RTC	AF15	I	OV _{DD}	—
SYSCLK	AH16	I	OV _{DD}	—
JTAG				
TCK	AG28	I	OV _{DD}	—
TDI	AH28	I	OV _{DD}	11
TDO	AF28	O	OV _{DD}	10
TMS	AH27	I	OV _{DD}	11
$\overline{\text{TRST}}$	AH22	I	OV _{DD}	11

Table 72. MPC8544E Thermal Model (continued)

Conductivity	Value	Units
Solder and Air (29 × 29 × 0.58 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

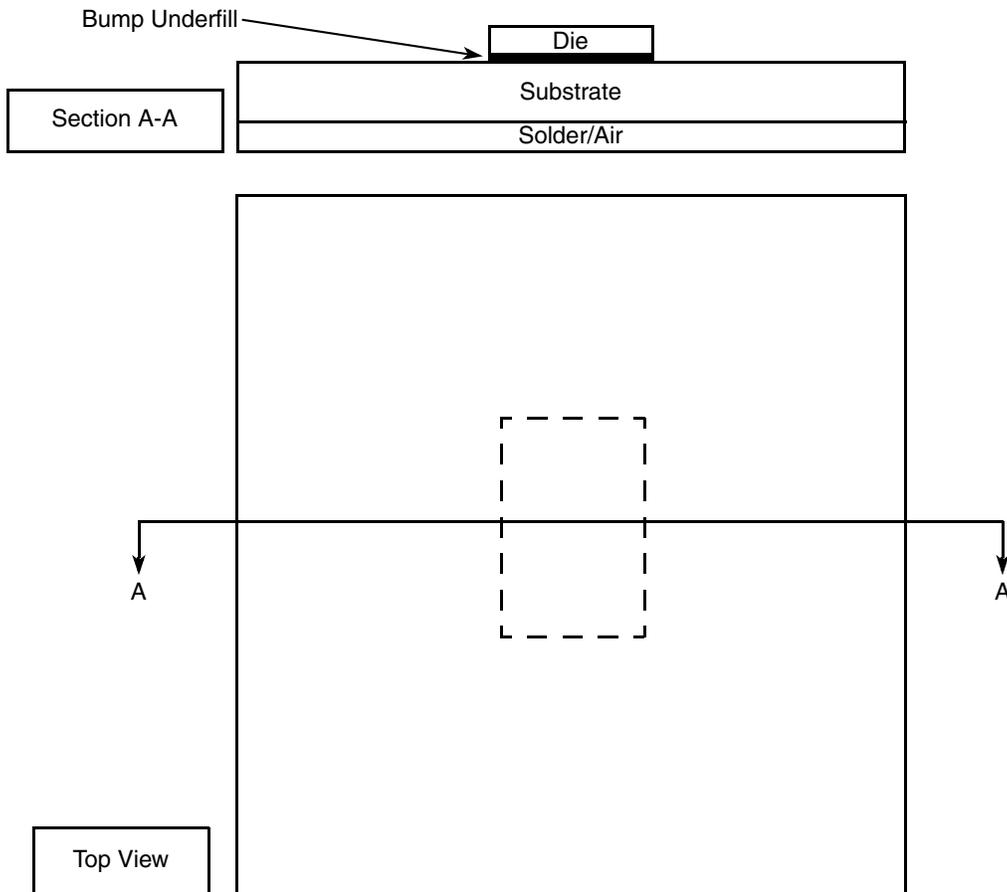


Figure 60. System Level Thermal Model for MPC8544E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

21.2 PLL Power Supply Filtering

Each of the PLLs listed above is provided with power through independent power supply pins (AV_{DD_PLAT} , AV_{DD_CORE} , AV_{DD_PCI} , AV_{DD_LBIU} , and AV_{DD_SRDS} , respectively). The AV_{DD} level should always be equivalent to V_{DD} , and preferably these voltages will be derived directly from V_{DD} through a low frequency filter scheme such as the following.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in [Figure 65](#), one to each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of 783 FC-PBGA the footprint, without the inductance of vias.

[Figure 65](#) shows the PLL power supply filter circuit.

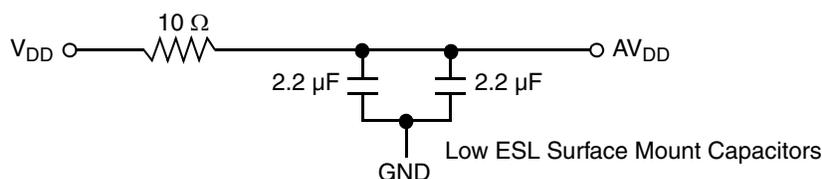
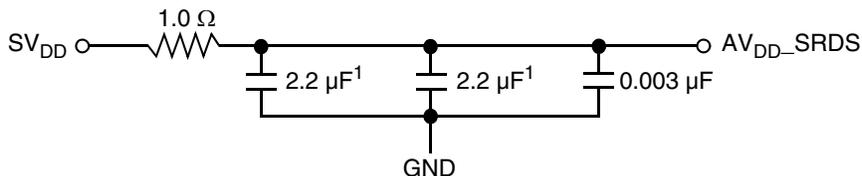


Figure 65. MPC8544E PLL Power Supply Filter Circuit

The AV_{DD_SRDSn} signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in [Figure 66](#). For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD_SRDSn} balls. The 0.003- μF capacitor is closest to the balls, followed by the 1- μF capacitor, and finally the 1- Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.



Note:

1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 66. SerDes PLL Power Supply Filter Circuit

resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.

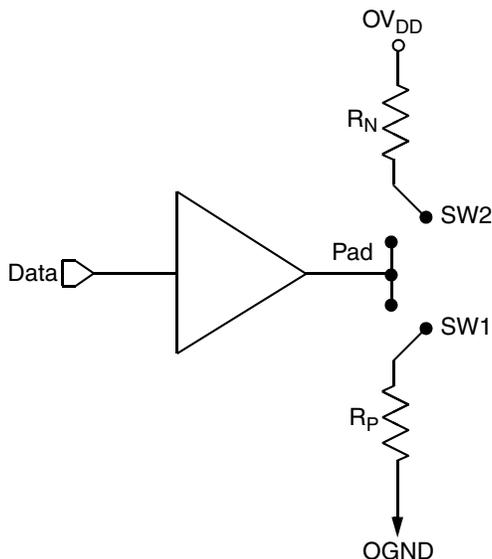


Figure 67. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 90°C .

Table 73. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R_N	43 Target	25 Target	20 Target	Z_0	W
R_P	43 Target	25 Target	20 Target	Z_0	W

Note: Nominal supply voltages. See Table 1.

21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of $4.7\text{ k}\Omega$ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately $20\text{ k}\Omega$. This value should permit the $4.7\text{-k}\Omega$ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in [Figure 69](#). Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the $\overline{\text{TCK}}$ and $\overline{\text{TMS}}$ signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in [Figure 69](#) allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in [Figure 68](#), for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in [Figure 68](#) is common to all known emulators.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in [Section 22.3, “Part Marking.”](#) Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. [Table 74](#) provides a description for commercial and industrial qualifications.

Table 74. Commercial and Industrial Description

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Note:

1. Refer to [Table 2](#) for operating temperature ranges. Temperature is independent of tier and varies per product.

22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

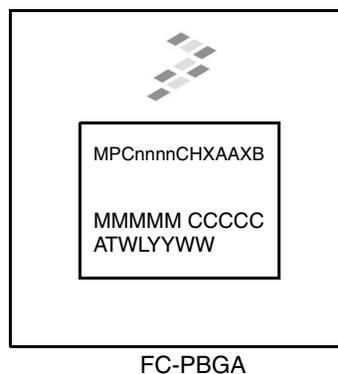
<i>MPC</i>	<i>nnnn</i>	<i>E</i>	<i>C</i>	<i>HX</i>	<i>AA</i>	<i>X</i>	<i>B</i>
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ¹	Processor Frequency ²	Platform Frequency	Revision Level
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(-40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:

1. See Section 18, "Package Description," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.



Notes:

- MMMMM is the 5-digit mask number.
- ATWLYYWW is the traceability code.
- CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device

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Document Number: MPC8544EEC

Rev. 8

09/2015

