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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544cvtalfa

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC8544E Overview

- Two key (K1, K2, K1) or three key (K1, K2, K3)
- ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU-Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Two protocol engines available on a per chip select basis:

Power Characteristics



3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V _{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	667	333	1.0	65	2.6	1, 2
Thermal				105	4.5	1, 3
Maximum					7.15	1, 4
Typical	800	400	1.0	65	2.9	1, 2
Thermal				105	4.8	1, 3
Maximum					7.35	1, 4
Typical	1000	400	1.0	65	3.6	1, 2
Thermal				105	5.3	1, 3
Maximum					7.5	1, 4
Typical	1067	533	1.0	65	3.9	1, 2
Thermal				105	6.0	1, 3
Maximum				105	7.7	1, 4

Table 4. MPC8544ECore Power Dissipation

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.

- Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
- Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
- 4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

4 Input Clocks

This section contains the following subsections:

- Section 4.1, "System Clock Timing"
- Section 4.2, "Real-Time Clock Timing"
- Section 4.3, "eTSEC Gigabit Reference Clock Timing"
- Section 4.4, "Platform to FIFO Restrictions"
- Section 4.5, "Other Input Clocks"



8.3 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-coupled serial link from the dedicated SerDes 2 interface of MPC8544E as shown in Figure 7, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50- Ω output impedance. Each input of the SerDes receiver differential pair features 50- Ω on-die termination to SGND_SRDS2 (xcorevss). The reference circuit of the SerDes transmitter and receiver is shown in Figure 7.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 21.5, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the eTSEC EC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD2_REF_CLK and SD2_REF_CLK pins.

8.3.1 AC Requirements for SGMII SD2_REF_CLK and SD2_REF_CLK

Table 23 lists the SGMII SerDes reference clock AC requirements. Please note that SD2_REF_CLK and SD2_REF_CLK are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Symbol	Parameter Description	Min	Typical	Max	Units	Notes
t _{REF}	REFCLK cycle time	—	10 (8)	_	ns	1
t _{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	_	100	ps	—
t _{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	-50	—	50	ps	—

Table 23. SD2_REF_CLK and SD2_REF_CLK AC Requirements

Note:

1. 8 ns applies only when 125 MHz SerDes2 reference clock frequency is selected via cfg_srds_sgmii_refclk during POR.

8.3.2 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 24 and Table 25 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD2_TX[n] and SD2_TX[n]) as depicted in Figure 8.

Parameter	Symbol	Min	Тур	Мах	Unit	Notes
Supply Voltage	V_{DD_SRDS2}	0.95	1.0	1.05	V	
Output high voltage	V _{OH}	_		V_{OS} -max + $ V_{OD} _{-max}/2$	mV	1
Output low voltage	V _{OL}	V_{OS} -min $- V_{OD} _{-max}/2$		_	mV	I
Output ringing	V _{RING}	—		10	%	_

Table 24. DC Transmitter Electrical Characteristics



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Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
Fall time TX_CLK (80%–20%)	t _{FITF}	_	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid $t_{\ensuremath{\mathsf{FITDV}}}$ to GTX_CLK Min setup time is a function of clock period and max hold time.

(Min setup = Cycle time - Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t _{FIRH} /t _{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t _{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t _{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%-20%)	t _{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.



Figure 12. FIFO Receive AC Timing Diagram



Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 17 provides the AC test load for eTSEC.



Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.



Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



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8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

Table 34. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	_	8.0	_	ns	—
GTX_CLK to TCG[9:0] delay time	t _{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK fall time (80%-20%)	t _{TTXF}	_	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 19 shows the TBI transmit AC timing diagram.



Figure 19. TBI Transmit AC Timing Diagram

8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

Table 35. TBI Receive AC	Timing Specifications
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At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
PMA_RX_CLK[0:1] clock period	t _{TRX}	_	16.0	_	ns	_
PMA_RX_CLK[0:1] skew	t _{SKTRX}	7.5	_	8.5	ns	—

Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).



Table 35. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
PMA_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	_	_	ns	—
PMA_RX_CLK to RCG[9:0] hold time	t _{TRDXKH}	1.5	_	_	ns	—
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t _{TRXR}	0.7	—	2.4	ns	—
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t _{TRXF}	0.7	_	2.4	ns	_

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

Figure 20 shows the TBI receive AC timing diagram.



Figure 20. TBI Receive AC Timing Diagram

8.7.3 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.



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A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

Table 36. TBI Single-Clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{TRR}	7.5	8.0	8.5	ns	—
RX_CLK duty cycle	t _{TRRH}	40	50	60	%	—
RX_CLK peak-to-peak jitter	t _{TRRJ}	—	—	250	ps	—
Rise time RX_CLK (20%-80%)	t _{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t _{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDV}	2.0	—	_	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDX}	1.0	—	—	ns	—

A timing diagram for TBI receive appears in Figure 21.



Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram

8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

Table 37. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGT_TX}	-500	0	500	ps	5
Data to clock input skew (at receiver)	t _{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns	—



Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Fall time (20%–80%)	t _{RGTF}	—		0.75	ns	—

Notes:

- In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{BGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams



8.7.5.2 RMII Receive AC Timing Specifications

Table 39 shows the RMII receive AC timing specifications.

Table 39. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
REF_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMRH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMRJ}	_	_	250	ps	—
Rise time REF_CLK (20%-80%)	t _{RMRR}	1.0		2.0	ns	—
Fall time REF_CLK (80%-20%)	t _{RMRF}	1.0		2.0	ns	—
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	_	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	_	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 24 provides the AC test load for eTSEC.



Figure 24. eTSEC AC Test Load

Figure 25 shows the RMII receive AC timing diagram.



Figure 25. RMII Receive AC Timing Diagram



Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	—	1.6	ns	4
Local bus clock to address valid for LAD, and LALE	t _{LBKLOV3}	—	1.6	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-4.1	—	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-4.1	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	_	1.4	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}	—	1.4	ns	7

Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by tLBKHKT.
- 3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 4. All signals are measured from BV_{DD}/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
- 5. Input timings are measured at the pin.
- 6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.



13.2 I²C AC Electrical Specifications

Table 52 provides the AC timing parameters for the I^2C interfaces.

Table 52. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 51).

Parameter	Symbol ¹	Min	Мах	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μS	—
High period of the SCL clock	t _{I2CH}	0.6	—	μS	—
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	—	μs	—
Data setup time	t _{i2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0		μs	2
Data output delay time	t _{I2OVKL}	—	0.9		3
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μS	_
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b	300	ns	4
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b	300	ns	4
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V	—

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub></sub>
- The MPC8544E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.



Figure 38 provides the AC test load for the I^2C .



Figure 38. I²C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.



Figure 39. I²C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DO	Electrical	Characteristics
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Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = mn$, $I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.



14.2 GPIO AC Electrical Specifications

Table 54 provides the GPIO input and output AC timing specifications.

Table 54. GPIO Input AC Timing Specifications

Parameter	Symbol	Тур	Unit	Notes
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns	1

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 40 provides the AC test load for the GPIO.



15 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8544E.

15.1 PCI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the PCI interface.

Table 55.	PCI DC	Electrical	Characteristics	1
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Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	2
High-level output voltage ($OV_{DD} = min, I_{OH} = -2mA$)	V _{OH}	2.4	_	V	—
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	—

Notes:

1. Ranges listed do not meet the full range of the DC specifications of the PCI 2.2 Local Bus Specifications.

2. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.



High-Speed Serial Interfaces (HSSI)



Figure 48. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 49 through Figure 52 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8544E SerDes reference clock receiver requirement provided in this document.



16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200	_	mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Table 57. SerDes Reference Clock Common AC Parameters

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.



Figure 53. Differential Measurement Points for Rise and Fall Time



Clocking

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio	Binary Value of LA[28:31] Signals	CCB:SYSCLK Ratio
0000	16:1	1000	8:1
0001	Reserved	1001	9:1
0010	Reserved	1010	10:1
0011	3:1	1011	Reserved
0100	4:1	1100	12:1
0101	5:1	1101	Reserved
0110	6:1	1110	Reserved
0111	Reserved	1111	Reserved

Table	65.	ССВ	Clock	Ratio
Table	00.	000	Olock	nauo

19.3 e500 Core PLL Ratio

Table 66 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in Table 66.

Table 6	6. e500	Core to	ССВ	Clock Ratio
	0.0000			

Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	Binary Value of LBCTL, LALE, LGPL2 Signals	e500 core:CCB Clock Ratio	
000	4:1	100	2:1	
001	Reserved	101	5:2	
010	Reserved	110	3:1	
011	3:2	111	7:2	

19.4 PCI Clocks

For specifications on the PCI_CLK, refer to the PCI 2.2 Local Bus Specifications.

The use of PCI_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.



Table 71 provides the thermal resistance with heat sink in open flow.

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield $53 \times 53 \times 25$ mm pin fin	Natural convection	6.1
Wakefield $53 \times 53 \times 25$ mm pin fin	1 m/s	3.0
Aavid $35 \times 31 \times 23$ mm pin fin	Natural convection	8.1
Aavid $35 \times 31 \times 23$ mm pin fin	1 m/s	4.3
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	11.6
Aavid $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.7
Aavid $43 \times 41 \times 16.5$ mm pin fin	Natural convection	8.3
Aavid $43 \times 41 \times 16.5$ mm pin fin	1 m/s	4.3

Table 71. Thermal Resistance with Heat Sink in Open Flow

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block $29 \times 29 \times 1.18$ mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block $29 \times 29 \times 0.58$ mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6×8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC	C8544EThermal	Model
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Conductivity	Value	Units	
Die (7.6 × 8.4 × 0.75mm)			
Silicon	Temperature dependent	_	
Bump/Underfill (7.6 $ imes$ 8.4 $ imes$ 0.070 mm) Collapsed Thermal Resistance			
Kz	6.5	W/m∙K	
Substrate (29 × 29 × 1.18 mm)			
Кх	18	W/m∙K	
Ку	18		
Kz	1.0		



Note the following:

- AV_{DD} SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a $1-\mu F$ ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a $10-\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a $100-\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.



resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 67. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 90°C.

 Table 73. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R _N	43 Target	25 Target	20 Target	Z ₀	W
R _P	43 Target	25 Target	20 Target	Z ₀	W

Note: Nominal supply voltages. See Table 1.

21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has