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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

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Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8544cvtanga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Electrical Characteristics

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV _{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV _{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI and JTAG I/O vol	Express, system control and power management, I ² C, tage	OV _{DD}	3.3 V ± 165 mV	V	3
Local bus I/O volt	age	BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3
Junction tempera	ture range	Τj	0 to 105	°C	—

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. Caution: T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.





Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS postamble	QS postamble t _{DDKHME} 0.4 x tMCK		0.6 x tMCK	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).





Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Fall time (20%–80%)	t _{RGTF}	—		0.75	ns	—

Notes:

- In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{BGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams



8.7.5.2 RMII Receive AC Timing Specifications

Table 39 shows the RMII receive AC timing specifications.

Table 39. RMII Receive AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
REF_CLK clock period	t _{RMR}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMRH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMRJ}	_	_	250	ps	—
Rise time REF_CLK (20%-80%)	t _{RMRR}	1.0	_	2.0	ns	—
Fall time REF_CLK (80%-20%)	t _{RMRF}	1.0	_	2.0	ns	—
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge	t _{RMRDV}	4.0	_	_	ns	—
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge	t _{RMRDX}	2.0	_	_	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 24 provides the AC test load for eTSEC.



Figure 24. eTSEC AC Test Load

Figure 25 shows the RMII receive AC timing diagram.



Figure 25. RMII Receive AC Timing Diagram



Table 46. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.6	ns	5

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table 47	describes the	general timing	parameters of the	local bus inter	face at $BV_{DD} =$	1.8 V DC.
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Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{lbkskew}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{lbotot}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	3.2	ns	_
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	3.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	3.2	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	_	2.6	ns	5

Table 47. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)



Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	—	1.6	ns	4
Local bus clock to address valid for LAD, and LALE	t _{LBKLOV3}	—	1.6	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-4.1	—	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-4.1	—	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	_	1.4	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}	—	1.4	ns	7

Table 48. Local Bus General Timing Parameters—PLL Bypassed (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
 </sub>
- 2. All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by tLBKHKT.
- 3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 4. All signals are measured from BV_{DD}/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
- 5. Input timings are measured at the pin.
- 6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.



Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Мах	Unit	Notes
JTAG external clock to output high impedance:				ns	5
Boundary-scan data	t _{JTKLDZ}	3	19		
TDO	t _{JTKLOZ}	3	9		

Notes:

- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK} .

Figure 34 provides the AC test load for TDO and the boundary-scan outputs.



Figure 34. AC Test Load for the JTAG Interface

Figure 35 provides the JTAG clock input timing diagram.



 $VM = Midpoint Voltage (OV_{DD}/2)$

Figure 35. JTAG Clock Input Timing Diagram

Figure 36 provides the TRST timing diagram.



All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



High-Speed Serial Interfaces (HSSI)



Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are <u>SD1_REF_CLK</u> and <u>SD1_REF_CLK</u> for PCI Express1, PCI Express2. SD2_REF_CLK, and <u>SD2_REF_CLK</u> for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
 - The SDn_REF_CLK and SDn_REF_CLK are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SDn_REF_CLK or SDn_REF_CLK) has a 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.



- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV.
 Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended Mode
 - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with SDn_REF_CLK either left unconnected or tied to ground.
 - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.





High-Speed Serial Interfaces (HSSI)



Figure 48. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 49 through Figure 52 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8544E SerDes reference clock receiver requirement provided in this document.



16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200		mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Table 57. SerDes Reference Clock Common AC Parameters

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.



Figure 53. Differential Measurement Points for Rise and Fall Time



Symbol	Parameter	Min	Nom	Мах	Unit	Comments
V _{TX-RCV-DETECT}	Amount of voltage change allowed during receiver detection	_	_	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.
V _{TX-DC-CM}	TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
I _{TX-SHORT}	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground.
T _{TX-IDLE-MIN}	Minimum time spent in electrical idle	50	_	_	UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
T _{TX-IDLE-SET-TO-IDLE}	Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set	_	_	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
T _{TX} -IDLE-TO-DIFF-DATA	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	_	_	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
RL _{TX-DIFF}	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
RL _{TX-CM}	Common mode return loss	6	_	_	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
Z _{TX-DIFF-DC}	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
Z _{TX-DC}	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC Impedance during all states.
L _{TX-SKEW}	Lane-to-lane output skew		—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link.
C _{TX}	AC coupling capacitor	75	_	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.



Table 60. Differential Receiver	(RX)	Input S	pecifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.





18.3 Pinout Listings

Table 62 provides the pinout listing for the MPC8544E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The DMA_DACK[0:1] and TEST_SEL pins must be set to a proper state during POR configuration. Please refer to Table 62 for more details.

Signal	Package Pin Number	Pin Type	Power Supply	Notes					
PCI									
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV _{DD}						
PCI1_C_BE[3:0]	AC10, AE12, AA14, AD17	I/O	OV _{DD}	—					
PCI1_GNT[4:1]	AE7, AG11,AH11, AC8	0	OV _{DD}	4, 8, 24					
PCI1_GNT0	AE6	I/O	OV _{DD}	—					
PCI1_IRDY	AF13	I/O	OV _{DD}	2					
PCI1_PAR	AB14	I/O	OV _{DD}	—					
PCI1_PERR	AE14	I/O	OV _{DD}	2					
PCI1_SERR	AC14	I/O	OV _{DD}	2					
PCI1_STOP	AA13	I/O	OV _{DD}	2					
PCI1_TRDY	AD13	I/O	OV _{DD}	2					
PCI1_REQ[4:1]	AF9, AG10, AH10, AD6	I	OV _{DD}	—					
PCI1_REQ0	AB8	I/O	OV _{DD}	—					
PCI1_CLK	AH26	I	OV _{DD}	—					
PCI1_DEVSEL	AC13	I/O	OV _{DD}	2					
PCI1_FRAME	AD12	I/O	OV _{DD}	2					
PCI1_IDSEL	AG6	l	OV _{DD}	—					

Table 62. MPC8544E Pinout Listing



Package Description

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes				
Ethernet Management Interface								
EC_MDC	AC7	0	OV _{DD}	4, 8, 14				
EC_MDIO	Y9	I/O	OV _{DD}	—				
Gigabit Reference Clock								
EC_GTX_CLK125	Т2	I	LV _{DD}	—				
Three-Speed Ethernet Controller (Gigabit Ethernet 1)								
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV _{DD}					
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	0	LV _{DD}	4, 8, 14				
TSEC1_COL	R5	I	LV _{DD}	—				
TSEC1_CRS	Τ4	I/O	LV _{DD}	16				
TSEC1_GTX_CLK	Т1	0	LV _{DD}	—				
TSEC1_RX_CLK	V7	I	LV _{DD}	—				
TSEC1_RX_DV	U7	I	LV _{DD}	—				
TSEC1_RX_ER	R9	I	LV _{DD}	4, 8				
TSEC1_TX_CLK	V6	I	LV _{DD}	—				
TSEC1_TX_EN	U4	0	LV _{DD}	22				
TSEC1_TX_ER	ТЗ	0	LV _{DD}					
	Three-Speed Ethernet Controller (Gigab	it Ethernet 3)						
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV _{DD}	—				
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	0	LV _{DD}	4, 8, 14				
TSEC3_COL	M9	I	LV _{DD}	—				
TSEC3_CRS	L9	I/O	LV _{DD}	16				
TSEC3_GTX_CLK	R7	0	LV _{DD}	—				
TSEC3_RX_CLK	Р9	I	LV _{DD}	—				
TSEC3_RX_DV	P8	I	LV _{DD}	—				
TSEC3_RX_ER	R11	I	LV _{DD}	—				
TSEC3_TX_CLK	L10	I	LV _{DD}	—				
TSEC3_TX_EN	N6	0	LV _{DD}	22				
TSEC3_TX_ER	L8	0	LV _{DD}	4, 8				
DUART								
UART_CTS[0:1]	AH8, AF6	I	OV _{DD}	_				
UART_RTS[0:1]	AG8, AG9	0	OV _{DD}	—				





20.3.4 Temperature Diode

The MPC8544E has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461TM). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment. It is recommended that each device be individually calibrated.

The following are voltage forward biased range of the on-board temperature diode:

$$V_{f} > 0.40 V$$

 $V_{f} < 0.90 V$

An approximate value of the ideality may be obtained by calibrating the device near the expected operating temperature. The ideality factor is defined as the deviation from the ideal diode equation:

$$I_{fw} = \mathbf{I}_{\mathbf{s}} \boxed{e^{\frac{qV_f}{nKT}} - 1}$$

Another useful equation is:

$$\mathbf{V}_{\mathrm{H}} - \mathbf{V}_{\mathrm{L}} = \mathbf{n} \frac{\mathrm{KT}}{\mathrm{q}} \left[\mathbf{n} \frac{\mathrm{I}_{\mathrm{H}}}{\mathrm{I}_{\mathrm{L}}} \right]$$



Note the following:

- AV_{DD} SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a $1-\mu F$ ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a $10-\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a $100-\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.



22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

Table 75. Device Nomenclature

MPC	nnnn	Ε	С	НХ	AA	X	В
Product Code	Part Identifier	Encryption Acceleration	Temperature Range	Package ¹	Processor Frequency ²	Platform Frequency	Revision Level
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(-40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:

- 1. See Section 18, "Package Description," for more information on available package types.
- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
- 3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
- 4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.



Notes:

MMMMM is the 5-digit mask number.

ATWLYYWW is the traceability code.

CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device



Document Revision History

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Revision Date Substantive Change(s) 8 09/2015 • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. 7 06/2014 • In Table 75, "Device Nomenclature," added full Pb-free part code. • In Table 75, "Device Nomenclature," added footnotes 3 and 4. 05/2011 6 Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50. 5 01/2011 • Updated Table 75. 4 09/2010 • Modified local bus information in Section 1.1, "Key Features," to show max local bus frequency as 133 MHz. Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61. 11/2009 • Update Section 20.3.4, "Temperature Diode," 3 • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn 2 01/2009 • Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.

• Update paragraph Section 21.3, "Decoupling Recommendations."

• Update Section 22, "Device Nomenclature," with regards to Commercial Tier.

Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed

Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value

• In Table 40, removed note 1 and renumbered remaining note.

Improvement to Section 16, "High-Speed Serial Interfaces (HSSI)

• Update Figure 5 DDR Output Timing Diagram.

Update Figure 59 Mechanical Dimensions

Table 76. MPC8544E Document Revision History

1

0

06/2008

04/2008

Initial release.



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