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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544cvtaqga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- General-purpose chip select machine (GPCM)
- Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Two enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Two IEEE Std 802.3[™], IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, SGMII, and RGMII.
 - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
 - Flexible configuration for multiple PHY interface configurations.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported



Electrical Characteristics

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths.

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	Notes
Local bus interface utilities signals	25 35	BV _{DD} = 3.3 V BV _{DD} = 2.5 V	1
	45 (default) 45 (default) 125	BV _{DD} = 3.3 V BV _{DD} = 2.5 V BV _{DD} = 1.8 V	
PCI signals	25	OV _{DD} = 3.3 V	2
	42 (default)		
DDR signal	20	GV _{DD} = 2.5 V	—
DDR2 signal	16 32 (half strength mode)	GV _{DD} = 1.8 V	—
TSEC signals	42	LV _{DD} = 2.5/3.3 V	—
DUART, system control, JTAG	42	OV _{DD} = 3.3 V	—
l ² C	150	OV _{DD} = 3.3 V	—

Table 3. Output Drive Capability

Notes:

1. The drive strength of the local bus interface is determined by the configuration of the appropriate bits in PORIMPSCR.

2. The drive strength of the PCI interface is determined by the setting of the PCI_GNT1 signal at reset.

2.2 Power Sequencing

The device requires its power rails to be applied in specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

- 1. V_{DD}, AV_{DD}, BV_{DD}, LV_{DD}, SV_{DD}, OV_{DD}, TV_{DD}, XV_{DD}
- 2. GV_{DD}

Note that all supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, then the sequencing for GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.





Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹ Min		Мах	Unit	Notes
MDQS postamble	t _{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).





8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

Table 27. SGMII Receiver AC Timing Specifications

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Deterministic jitter tolerance	J _D	0.37	_	_	UI p-p	1
Combined deterministic and random jitter tolerance	J _{DR}	0.55	_	_	UI p-p	1
Sinusoidal jitter tolerance	Jsin	0.1	_	_	UI p-p	1
Total jitter tolerance	J _T	0.65	_	_	UI p-p	1
Bit error ratio	BER	—	—	10 ⁻¹²	—	_
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C _{TX}	5		200	nF	3

At recommended operating conditions with XVDD_SRDS2 = $1.0 V \pm 5\%$.

Notes:

1. Measured at receiver.

2. Each UI value is 800 ps \pm 100 ppm.

3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.



Figure 9. Receive Input Compliance Mask



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.5.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.5.2.1 GMII Transmit AC Timing Specifications

Table 30 provides the GMII transmit AC timing specifications.

Table 30. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	—	8.0	—	ns	—
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	t _{GTKHDX}	0.2	—	5.0	ns	2
GTX_CLK data clock rise time (20%-80%)	t _{GTXR}	—	—	1.0	ns	—
GTX_CLK data clock fall time (80%-20%)	t _{GTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

2. Data valid t_{GTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).

Figure 13 shows the GMII transmit AC timing diagram.



Figure 13. GMII Transmit AC Timing Diagram



8.5.2.2 GMII Receive AC Timing Specifications

Table 31 provides the GMII receive AC timing specifications.

Table 31. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	_	8.0	_	ns	_
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	35	_	65	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{GRDXKH}	0.5	-	-	ns	—
RX_CLK clock rise (20%–80%)	t _{GRXR}		-	1.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{GRXF}	_	_	1.0	ns	_

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 14 provides the AC test load for eTSEC.



Figure 14. eTSEC AC Test Load

Figure 15 shows the GMII receive AC timing diagram.



Figure 15. GMII Receive AC Timing Diagram

8.6 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.



Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 17 provides the AC test load for eTSEC.



Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.



Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
- 3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
- 4. t_{plb clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.



Figure 26. MII Management Interface Timing Diagram



Local Bus

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8544E.

10.1 Local Bus DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 3.3 \text{ V DC}$.

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	BV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current (BV _{IN} = 0 V or BV _{IN} = BOV _{DD})	I _{IN}	—	±5	μA	1
High-level output voltage ($BV_{DD} = min$, $I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage ($BV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	—

Table 42. Local Bus DC Electrical Characteristics (3.3 V DC)

Note:

1. The symbol $\mathsf{BV}_{\mathsf{IN}}$ in this case, represents the $\mathsf{BV}_{\mathsf{IN}}$ symbol referenced in Table 1 and Table 2.

Table 43 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 2.5 \text{ V DC}$.

Table 43. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	1.70	BV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.7	V	—
Input current ($BV_{IN} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	—	±15	μA	1
High-level output voltage ($BV_{DD} = min, I_{OH} = -1 mA$)	V _{OH}	2.0	—	V	—
Low-level output voltage ($BV_{DD} = min, I_{OL} = 1 mA$)	V _{OL}	—	0.4	V	—

Note:

1. The symbol BV_{IN} , in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 44 provides the DC electrical characteristics for the local bus interface operating at $BV_{DD} = 1.8 \text{ V DC}$.

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	1.3	BV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.6	V	—
Input current ($BV_{IN} = 0 V \text{ or } BV_{IN} = BV_{DD}$)	I _{IN}	—	±15	μA	1



Figure 28 through Figure 33 show the local bus signals.



Table 48 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	_
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	1.2	4.9	ns	_
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	7.4	_	ns	4, 5
LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.75	_	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	-0.2	_	ns	4, 5
LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-0.2	_	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	—	1.6	ns	_

Table 48. Local Bus General Timing Parameters—PLL Bypassed







Figure 31. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Bypass Mode)



Local Bus



Figure 32. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	5
Boundary-scan data	t _{JTKLDZ}	3	19		
TDO	t _{JTKLOZ}	3	9		

Notes:

- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK} .

Figure 34 provides the AC test load for TDO and the boundary-scan outputs.



Figure 34. AC Test Load for the JTAG Interface

Figure 35 provides the JTAG clock input timing diagram.



 $VM = Midpoint Voltage (OV_{DD}/2)$

Figure 35. JTAG Clock Input Timing Diagram

Figure 36 provides the TRST timing diagram.



All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.



Figure 37 provides the boundary-scan timing diagram.



Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Input high voltage level	V _{IH}	$0.7\times \text{OV}_{\text{DD}}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	3
Capacitance for each I/O pin	CI	_	10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. Refer to the MPC8544EPowerQUICC III Integrated Communications Host Processor Reference Manual for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\text{DD}}}$ is switched off.



Figure 38 provides the AC test load for the I^2C .



Figure 38. I²C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.



Figure 39. I²C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DO	Electrical	Characteristics
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Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = mn$, $I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.



High-Speed Serial Interfaces (HSSI)

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, VOD (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, VDIFFp

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, V_{DIFFp-p}

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n_TX}$, for example) from the non-inverting signal ($\overline{\text{SD}n_TX}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 44 as an example for differential waveform.

7. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SDn_TX} + V_{\overline{SDn_TX}} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasions.



Table 71 provides the thermal resistance with heat sink in open flow.

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield $53 \times 53 \times 25$ mm pin fin	Natural convection	6.1
Wakefield $53 \times 53 \times 25$ mm pin fin	1 m/s	3.0
Aavid $35 \times 31 \times 23$ mm pin fin	Natural convection	8.1
Aavid $35 \times 31 \times 23$ mm pin fin	1 m/s	4.3
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	11.6
Aavid $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.7
Aavid $43 \times 41 \times 16.5$ mm pin fin	Natural convection	8.3
Aavid $43 \times 41 \times 16.5$ mm pin fin	1 m/s	4.3

Table 71. Thermal Resistance with Heat Sink in Open Flow

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block $29 \times 29 \times 1.18$ mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block $29 \times 29 \times 0.58$ mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6×8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC	C8544EThermal	Model
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Conductivity	Conductivity Value			
	Die (7.6 × 8.4 × 0.75mm)			
Silicon	Silicon Temperature dependent			
Bump/U	Bump/Underfill (7.6 \times 8.4 \times 0.070 mm) Collapsed Thermal Resistance			
Kz 6.5		W/m∙K		
Substrate (29 × 29 × 1.18 mm)				
Кх	18 W/m•K			
Ку	18			
Kz	1.0			



System Design Information

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power ArchitectureTM technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.



21.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0-kΩ isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 69. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Figure 68 shows the COP connector physical pinout.



Figure 68. COP Connector Physical Pinout



Device Nomenclature

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Table 74. Commercial and Industrial Description

Note:

1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.