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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
PowerPC e500
1 Core, 32-Bit
667MHz
Signal Processing; SPE
DDR, DDR2, SDRAM
No
-
10/100/1000Mbps (2)
-
-
1.8V, 2.5V, 3.3V
0°C ~ 105°C (TA)
-
783-BBGA, FCBGA
783-FCPBGA (29x29)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544dvtalfa

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Input Clocks

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 \text{ V} \pm 165 \text{ mV}$.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t _{SYSCLK}	7.5	—	30.3	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t _{KHK} ∕t _{SYSCLK}	40	—	60	%	_
SYSCLK jitter	_	—	—	±150	ps	3, 4

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

3. This represents the total input jitter-short- and long-term.

4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.



DDR and DDR2 SDRAM

Table 16 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 V$.

Table 16. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V	—

Table 17 provides the input AC timing specifications for the DDR SDRAM interface.

Table 17. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller skew for MDQS—MDQ/MECC/MDM	t _{CISKEW}			ps	1, 2
533 MHz		-300	300		3
400 MHz		-365	365		—
333 MHz		-390	390		_

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

- 2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW} . This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW} . See Figure 3.
- 3. Maximum DDR1 frequency is 400 MHz.

Figure 3 shows the DDR SDRAM input timing diagram.



Figure 3. DDR SDRAM Input Timing Diagram (t_{DISKEW})





Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS postamble	t _{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).







Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.



Figure 8 shows an SGMII transmitter DC measurement circuit.



Figure 8. SGMII Transmitter DC Measurement Circuit

Table 25 shows the DC receiver electrical characteristics.

Table 25. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Supply Voltage	V _{DD_SRDS2}	0.9	1.0	1.05	V	_
DC input voltage range	—		_	_	—	1



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Table 28. FIFO Mode Transmit AC Timing Specification (continued)

(continued)At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
Fall time TX_CLK (80%–20%)	t _{FITF}	_	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	—	3.0	ns	1

Note:

1. Data valid $t_{\ensuremath{\mathsf{FITDV}}}$ to GTX_CLK Min setup time is a function of clock period and max hold time.

(Min setup = Cycle time - Max hold).

Table 29. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{FIR}	—	8.0	—	ns	—
RX_CLK duty cycle	t _{FIRH} /t _{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t _{FIRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t _{FIRR}	—	—	0.75	ns	—
Fall time RX_CLK (80%-20%)	t _{FIRF}	—	—	0.75	ns	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 11 and Figure 12.



Figure 12. FIFO Receive AC Timing Diagram



Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 17 provides the AC test load for eTSEC.



Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.



Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



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A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

Table 36. TBI Single-Clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Тур	Мах	Unit	Notes
RX_CLK clock period	t _{TRR}	7.5	8.0	8.5	ns	—
RX_CLK duty cycle	t _{TRRH}	40	50	60	%	—
RX_CLK peak-to-peak jitter	t _{TRRJ}	—	—	250	ps	—
Rise time RX_CLK (20%-80%)	t _{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t _{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t _{TRRDV}	2.0	—	_	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t _{TRRDX}	1.0	—	—	ns	—

A timing diagram for TBI receive appears in Figure 21.



Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram

8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

Table 37. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
Data to clock output skew (at transmitter)	t _{SKRGT_TX}	-500	0	500	ps	5
Data to clock input skew (at receiver)	t _{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t _{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t _{RGTH} /t _{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns	—



Table 41. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC fall time	t _{MDHF}	_	_	10	ns	

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
- 3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
- 4. t_{plb clk} is the platform (CCB) clock.

Figure 26 shows the MII management AC timing diagram.



Figure 26. MII Management Interface Timing Diagram



Figure 28 through Figure 33 show the local bus signals.



Table 48 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	_
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	1.2	4.9	ns	_
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	7.4	_	ns	4, 5
LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.75	_	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	-0.2	_	ns	4, 5
LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-0.2	_	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	—	1.6	ns	_

Table 48. Local Bus General Timing Parameters—PLL Bypassed



13.2 I²C AC Electrical Specifications

Table 52 provides the AC timing parameters for the I^2C interfaces.

Table 52. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 51).

Parameter	Symbol ¹	Min	Мах	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	—
Low period of the SCL clock	t _{I2CL}	1.3	—	μS	—
High period of the SCL clock	t _{I2CH}	0.6	—	μS	_
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{i2SXKL}	0.6		μs	—
Data setup time	t _{i2DVKH}	100	—	ns	—
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0		μs	2
Data output delay time	t _{I2OVKL}	—	0.9		3
Set-up time for STOP condition	t _{I2PVKH}	0.6	—	μS	_
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b	300	ns	4
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b	300	ns	4
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V	—

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub></sub>
- The MPC8544E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.

1²C

Figure 42 shows the PCI input AC timing conditions.



Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.



Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{SDn}_T\overline{X}$) or a receiver input (SD*n*_RX and $\overline{SDn}_R\overline{X}$). Each signal swings between A Volts and B Volts where A > B.



High-Speed Serial Interfaces (HSSI)



Figure 44. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and TD, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are <u>SD1_REF_CLK</u> and <u>SD1_REF_CLK</u> for PCI Express1, PCI Express2. SD2_REF_CLK, and <u>SD2_REF_CLK</u> for the PCI Express3 or SGMII interface, respectively. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 45 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for $XV_{DD SRDS2}$ are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
 - The SDn_REF_CLK and SDn_REF_CLK are internally AC-coupled differential inputs as shown in Figure 45. Each differential clock input (SDn_REF_CLK or SDn_REF_CLK) has a 50-Ω termination to SGND_SRDSn (xcorevss) followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.



High-Speed Serial Interfaces (HSSI)



Figure 48. Single-Ended Reference Clock Input DC Requirements

16.2.3 Interfacing With Other Differential Signaling Levels

With on-chip termination to SGND_SRDS*n* (xcorevss), the differential reference clocks inputs are HCSL (high-speed current steering logic) compatible DC-coupled.

Many other low voltage differential type outputs like LVDS (low voltage differential signaling) can be used but may need to be AC-coupled due to the limited common mode input range allowed (100 to 400 mV) for DC-coupled connection.

LVPECL outputs can produce signal with too large amplitude and may need to be DC-biased at clock driver output first, then followed with series attenuation resistor to reduce the amplitude, in addition to AC-coupling.

NOTE

Figure 49 through Figure 52 are for conceptual reference only. Due to the fact that clock driver chip's internal structure, output impedance and termination requirements are different between various clock driver chip manufacturers, it is very possible that the clock circuit reference designs provided by clock driver chip vendor are different from what is shown below. They might also vary from one vendor to the other. Therefore, Freescale Semiconductor can neither provide the optimal clock driver reference circuits, nor guarantee the correctness of the following clock driver connection reference circuits. The system designer is recommended to contact the selected clock driver chip vendor for the optimal reference circuits with the MPC8544E SerDes reference clock receiver requirement provided in this document.



16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200		mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Table 57. SerDes Reference Clock Common AC Parameters

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.



Figure 53. Differential Measurement Points for Rise and Fall Time



Table 60. Differential Receiver	(RX)	Input S	pecifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in Table 61.

Parameter	PBGA ¹
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Table 61. Package Parameters

Note:

1. (FC-PBGA) without a lid.



Package Description

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
Ethernet Management Interface							
EC_MDC	AC7	0	OV _{DD}	4, 8, 14			
EC_MDIO	Y9	I/O	OV _{DD}	—			
	Gigabit Reference Clock	•					
EC_GTX_CLK125	Т2	I	LV _{DD}	—			
	Three-Speed Ethernet Controller (Gigab	it Ethernet 1)					
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV _{DD}	—			
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	0	LV _{DD}	4, 8, 14			
TSEC1_COL	R5	I	LV _{DD}	—			
TSEC1_CRS	Τ4	I/O	LV _{DD}	16			
TSEC1_GTX_CLK	Т1	0	LV _{DD}	—			
TSEC1_RX_CLK	V7	I	LV _{DD}	—			
TSEC1_RX_DV	U7	I	LV _{DD}	—			
TSEC1_RX_ER	R9	I	LV _{DD}	4, 8			
TSEC1_TX_CLK	V6	I	LV _{DD}	—			
TSEC1_TX_EN	U4	0	LV _{DD}	22			
TSEC1_TX_ER	ТЗ	0	LV _{DD}	—			
	Three-Speed Ethernet Controller (Gigab	it Ethernet 3)		·			
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV _{DD}	—			
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	0	LV _{DD}	4, 8, 14			
TSEC3_COL	M9	I	LV _{DD}	—			
TSEC3_CRS	L9	I/O	LV _{DD}	16			
TSEC3_GTX_CLK	R7	0	LV _{DD}	—			
TSEC3_RX_CLK	Р9	I	LV _{DD}	—			
TSEC3_RX_DV	P8	I	LV _{DD}	—			
TSEC3_RX_ER	R11	I	LV _{DD}	—			
TSEC3_TX_CLK	L10	I	LV _{DD}	—			
TSEC3_TX_EN	N6	0	LV _{DD}	22			
TSEC3_TX_ER	L8	0	LV _{DD}	4, 8			
	DUART						
UART_CTS[0:1]	AH8, AF6	I	OV _{DD}	_			
UART_RTS[0:1]	AG8, AG9	0	OV _{DD}	—			



System Design Information

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power ArchitectureTM technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.



21.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0-kΩ isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 69. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Figure 68 shows the COP connector physical pinout.



Figure 68. COP Connector Physical Pinout



Device Nomenclature

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-k Ω resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-k Ω resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-k Ω resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-k Ω resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8544E device has been tested to meet the industrial tier qualification. Table 74 provides a description for commercial and industrial qualifications.

Tier ¹	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Table 74. Commercial and Industrial Description

Note:

1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.