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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544dvtang

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



MPC8544E Overview

- Two key (K1, K2, K1) or three key (K1, K2, K3)
- ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
 - Implements the Rijndael symmetric key cipher
 - ECB, CBC, CTR, and CCM modes
 - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
 - Implements a stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
- MDEU—message digest execution unit
 - SHA with 160- or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
- KEU-Kasumi execution unit
 - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
 - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications
- Dual I²C controllers
 - Two-wire interface
 - Multiple master support
 - Master or slave I²C mode support
 - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
 - Optionally loads configuration data from serial ROM at reset via the I²C interface
 - Can be used to initialize configuration registers and/or memory
 - Supports extended I^2C addressing mode
 - Data integrity checked with preamble signature and CRC
- DUART
 - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
 - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data bus operating at up to 133 MHz
 - Eight chip selects support eight external slaves
 - Up to eight-beat burst transfers
 - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
 - Two protocol engines available on a per chip select basis:



Figure 1 shows the MPC8544E block diagram.



Figure 1. MPC8544E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8544E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 **Overall DC Electrical Characteristics**

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

able 1. Absolute	Maximum	Ratings ¹
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Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V _{DD}	-0.3 to 1.1	V	—
PLL supply voltage	AV _{DD}	–0.3 to 1.1	V	_
Core power supply for SerDes transceivers	SV _{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV _{DD}	-0.3 to 1.1	V	_



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Parameter		Symbol	Min	Тур	Max	Unit	Notes
Input differential voltage	LSTS = 0	V _{rx_diffpp}	100	—	1200	mV	2, 4
	LSTS = 1	1	175	—			
Loss of signal threshold	LSTS = 0	VI _{os}	30	—	100	mV	3, 4
	LSTS = 1	1	65	—	175		
Input AC common mode voltage		V _{cm_acpp}	—	—	100	mV	5.
Receiver differential input impedar	ice	Zrx_diff	80	—	120	Ω	
Receiver common mode input impedance		Zrx_cm	20	—	35	Ω	—
Common mode input voltage		Vcm	xcorevss	—	xcorevss	V	6

Table 25. DC Receiver Electrical Characteristics (continued)

Notes:

1. Input must be externally AC-coupled.

- 2. $V_{RX_DIFFp-p}$ is also referred to as peak-to-peak input differential voltage
- 3. The concept of this parameter is equivalent to the electrical idle detect threshold parameter in PCI Express. Refer to Section 17.4.3, "Differential Receiver (RX) Input Specifications," for further explanation.
- 4. The LSTS shown in this table refers to the LSTSCD bit field of MPC8544E SerDes 2 control register 1.
- 5. V_{CM ACp-p} is also referred to as peak-to-peak AC common mode voltage.
- 6. On-chip termination to SGND_SRDS2 (xcorevss).

8.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs ($SD2_TX[n]$ and $\overline{SD2_TX[n]}$) or at the receiver inputs ($SD2_RX[n]$ and $\overline{SD2_RX[n]}$) as depicted in Figure 10, respectively.

8.4.1 SGMII Transmit AC Timing Specifications

Table 26 provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 26. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XVDD_SRDS2 = $1.0 V \pm 5\%$.

Parameter	Symbol	Min	Тур	Мах	Unit	Notes
Deterministic jitter	J _D	—	—	0.17	UI p-p	—
Total jitter	J _T	—	—	0.35	UI p-p	—
Unit interval	UI	799.92	800	800.08	ps	2
V _{OD} fall time (80%–20%)	t _{fall}	50	—	120	ps	—
V _{OD} rise time (20%–80%)	t _{rise}	50	—	120	ps	—

Notes;

1. Source synchronous clock is not supported.

2. Each UI value is 800 ps \pm 100 ppm.



8.4.2 SGMII Receive AC Timing Specifications

Table 27 provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 9 shows the SGMII receiver input compliance mask eye diagram.

Table 27. SGMII Receiver AC Timing Specifications

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Deterministic jitter tolerance	J _D	0.37	_	_	UI p-p	1
Combined deterministic and random jitter tolerance	J _{DR}	0.55	_	_	UI p-p	1
Sinusoidal jitter tolerance	Jsin	0.1	_	_	UI p-p	1
Total jitter tolerance	J _T	0.65	_	_	UI p-p	1
Bit error ratio	BER	—	—	10 ⁻¹²	—	_
Unit interval	UI	799.92	800	800.08	ps	2
AC coupling capacitor	C _{TX}	5		200	nF	3

At recommended operating conditions with XVDD_SRDS2 = $1.0 V \pm 5\%$.

Notes:

1. Measured at receiver.

2. Each UI value is 800 ps \pm 100 ppm.

3. The external AC coupling capacitor is required. It's recommended to be placed near the device transmitter outputs.



Figure 9. Receive Input Compliance Mask



Table 37. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
Fall time (20%–80%)	t _{RGTF}	—		0.75	ns	—

Notes:

- In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
- 2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
- 3. For 10 and 100 Mbps, t_{BGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
- 4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
- 5. Guaranteed by design.

Figure 22 shows the RGMII and RTBI AC timing and multiplexing diagrams.



Figure 22. RGMII and RTBI AC Timing and Multiplexing Diagrams



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.7.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.7.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 38.

Table 38. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
REF_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMTJ}	_	_	250	ps	—
Rise time REF_CLK (20%–80%)	t _{RMTR}	1.0	_	2.0	ns	—
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns	—

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 23 shows the RMII transmit AC timing diagram.



Figure 23. RMII Transmit AC Timing Diagram



Figure 28 through Figure 33 show the local bus signals.



Table 48 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus cycle time	t _{LBK}	12	_	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	_
Internal launch/capture clock to LCLK delay	t _{LBKHKT}	1.2	4.9	ns	_
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	7.4	_	ns	4, 5
LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.75	_	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	-0.2	_	ns	4, 5
LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-0.2	_	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	—	1.6	ns	_

Table 48. Local Bus General Timing Parameters—PLL Bypassed



Figure 38 provides the AC test load for the I^2C .



Figure 38. I²C AC Test Load

Figure 39 shows the AC timing diagram for the I^2C bus.



Figure 39. I²C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8544E.

14.1 GPIO DC Electrical Characteristics

Table 53 provides the DC electrical characteristics for the GPIO interface.

Table 53. GPIO DO	Electrical	Characteristics
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Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	—
Low-level input voltage	V _{IL}	-0.3	0.8	V	—
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = mn, I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	—
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

Figure 42 shows the PCI input AC timing conditions.



Figure 42. PCI Input AC Timing Measurement Conditions

Figure 43 shows the PCI output AC timing conditions.



Figure 43. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8544E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications. The SerDes1 dedicated for PCI Express data transfers. The SerDes2 can be used for PCI Express and/or SGMII application. This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 44 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{SDn}_T\overline{X}$) or a receiver input (SD*n*_RX and $\overline{SDn}_R\overline{X}$). Each signal swings between A Volts and B Volts where A > B.



Table 59. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
T _{crosslink}	Crosslink random timeout	0		1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 58 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 56.)
- 3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
- 4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 58.) Note that the series capacitors C_{TX} is optional for the return loss measurement.
- 5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 58 for both V_{TX-D+} and V_{TX-D-} .
- 6. See Section 4.3.1.8 of the PCI Express Base Specifications, Rev 1.0a.
- 7. See Section 4.2.6.3 of the PCI Express Base Specifications, Rev 1.0a.

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 56 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).



PCI Express

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.



Figure 57. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 58.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary.



Figure 58. Compliance Test/Measurement Load





18.3 Pinout Listings

Table 62 provides the pinout listing for the MPC8544E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The DMA_DACK[0:1] and TEST_SEL pins must be set to a proper state during POR configuration. Please refer to Table 62 for more details.

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	PCI			
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV _{DD}	
PCI1_C_BE[3:0]	AC10, AE12, AA14, AD17	I/O	OV _{DD}	—
PCI1_GNT[4:1]	AE7, AG11,AH11, AC8	0	OV _{DD}	4, 8, 24
PCI1_GNT0	AE6	I/O	OV _{DD}	—
PCI1_IRDY	AF13	I/O	OV _{DD}	2
PCI1_PAR	AB14	I/O	OV _{DD}	—
PCI1_PERR	AE14	I/O	OV _{DD}	2
PCI1_SERR	AC14	I/O	OV _{DD}	2
PCI1_STOP	AA13	I/O	OV _{DD}	2
PCI1_TRDY	AD13	I/O	OV _{DD}	2
PCI1_REQ[4:1]	AF9, AG10, AH10, AD6	I	OV _{DD}	—
PCI1_REQ0	AB8	I/O	OV _{DD}	—
PCI1_CLK	AH26	I	OV _{DD}	—
PCI1_DEVSEL	AC13	I/O	OV _{DD}	2
PCI1_FRAME	AD12	I/O	OV _{DD}	2
PCI1_IDSEL	AG6	l	OV _{DD}	—

Table 62. MPC8544E Pinout Listing



Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
DDR SDRAM Memory Interface							
MDQ[0:63]	A26, B26, C22, D21, D25, B25, D22, E21, A24, A23, B20, A20, A25, B24, B21, A21, E19, D19, E16, C16, F19, F18, F17, D16, B18, A18, A15, B14, B19, A19, A16, B15, D1, F3, G1, H2, E4, G5, H3, J4, B2, C3, F2, G2, A2, B3, E1, F1, L5, L4,N3, P3, J3, K4, N4, P4, J1, K1, P1, R1, J2, K2, N1, R2	I/O	GV _{DD}	_			
MECC[0:7]	G12, D14, F11, C11, G14, F14,C13, D12	I/O	GV _{DD}	—			
MDM[0:8]	C25, B23, D18, B17, G4, C2, L3, L2, F13	0	GV _{DD}	21			
MDQS[0:8]	D24, B22, C18, A17, J5, C1, M4, M2, E13	I/O	GV _{DD}	—			
MDQS[0:8]	C23, A22, E17, B16, K5, D2, M3, P2, D13	I/O	GV _{DD}	_			
MA[0:15]	B7, G8, C8, A10, D9, C10, A11, F9, E9, B12, A5, A12, D11, F7, E10, F10	0	GV _{DD}	_			
MBA[0:2]	A4, B5, B13	0	GV _{DD}	_			
MWE	B4	0	GV _{DD}	—			
MCAS	E7	0	GV _{DD}	—			
MRAS	C5	0	GV _{DD}	_			
MCKE[0:3]	H10, K10, G10, H9	0	GV _{DD}	10			
MCS[0:3]	D3, H6, C4, G6	0	GV _{DD}	—			
MCK[0:5]	A9, J11, J6, A8, J13, H8	0	GV _{DD}	_			
MCK[0:5]	B9, H11, K6, B8, H13, J8	0	GV _{DD}	_			
MODT[0:3]	E5, H7, E6, F6	0	GV _{DD}	—			
MDIC[0:1]	H15, K15	I/O	GV _{DD}	25			
TEST_IN	A13	I	—	27			
TEST_OUT	A6	0	—	17			
	Local Bus Controller Interfac	e	I				
LAD[0:31]	K22, L21, L22, K23, K24, L24, L25, K25, L28, L27, K28, K27, J28, H28, H27, G27, G26, F28, F26, F25, E28, E27, E26, F24, E24, C26, G24, E23, G23, F22, G22, G21	I/O	BV _{DD}	23			
LDP[0:3]	K26, G28, B27, E25	I/O	BV _{DD}				
LA[27]	L19	0	BV _{DD}	4, 8			
LA[28:31]	K16, K17, H17,G17	0	BV _{DD}	4, 6, 8			
LCS[0:4]	K18, G19, H19, H20, G16	0	BV _{DD}	—			
LCS5/DMA_DREQ2	H16	I/O	BV _{DD}	1			

Table 62. MPC8544E Pinout Listing (continued)



Package Description

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type Power Supply		Notes
SD2_REF_CLK	AF2	I	xv _{DD}	—
SD2_TST_CLK	AG4	_	—	—
SD2_TST_CLK	AF4	_	—	—
	General-Purpose Output			
GPOUT[0:7]	AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26	0	OV _{DD}	_
	General-Purpose Input			•
GPIN[0:7]	AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20	I	OV _{DD}	_
	System Control		I	
HRESET	AG16	I	OV _{DD}	—
HRESET_REQ	AG15	0	OV _{DD}	21
SRESET	AG19	I	OV _{DD}	—
CKSTP_IN	AH5	I	OV _{DD}	—
CKSTP_OUT	AA12	0	OV _{DD}	2, 4
	Debug			
TRIG_IN	AC5	I	OV _{DD}	—
TRIG_OUT/READY/ QUIESCE	AB5	0	OV _{DD}	5, 8, 15, 21
MSRCID[0:1]	Y7, W9	0	OV _{DD}	4, 5, 8
MSRCID[2:4]	AA9, AB6, AD5	0	OV _{DD}	5, 15, 21
MDVAL	Y8	0	OV _{DD}	5
CLK_OUT	AE16	0	OV _{DD}	10
	Clock			
RTC	AF15	I	OV _{DD}	—
SYSCLK	AH16	-	OV _{DD}	—
	JTAG			
тск	AG28	-	OV _{DD}	—
TDI	AH28	-	OV _{DD}	11
TDO	AF28	0	OV _{DD}	10
TMS	AH27	I	OV _{DD}	11
TRST	AH22	I	OV _{DD}	11



Table 71 provides the thermal resistance with heat sink in open flow.

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield $53 \times 53 \times 25$ mm pin fin	Natural convection	6.1
Wakefield $53 \times 53 \times 25$ mm pin fin	1 m/s	3.0
Aavid $35 \times 31 \times 23$ mm pin fin	Natural convection	8.1
Aavid $35 \times 31 \times 23$ mm pin fin	1 m/s	4.3
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	11.6
Aavid $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.7
Aavid $43 \times 41 \times 16.5$ mm pin fin	Natural convection	8.3
Aavid $43 \times 41 \times 16.5$ mm pin fin	1 m/s	4.3

Table 71. Thermal Resistance with Heat Sink in Open Flow

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block $29 \times 29 \times 1.18$ mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block $29 \times 29 \times 0.58$ mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6×8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC	C8544EThermal	Model
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Conductivity	Value	Units		
	Die (7.6 × 8.4 × 0.75mm)			
Silicon	Temperature dependent	_		
Bump/Underfill (7.6 $ imes$ 8.4 $ imes$ 0.070 mm) Collapsed Thermal Resistance				
Kz	6.5	W/m∙K		
Substrate (29 × 29 × 1.18 mm)				
Кх	18	W/m∙K		
Ку	18			
Kz	1.0			



Thermal

Conductivity	Value	Units
	Solder and Air (29 \times 29 \times 0.58 mm)	
Кх	0.034	W/m∙K
Ку	0.034	
Kz	12.1	





Figure 60. System Level Thermal Model for MPC8544E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.



20.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8544E implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 20.3.4, "Temperature Diode," for more information.

The recommended attachment method to the heat sink is illustrated in Figure 61. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).



Figure 61. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

Aavid Thermalloy603-224-9988 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com Advanced Thermal Solutions781-769-2800 89 Access Road #27. Norwood, MA02062 Internet: www.qats.com Alpha Novatech408-567-8082

473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com



Note the following:

- AV_{DD} SRDS should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.

21.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8544E system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These decoupling capacitors should receive their power from separate V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} ; and GND power planes in the PCB, utilizing short low impedance traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD} , TV_{DD} , BV_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 μ F (AVX TPS tantalum or Sanyo OSCON). However, customers should work directly with their power regulator vendor for best values and types and quantity of bulk capacitors.

21.4 SerDes Block Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

Only surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.

- First, the board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias, these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.
- Second, there should be a $1-\mu F$ ceramic chip capacitor on each side of the device. This should be done for all SerDes supplies.
- Third, between the device and any SerDes voltage regulator there should be a $10-\mu$ F, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a $100-\mu$ F, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.



resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 67. Driver Impedance Measurement

Table 73 summarizes the signal impedance targets. The driver impedances are targeted at minimum V_{DD} , nominal OV_{DD} , 90°C.

 Table 73. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI	DDR DRAM	Symbol	Unit
R _N	43 Target	25 Target	20 Target	Z ₀	W
R _P	43 Target	25 Target	20 Target	Z ₀	W

Note: Nominal supply voltages. See Table 1.

21.8 Configuration Pin Muxing

The MPC8544E provides the user with power-on configuration options which can be set through the use of external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{HRESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Most of these sampled configuration pins are equipped with an on-chip gated resistor of approximately 20 kΩ. This value should permit the 4.7-kΩ resistor to pull the configuration pin to a valid logic low level. The pull-up resistor is enabled only during $\overline{\text{HRESET}}$ (and for platform /system clocks after $\overline{\text{HRESET}}$ deassertion to ensure capture of the reset value). When the input receiver is disabled the pull-up is also, thus allowing functional operation of the pin as an output with minimal signal quality or delay disruption. The default value for all configuration bits treated this way has



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been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power ArchitectureTM technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.