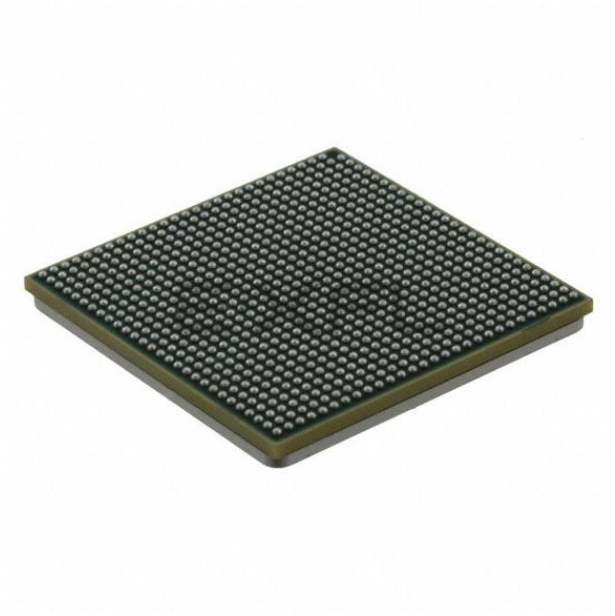

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544eavtalfa

  - Broadcast address (accept/reject)
  - Hash table match on up to 512 multicast addresses
  - Promiscuous mode
- Buffer descriptors backward compatible with MPC8260 and MPC860T 10/100 Ethernet programming models
- RMON statistics support
- 10-Kbyte internal transmit and 2-Kbyte receive FIFOs
- MII management interface for control and status
- Ability to force allocation of header information and buffer descriptors into L2 cache

- OCeaN switch fabric
  - Full crossbar packet switch
  - Reorders packets from a source based on priorities
  - Reorders packets to bypass blocked packets
  - Implements starvation avoidance algorithms
  - Supports packets with payloads of up to 256 bytes
- Integrated DMA controller
  - Four-channel controller
  - All channels accessible by both the local and remote masters
  - Extended DMA functions (advanced chaining and striding capability)
  - Support for scatter and gather transfers
  - Misaligned transfer capability
  - Interrupt on completed segment, link, list, and error
  - Supports transfers to or from any local memory or I/O port
  - Selectable hardware-enforced coherency (snoop/no snoop)
  - Ability to start and flow control each DMA channel from external 3-pin interface
  - Ability to launch DMA from single write transaction
- PCI controller
  - PCI 2.2 compatible
  - One 32-bit PCI port with support for speeds from 16 to 66 MHz
  - Host and agent mode support
  - 64-bit dual address cycle (DAC) support
  - Supports PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses
  - Supports posting of processor-to-PCI and PCI-to-memory writes
  - PCI 3.3-V compatible
  - Selectable hardware-enforced coherency

Figure 1 shows the MPC8544E block diagram.

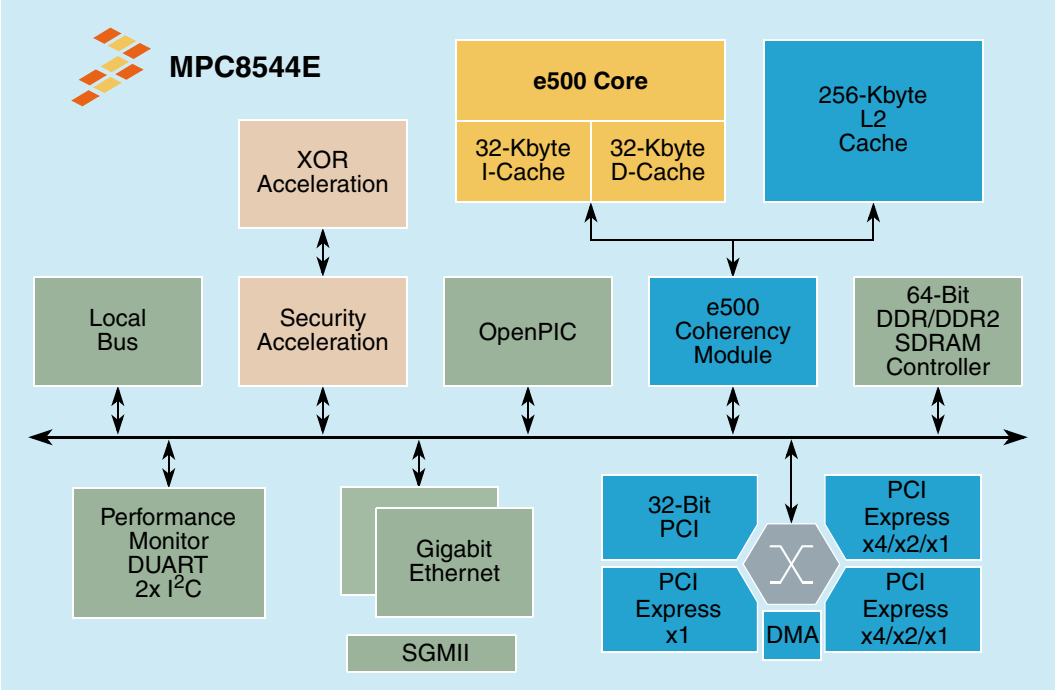


Figure 1. MPC8544E Block Diagram

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8544E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

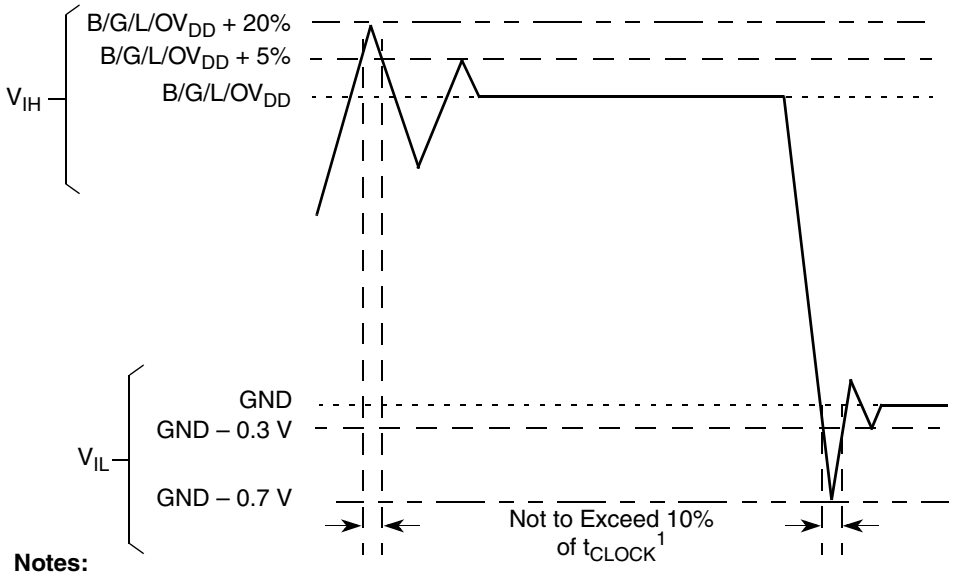
2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Characteristic	Symbol	Max Value	Unit	Notes
Core supply voltage	V_{DD}	–0.3 to 1.1	V	—
PLL supply voltage	AV_{DD}	–0.3 to 1.1	V	—
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.1	V	—

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8544E.



Notes:
1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in Section 4.2.2.3 of the *PCI 2.2 Local Bus Specifications*.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time, MCK[n]/$\overline{\text{MCK}}$[n] crossing	t_{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		
333 MHz		2.40	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
533 MHz		1.48	—		7
400 MHz		1.95	—		—
333 MHz		2.40	—		—
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
533 MHz		538	—		7
400 MHz		700	—		—
333 MHz		900	—		—
MDQS preamble	t_{DDKHMP}	0.75 x tMCK	—	ns	6

Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Max	Unit	Notes
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:
1. CCB clock refers to the platform clock.
2. Actual attainable baud rate will be limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—SGMII/GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial gigabit media independent interface (SGMII), media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The SGMII interfaces follow the *Serial Gigabit Media-Independent Interface (SGMII) Specification Version 1.8*. The electrical characteristics for MDIO and MDC are specified in Section 9, “Ethernet Management Interface Electrical

Figure 10 provides the AC test load for SGMII.

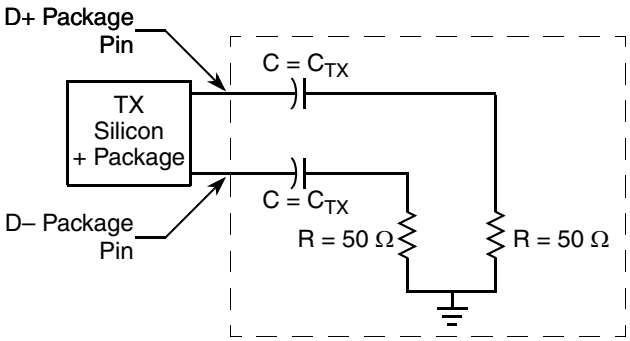


Figure 10. SGMII AC Test/Measurement Load

8.5 FIFO, GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.5.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n* TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in Table 28 and Table 29.

Table 28. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—

8.6.1 MII Transmit AC Timing Specifications

Table 32 provides the MII transmit AC timing specifications.

Table 32. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 16 shows the MII transmit AC timing diagram.

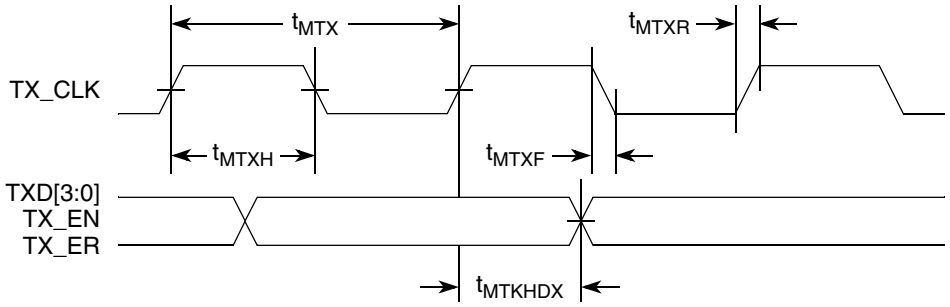


Figure 16. MII Transmit AC Timing Diagram

8.6.2 MII Receive AC Timing Specifications

Table 33 provides the MII receive AC timing specifications.

Table 33. MII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	—
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	—
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—

A summary of the single-clock TBI mode AC specifications for receive appears in Table 36.

Table 36. TBI Single-Clock Mode Receive AC Timing Specification

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
RX_CLK clock period	t_{TRR}	7.5	8.0	8.5	ns	—
RX_CLK duty cycle	t_{TRRH}	40	50	60	%	—
RX_CLK peak-to-peak jitter	t_{TRRJ}	—	—	250	ps	—
Rise time RX_CLK (20%–80%)	t_{TRRR}	—	—	1.0	ns	—
Fall time RX_CLK (80%–20%)	t_{TRRF}	—	—	1.0	ns	—
RCG[9:0] setup time to RX_CLK rising edge	t_{TRRDV}	2.0	—	—	ns	—
RCG[9:0] hold time to RX_CLK rising edge	t_{TRRDX}	1.0	—	—	ns	—

A timing diagram for TBI receive appears in Figure 21.

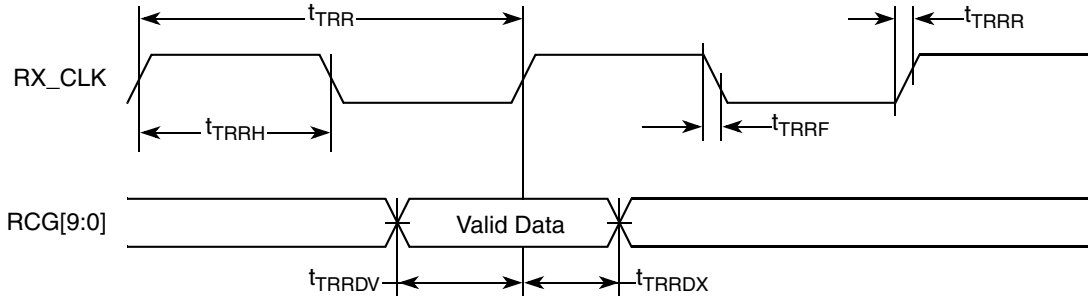


Figure 21. TBI Single-Clock Mode Receive AC Timing Diagram

8.7.4 RGMII and RTBI AC Timing Specifications

Table 37 presents the RGMII and RTBI AC timing specifications.

Table 37. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.8	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.45	V	—

10.2 Local Bus AC Electrical Specifications

Table 45 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 19.1, "Clock Ranges."

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.85	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.9	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.7	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.7	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5

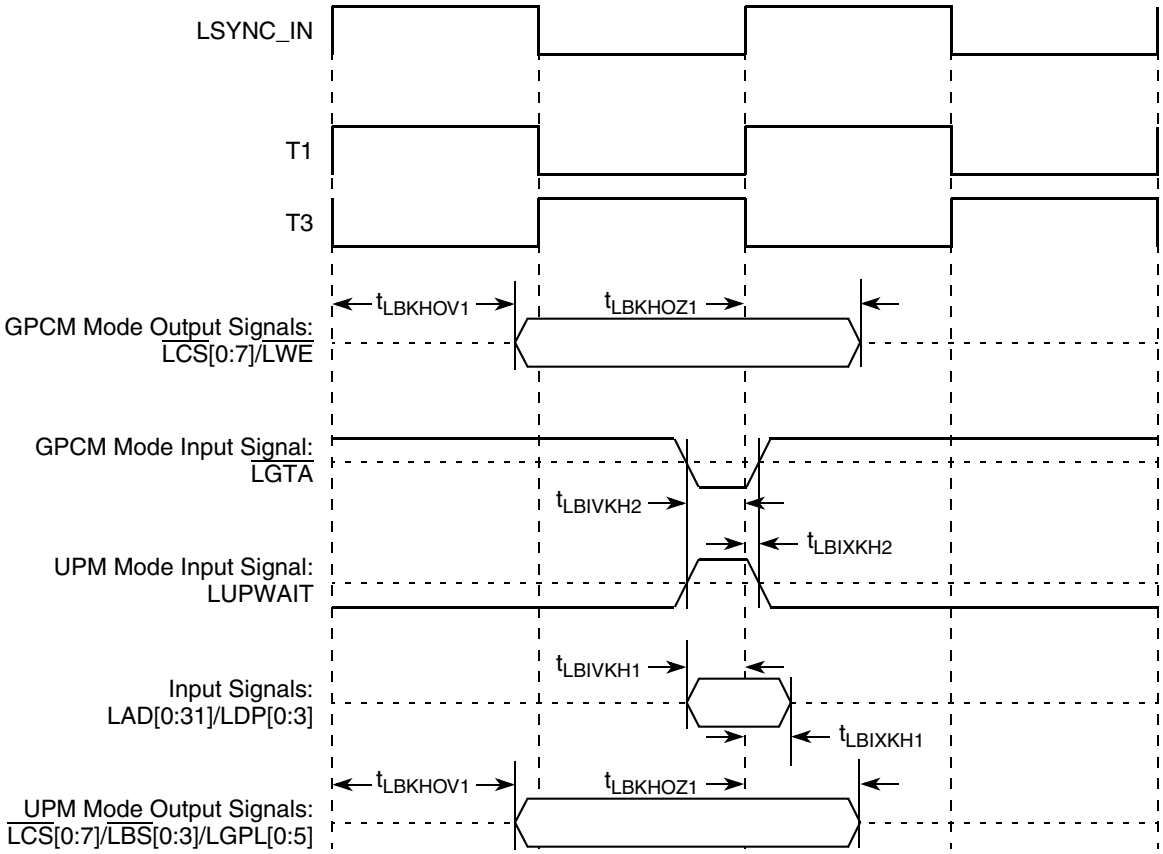


Figure 30. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)

Figure 37 provides the boundary-scan timing diagram.

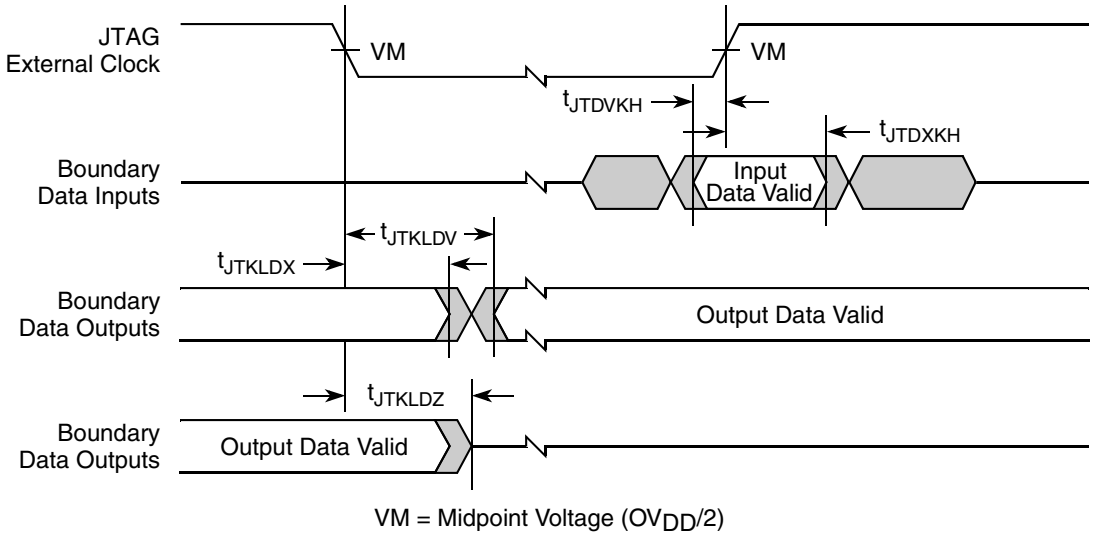


Figure 37. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8544E.

13.1 I²C DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the I²C interfaces.

Table 51. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8544EPowerQUICC III Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

14.2 GPIO AC Electrical Specifications

Table 54 provides the GPIO input and output AC timing specifications.

Table 54. GPIO Input AC Timing Specifications

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 40 provides the AC test load for the GPIO.

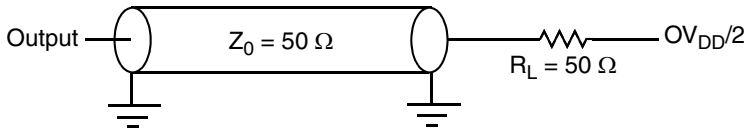


Figure 40. GPIO AC Test Load

15 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8544E.

15.1 PCI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the PCI interface.

Table 55. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Table 56. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	7.4	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0.5	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$[9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Fall time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, “Clocking.”
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.

Figure 41 provides the AC test load for PCI.

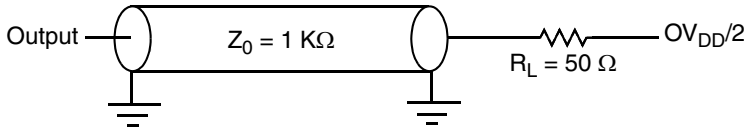


Figure 41. PCI AC Test Load

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

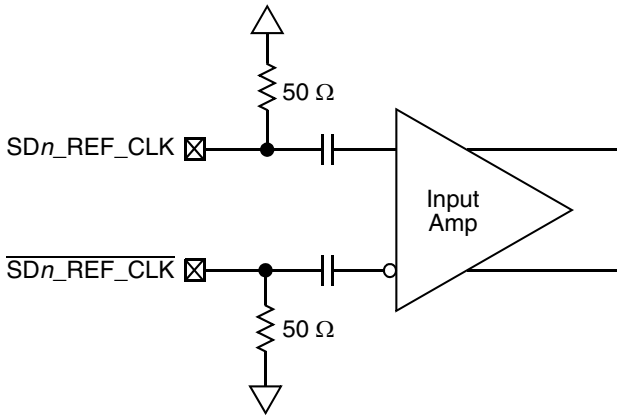


Figure 45. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8544E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in Table 61.

Table 61. Package Parameters

Parameter	PBGA[1]
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Note:
1. (FC-PBGA) without a lid.

19.5 Security Controller PLL Ratio

Table 67 shows the SEC frequency ratio.

Table 67. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1[1]
	1	3:1[2]

Notes:
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

19.6.1 SYSCLK to Platform Frequency Options

Table 68 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 68. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
2							—
3					—	333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500			
8		333	533				
9		375					
10	333	417					
12	400	500					
16	533						

been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 69. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

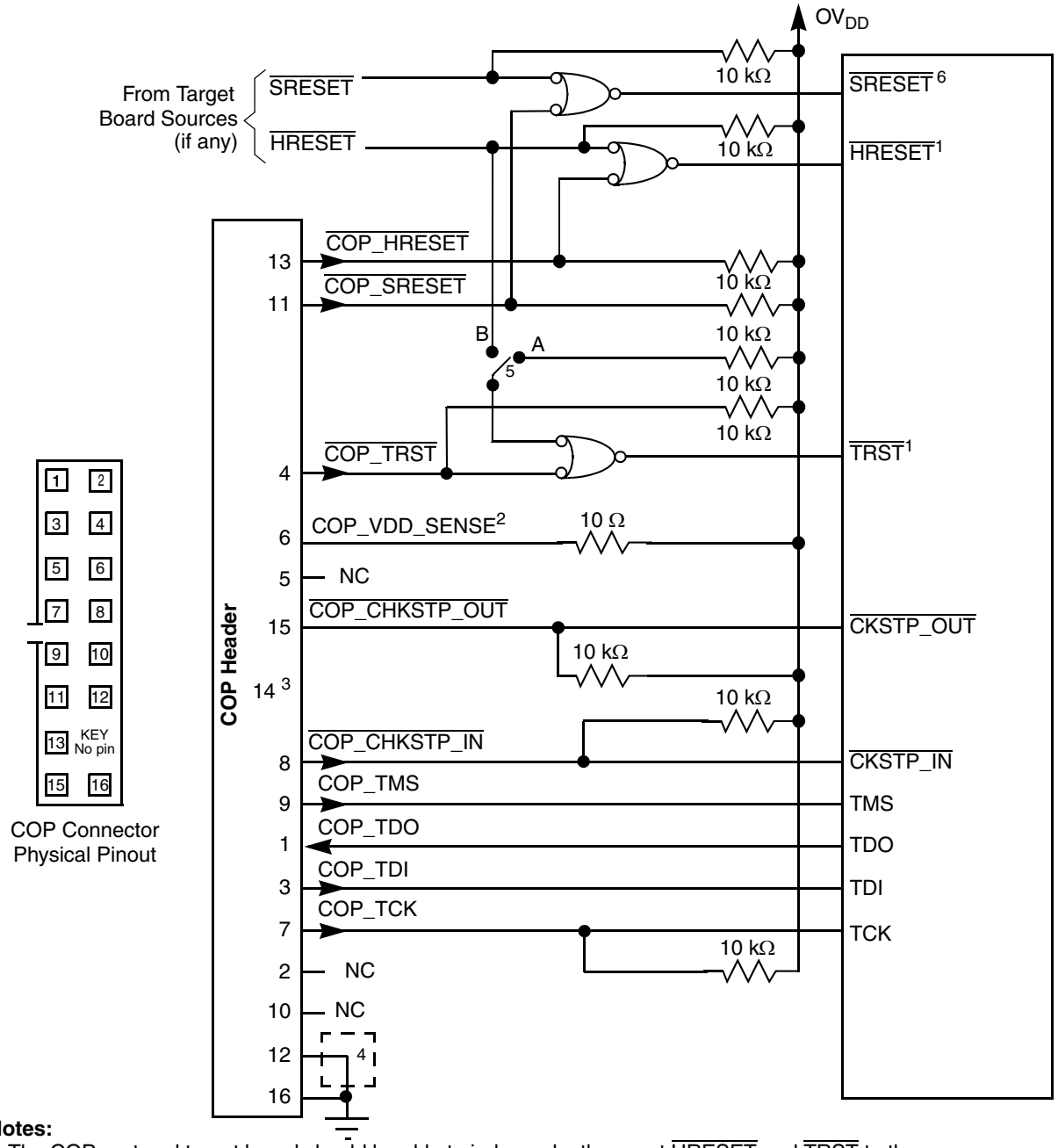
The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 69 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 68, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 68 is common to all known emulators.

Figure 69 shows the JTAG interface connection.



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 69. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Table 76. MPC8544E Document Revision History

Revision	Date	Substantive Change(s)
8	09/2015	• In Table 10 and Table 12, removed the output leakage current rows and removed table note 4.
7	06/2014	• In Table 75, “Device Nomenclature,” added full Pb-free part code. • In Table 75, “Device Nomenclature,” added footnotes 3 and 4.
6	05/2011	• Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50.
5	01/2011	• Updated Table 75.
4	09/2010	• Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz. • Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61.
3	11/2009	• Update Section 20.3.4, “Temperature Diode,” • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn
2	01/2009	• Update power number table to include 1067 MHz/533 MHz power numbers. • Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. • Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle. • Update paragraph Section 21.3, “Decoupling Recommendations.” • Update Figure 5 DDR Output Timing Diagram. • In Table 40, removed note 1 and renumbered remaining note. • Update Section 22, “Device Nomenclature,” with regards to Commercial Tier.
1	06/2008	Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value Improvement to Section 16, “High-Speed Serial Interfaces (HSSI) Update Figure 59 Mechanical Dimensions Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed
0	04/2008	Initial release.