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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544eavtang

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Input Clocks

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8544E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with $OV_{DD} = 3.3 V \pm 165 mV$.

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
SYSCLK frequency	f _{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t _{SYSCLK}	7.5	—	30.3	ns	_
SYSCLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t _{KHK} ∕t _{SYSCLK}	40	—	60	%	_
SYSCLK jitter	_	—	—	±150	ps	3, 4

Notes:

1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.

2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.

3. This represents the total input jitter-short- and long-term.

4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8544E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8544E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Мах	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:

1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.



DDR and DDR2 SDRAM

6.2.2 DDR SDRAM Output AC Timing Specifications

Table 18 provides the output AC timing specifications for the DDR SDRAM interface.

Table 18. DDR SDRAM Output AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MCK[n] cycle time, MCK[n]/MCK[n] crossing	t _{MCK}	3.75	6	ns	2
ADDR/CMD output setup with respect to MCK	t _{DDKHAS}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
ADDR/CMD output hold with respect to MCK	t _{DDKHAX}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCS[n] output setup with respect to MCK	t _{DDKHCS}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCS[n] output hold with respect to MCK	t _{DDKHCX}			ns	3
533 MHz 400 MHz 333 MHz		1.48 1.95 2.40			7
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	^t DDKHDS, t _{DDKLDS}			ps	5
533 MHz 400 MHz 333 MHz		538 700 900			7
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
533 MHz 400 MHz 333 MHz		538 700 900			7 — —
MDQS preamble	t _{DDKHMP}	0.75 x tMCK	—	ns	6





Table 18. DDR SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
MDQS postamble	t _{DDKHME}	0.4 x tMCK	0.6 x tMCK	ns	6

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
 </sub>
- 2. All MCK/ \overline{MCK} referenced measurements are made from the crossing of the two signals ±0.1 V.
- 3. ADDR/CMD includes all DDR SDRAM output signals except MCK/MCK, MCS, and MDQ/MECC/MDM/MDQS.
- 4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the MPC8544E PowerQUICC III Integrated Communications Processor Reference Manual, for a description and understanding of the timing modifications enabled by use of these bits.
- 5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
- 6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.
- 7. Maximum DDR1 frequency is 400 MHz.

NOTE

For the ADDR/CMD setup and hold specifications in Table 18, it is assumed that the clock control register is set to adjust the memory clocks by $\frac{1}{2}$ applied cycle.

Figure 4 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).





Enhanced Three-Speed Ethernet (eTSEC), MII Management

Characteristics."

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.135	3.465	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OH} = -4.0 mA$)	V _{OH}	2.4	_	V	—
Output low voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OL} = 4.0 mA$)	V _{OL}	—	0.5	V	—
Input high voltage	V _{IH}	1.95	—	V	—
Input low voltage	V _{IL}	—	0.90	V	—
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IH}	—	40	μA	1, 2, 3
Input low current (V _{IN} = GND)	I _{IL}	-600	_	μA	3

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Notes:

1. LV_{DD} supports eTSEC1.

2. TV_{DD} supports eTSEC3.

3. The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. 0	GMIL MIL	. RMII. RGMI	I. RTBI. TBI	and FIFO DC	Electrical	Characteristics
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Parameters	Symbol	Min	Мах	Unit	Notes
Supply voltage 2.5 V	LV _{DD} /TV _{DD}	2.375	2.625	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OH} = -1.0 mA$)	V _{OH}	2.0	—	V	—
Output low voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OL} = 1.0 mA$)	V _{OL}	_	0.4	V	—
Input high voltage	V _{IH}	1.70	—	V	—
Input low voltage	V _{IL}	_	0.7	V	—
Input current ($V_{IN} = 0$, $V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IN}	_	±15	μA	1, 2, 3

Notes:

1. LV_{DD} supports eTSEC1.

2. TV_{DD} supports eTSEC3.

3. The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.





Figure 7 shows an example of a 4-wire AC-coupled SGMII serial link connection.



Figure 8 shows an SGMII transmitter DC measurement circuit.



Figure 8. SGMII Transmitter DC Measurement Circuit

Table 25 shows the DC receiver electrical characteristics.

Table 25. DC Receiver Electrical Characteristics

Parameter	Symbol	Min	Тур	Max	Unit	Notes
Supply Voltage	V _{DD_SRDS2}	0.9	1.0	1.05	V	_
DC input voltage range	—			_	—	1



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.7.1 TBI Transmit AC Timing Specifications

Table 34 provides the TBI transmit AC timing specifications.

Table 34. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	_	8.0	_	ns	—
GTX_CLK to TCG[9:0] delay time	t _{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t _{TTXR}	_	—	1.0	ns	—
GTX_CLK fall time (80%-20%)	t _{TTXF}	_	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 19 shows the TBI transmit AC timing diagram.



Figure 19. TBI Transmit AC Timing Diagram

8.7.2 TBI Receive AC Timing Specifications

Table 35 provides the TBI receive AC timing specifications.

Table 35. TBI Receive AC	Timing Specifications
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At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
PMA_RX_CLK[0:1] clock period	t _{TRX}	_	16.0	_	ns	_
PMA_RX_CLK[0:1] skew	t _{SKTRX}	7.5	_	8.5	ns	—

Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).



Table 35. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
PMA_RX_CLK[0:1] duty cycle	t _{TRXH} /t _{TRX}	40	—	60	%	—
RCG[9:0] setup time to rising PMA_RX_CLK	t _{TRDVKH}	2.5	—	_	ns	—
PMA_RX_CLK to RCG[9:0] hold time	t _{TRDXKH}	1.5	—	_	ns	—
PMA_RX_CLK[0:1] clock rise time (20%-80%)	t _{TRXR}	0.7	—	2.4	ns	—
PMA_RX_CLK[0:1] clock fall time (80%-20%)	t _{TRXF}	0.7	—	2.4	ns	_

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

Figure 20 shows the TBI receive AC timing diagram.



Figure 20. TBI Receive AC Timing Diagram

8.7.3 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC n_RX_CLK pin (no receive clock is used on TSEC n_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.7.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.7.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 38.

Table 38. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
REF_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMTJ}	_	_	250	ps	—
Rise time REF_CLK (20%–80%)	t _{RMTR}	1.0	_	2.0	ns	—
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns	—

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 23 shows the RMII transmit AC timing diagram.



Figure 23. RMII Transmit AC Timing Diagram



Parameter	Symbol	Min	Мах	Unit	Notes
High-level output voltage (BV _{DD} = min, I _{OH} = -2 mA)	V _{OH}	1.35	_	V	
Low-level output voltage (BV _{DD} = min, I _{OL} = 2 mA)	V _{OL}		0.45	V	

Table 44. Local Bus DC Electrical Characteristics (1.8 V DC) (continued)

10.2 Local Bus AC Electrical Specifications

Table 45 describes the general timing parameters of the local bus interface at $BV_{DD} = 3.3$ V. For information about the frequency range of local bus see Section 19.1, "Clock Ranges."

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7, 8
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.85	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.9	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.8	ns	—
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.7	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.7	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{lbkhox2}	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	_	2.5	ns	5

Table 45. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled



High-Speed Serial Interfaces (HSSI)

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, VOD (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, VDIFFp

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, V_{DIFFp-p}

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n_TX}$, for example) from the non-inverting signal ($\overline{\text{SD}n_TX}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 44 as an example for differential waveform.

7. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SDn_TX} + V_{\overline{SDn_TX}} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasions.



- For external DC-coupled connection, as described in Section 16.2.1, "SerDes Reference Clock Receiver Characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) to be between 100 and 400 mV.
 Figure 46 shows the SerDes reference clock input requirement for DC-coupled connection scheme.
- For external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Since the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND_SRDSn. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage (SGND_SRDSn). Figure 47 shows the SerDes reference clock input requirement for AC-coupled connection scheme.
- Single-ended Mode
 - The reference clock can also be single-ended. The SDn_REF_CLK input amplitude (single-ended swing) must be between 400 and 800 mV peak-peak (from Vmin to Vmax) with SDn_REF_CLK either left unconnected or tied to ground.
 - The SDn_REF_CLK input average voltage must be between 200 and 400 mV. Figure 48 shows the SerDes reference clock input requirement for single-ended signaling mode.
 - To meet the input amplitude requirement, the reference clock inputs might need to be DC or AC-coupled externally. For the best noise performance, the reference of the clock could be DC or AC-coupled into the unused phase (SDn_REF_CLK) through the same source impedance as the clock input (SDn_REF_CLK) in use.





16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 57 describes some AC parameters common to SGMII, and PCI Express protocols.

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V _{IH}	+200		mV	2
Differential Input Low Voltage	V _{IL}	_	-200	mV	2
Rising edge rate (SD <i>n</i> _REF_CLK) to falling edge rate (SD <i>n</i> _REF_CLK) matching	Rise-Fall Matching	_	20	%	1, 4

Table 57. SerDes Reference Clock Common AC Parameters

Notes:

- 1. Measurement taken from single ended waveform.
- 2. Measurement taken from differential waveform.
- 3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus SD*n*_REF_CLK). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 53.
- 4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for SDn_REF_CLK. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets SDn_REF_CLK falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SDn_REF_CLK should be compared to the fall edge rate of SDn_REF_CLK, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 54.



Figure 53. Differential Measurement Points for Rise and Fall Time



Table 60. Differential Receiver	(RX)	Input S	pecifications	(continued)
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Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 58 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 57). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 58). Note that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 57 is specified using the passive compliance/test measurement load (see Figure 58) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 58) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 57) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



Package Description

18.2 Mechanical Dimensions of the MPC8544E FC-PBGA

Figure 59 shows the mechanical dimensions and bottom surface nomenclature of the MPC8544E, 783 FC-PBGA package without a lid.



Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
- 7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 59. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8544E FC-PBGA without a Lid



Table 62. MPC8544E Pinout Listing (continued	Table 62	. MPC8544E	Pinout	Listing	(continued
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Signal	Package Pin Number	Pin Type	Power Supply	Notes				
UART_SIN[0:1]	AG7, AH6	I	OV _{DD}					
UART_SOUT[0:1]	AH7, AF7	0	OV _{DD}					
	I ² C interface							
IIC1_SCL	AG21	I/O	OV _{DD}	20				
IIC1_SDA	AH21	I/O	OV _{DD}	20				
IIC2_SCL	AG13	I/O	OV _{DD}	20				
IIC2_SDA	AG14	I/O	OV _{DD}	20				
	SerDes 1							
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV _{DD}	_				
SD1_RX[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV _{DD}					
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	0	XV _{DD}					
SD1_TX[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	0	XV _{DD}					
SD1_PLL_TPD	V28	0	XV _{DD}	17				
SD1_REF_CLK	U28	I	XV _{DD}	_				
SD1_REF_CLK	U27	I	XV _{DD}	_				
SD1_TST_CLK	T22		—	—				
SD1_TST_CLK	Т23		—	—				
	SerDes 2							
SD2_RX[0]	AD25	I	xv _{DD}	—				
SD2_RX[2]	AD1	I	XV _{DD}	26				
SD2_RX[3]	AB2	I	XV _{DD}	26				
SD2_RX[0]	AD26	I	XV _{DD}	—				
SD2_RX[2]	AC1	I	XV _{DD}	26				
SD2_RX[3]	AA2	I	XV _{DD}	26				
SD2_TX[0]	AA21	0	XV _{DD}	—				
SD2_TX[2]	AC4	0	xv _{DD}	26				
SD2_TX[3]	AA5	0	XV _{DD}	26				
SD2_TX[0]	AA20	0	XV _{DD}	—				
SD2_TX[2]	AB4	0	XV _{DD}	26				
SD2_TX[3]	Y5	0	XV _{DD}	26				
SD2_PLL_TPD	AG3	0	XV _{DD}	17				
SD2_REF_CLK	AE2	I	XV _{DD}	—				



Package Description

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes			
SD2_REF_CLK	AF2	I	xv _{DD}	—			
SD2_TST_CLK	AG4	_	—	—			
SD2_TST_CLK	AF4	_	—	—			
	General-Purpose Output						
GPOUT[0:7]	AF22, AH23, AG27, AH25, AF21, AF25, AG26, AF26	0	OV _{DD}	_			
	General-Purpose Input			•			
GPIN[0:7]	AH24, AG24, AD23, AE21, AD22, AF23, AG25, AE20	I	OV _{DD}	_			
	System Control		I				
HRESET	AG16	I	OV _{DD}	—			
HRESET_REQ	AG15	0	OV _{DD}	21			
SRESET	AG19	I	OV _{DD}	—			
CKSTP_IN	AH5	I	OV _{DD}	—			
CKSTP_OUT	AA12	0	OV _{DD}	2, 4			
	Debug						
TRIG_IN	AC5	I	OV _{DD}	—			
TRIG_OUT/READY/ QUIESCE	AB5	0	OV _{DD}	5, 8, 15, 21			
MSRCID[0:1]	Y7, W9	0	OV _{DD}	4, 5, 8			
MSRCID[2:4]	AA9, AB6, AD5	0	OV _{DD}	5, 15, 21			
MDVAL	Y8	0	OV _{DD}	5			
CLK_OUT	AE16	0	OV _{DD}	10			
Clock							
RTC	AF15	I	OV _{DD}	—			
SYSCLK	AH16		OV _{DD}	—			
JTAG							
тск	AG28		OV _{DD}	—			
TDI	AH28		OV _{DD}	11			
TDO	AF28	0	OV _{DD}	10			
TMS	AH27	I	OV _{DD}	11			
TRST	AH22	I	OV _{DD}	11			



Package Description

Table 62. MPC8544E Pinout Listing (continued)

		(,		
Signal	Package Pin Number	Pin Type	Power Supply	Notes
6.The value of LA[28:31] du resistors. See Section 1	ring reset sets the CCB clock to SYSCLK PLL ration 9.2. "CCB/SYSCLK PLL Ratio."	o. These pins requ	ire 4.7-k Ω pull-up (or pull-down

- 7.The value of LALE, LGPL2, and LBCTL at reset set the e500 core clock to CCB clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors. See Section 19.3, "e500 Core PLL Ratio."
- 8. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan.
- 9. For proper state of these signals during reset, DMA_DACK[1] must be pulled down to GND through a resistor. DMA_DACK[0] can be pulled up or left without a resistor. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed on DMA_DACK[0].
- 10. This output is actively driven during reset rather than being three-stated during reset.
- 11. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
- 12. These pins are connected to the V_{DD}/GND planes internally and may be used by the core power supply to improve tracking and regulation.
- 13. Anode and cathode of internal thermal diode.
- 14.Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.
- 15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.
- 16. This pin is only an output in FIFO mode when used as Rx flow control.

17.Do not connect.

18. These are test signals for factory use only and must be pulled up (100 Ω to 1 k Ω) to OV_{DD} for normal machine operation.

- 19.Independent supplies derived from board $\ensuremath{\mathsf{V}_{\text{DD}}}$.
- 20.Recommend a pull-up resistor (1 K~) be placed on this pin to OV_{DD} .
- 21. The following pins must not be pulled down during power-on reset: HRESET_REQ, TRIG_OUT/READY/QUIESCE, MSRCID[2:4], and ASLEEP.
- 22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.
- 23.General-purpose POR configuration of user system.
- 24.When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
- 25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
- 26.For SGMII mode.

27.Connect to GND.

28. For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.



Thermal

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.



Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com Dow-Corning Corporation800-248-2481 Corporate Center P.O.Box 999 Midland, MI 48686-0997 Internet: www.dow.com Shin-Etsu MicroSi, Inc.888-642-7674 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com The Bergquist Company800-347-4572 18930 West 78th St.



21.9.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- TRST should be tied to HRESET through a 0-kΩ isolation resistor so that it is asserted when the system reset signal (HRESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 69. If this is not possible, the isolation resistor will allow future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

Figure 68 shows the COP connector physical pinout.



Figure 68. COP Connector Physical Pinout



Document Revision History

23 Document Revision History

This table provides a revision history for the MPC8544E hardware specification.

Revision Date Substantive Change(s) 8 09/2015 • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. 7 06/2014 • In Table 75, "Device Nomenclature," added full Pb-free part code. • In Table 75, "Device Nomenclature," added footnotes 3 and 4. 05/2011 6 Updated the value of t_{JTKLDX} to 2.5 ns from 4ns in Table 50. 5 01/2011 • Updated Table 75. 4 09/2010 • Modified local bus information in Section 1.1, "Key Features," to show max local bus frequency as 133 MHz. Added footnote 28 to Table 62. • Updated solder-ball parameter in Table 61. 11/2009 • Update Section 20.3.4, "Temperature Diode," 3 • Update Table 61 Package Parameters from 95.5%sn to 96.5%sn 2 01/2009 • Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide application note. • Update t_{DDKHMP}, t_{DDKHME} in Table 18. • Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.

• Update paragraph Section 21.3, "Decoupling Recommendations."

• Update Section 22, "Device Nomenclature," with regards to Commercial Tier.

Update in Table 48 Local Bus General Timing Parameters—PLL Bypassed

Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value

• In Table 40, removed note 1 and renumbered remaining note.

Improvement to Section 16, "High-Speed Serial Interfaces (HSSI)

• Update Figure 5 DDR Output Timing Diagram.

Update Figure 59 Mechanical Dimensions

Table 76. MPC8544E Document Revision History

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06/2008

04/2008

Initial release.