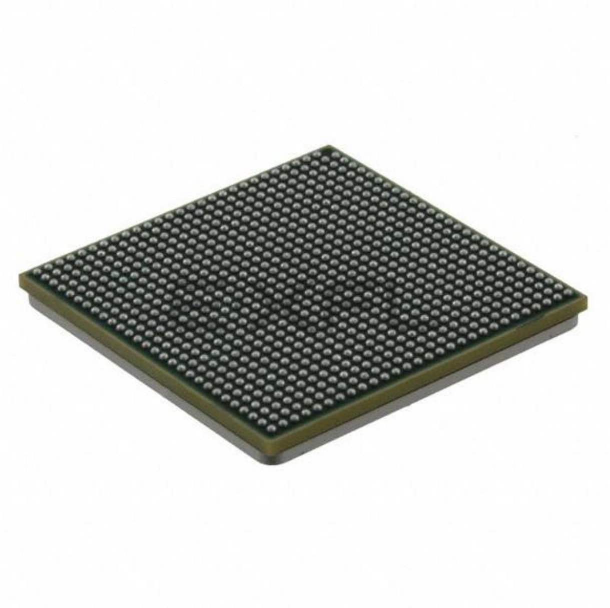

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Understanding Embedded - Microprocessors

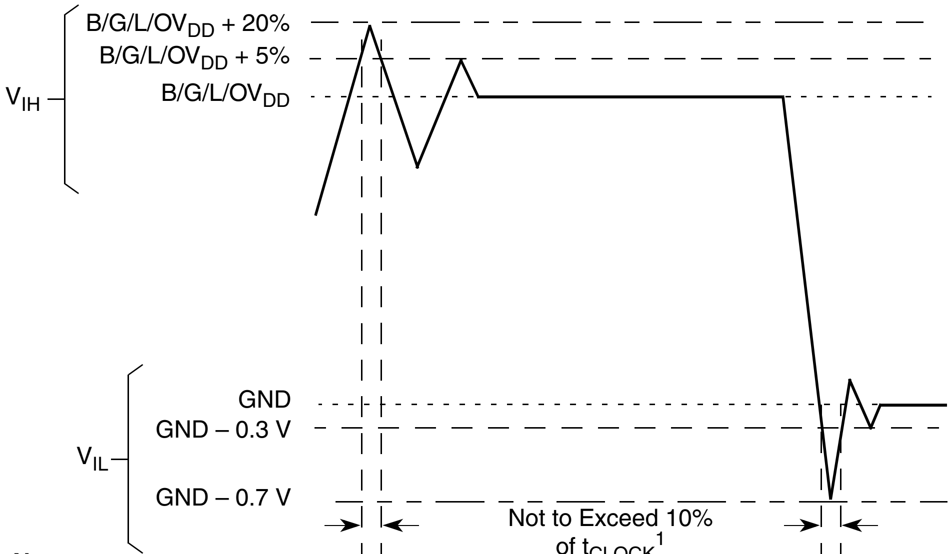
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e500
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Signal Processing; SPE, Security; SEC
RAM Controllers	DDR, DDR2, SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8544eavtanga

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8544E.



Notes:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^{2}C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in Section 4.2.2.3 of the *PCI 2.2 Local Bus Specifications*.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

Table 16 provides the input AC timing specifications for the DDR SDRAM when GV_{DD}(typ) = 2.5 V.

Table 16. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V_{IL}	—	MV_{REF} – 0.31	V	—
AC input high voltage	V_{IH}	MV_{REF} + 0.31	—	V	—

Table 17 provides the input AC timing specifications for the DDR SDRAM interface.

Table 17. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Controller skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
533 MHz		–300	300		3
400 MHz		–365	365		—
333 MHz		–390	390		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$, where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}. See Figure 3.
3. Maximum DDR1 frequency is 400 MHz.

Figure 3 shows the DDR SDRAM input timing diagram.

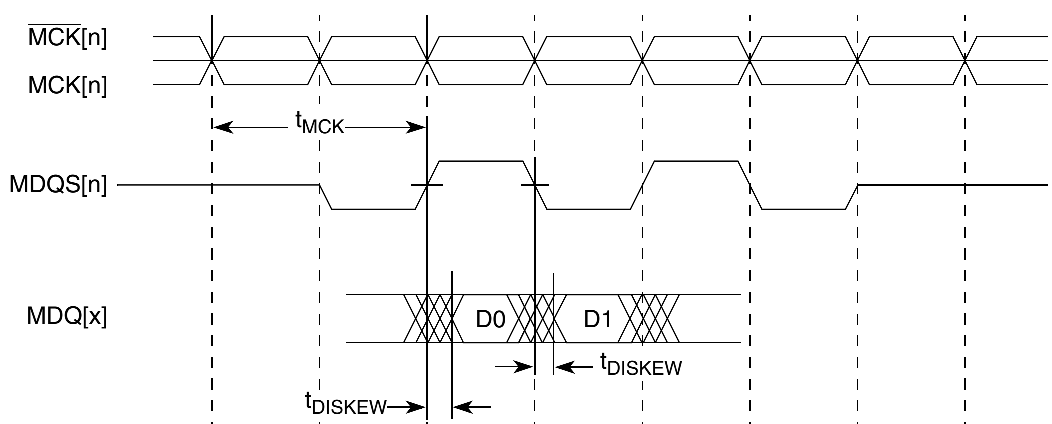


Figure 3. DDR SDRAM Input Timing Diagram (t_{DISKEW})

Figure 10 provides the AC test load for SGMII.

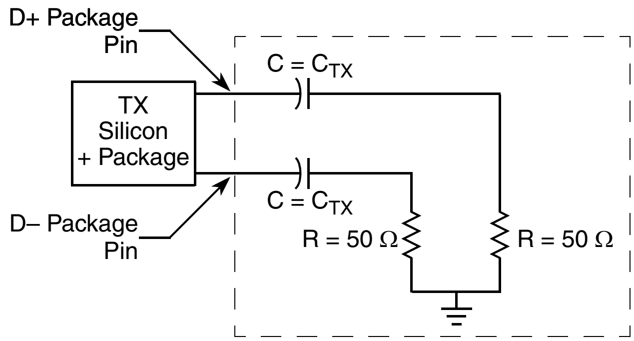


Figure 10. SGMII AC Test/Measurement Load

8.5 FIFO, GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.5.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n* TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

A summary of the FIFO AC specifications appears in Table 28 and Table 29.

Table 28. FIFO Mode Transmit AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t_{FIT}	—	8.0	—	ns	—
TX_CLK, GTX_CLK duty cycle	t_{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t_{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%–80%)	t_{FITR}	—	—	0.75	ns	—

Table 33. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 17 provides the AC test load for eTSEC.

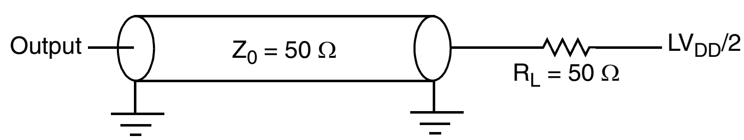


Figure 17. eTSEC AC Test Load

Figure 18 shows the MII receive AC timing diagram.

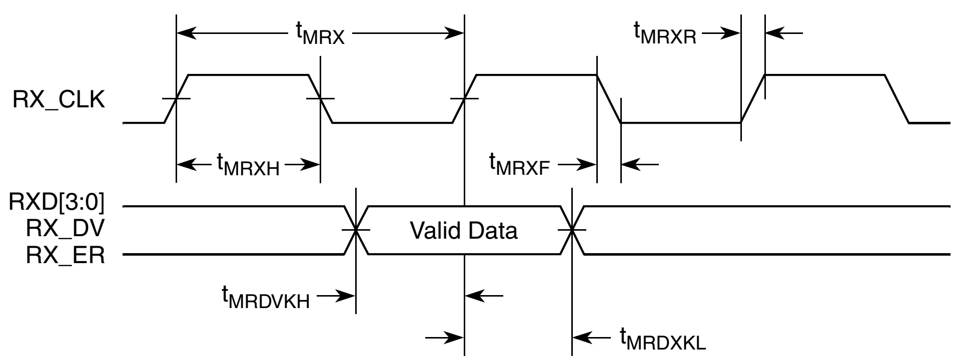


Figure 18. MII Receive AC Timing Diagram

8.7 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.7.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.7.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 38.

Table 38. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t_{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 23 shows the RMII transmit AC timing diagram.

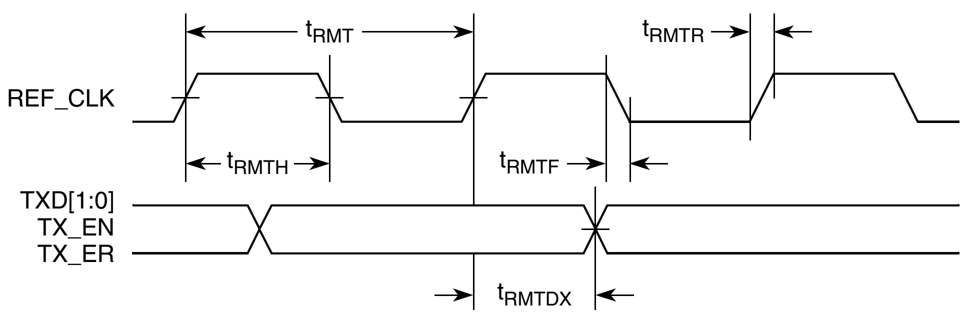


Figure 23. RMII Transmit AC Timing Diagram

Table 50. JTAG AC Timing Specifications (Independent of SYSCLK)[1] (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 3 3	 19 9	ns	5

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 34). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.

Figure 34 provides the AC test load for TDO and the boundary-scan outputs.

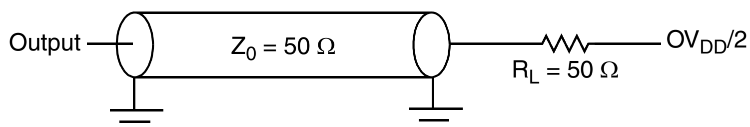


Figure 34. AC Test Load for the JTAG Interface

Figure 35 provides the JTAG clock input timing diagram.

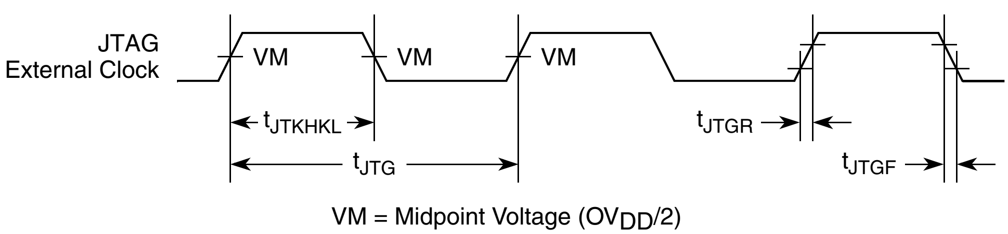


Figure 35. JTAG Clock Input Timing Diagram

Figure 36 provides the $\overline{\text{TRST}}$ timing diagram.

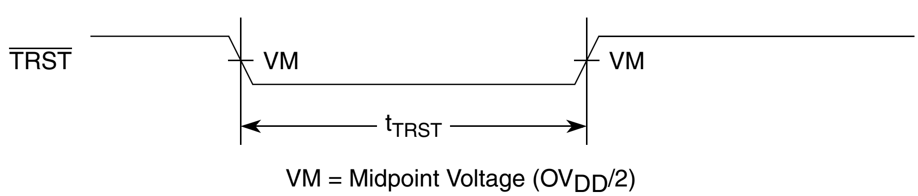


Figure 36. $\overline{\text{TRST}}$ Timing Diagram

14.2 GPIO AC Electrical Specifications

Table 54 provides the GPIO input and output AC timing specifications.

Table 54. GPIO Input AC Timing Specifications

Parameter	Symbol	Typ	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

Figure 40 provides the AC test load for the GPIO.

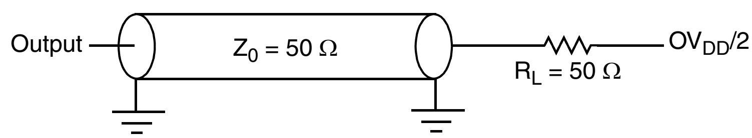


Figure 40. GPIO AC Test Load

15 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8544E.

15.1 PCI DC Electrical Characteristics

Table 55 provides the DC electrical characteristics for the PCI interface.

Table 55. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (V_{IN} = 0 V or V_{IN} = V_{DD})	I_{IN}	—	±5	μA	2
High-level output voltage (OV_{DD} = min, I_{OH} = –2mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. Ranges listed do not meet the full range of the DC specifications of the *PCI 2.2 Local Bus Specifications*.
2. Note that the symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

15.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the SYSCLK signal is used as the PCI input clock. Table 56 provides the PCI AC timing specifications at 66 MHz.

Table 56. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol[1]	Min	Max	Unit	Notes
SYSCLK to output valid	t_{PCKHOV}	—	7.4	ns	2, 3
Output hold from SYSCLK	t_{PCKHOX}	2.0	—	ns	2
SYSCLK to output high impedance	t_{PCKHOZ}	—	14	ns	2, 4
Input setup to SYSCLK	t_{PCIVKH}	3.7	—	ns	2, 5
Input hold from SYSCLK	t_{PCIXKH}	0.5	—	ns	2, 5
$\overline{\text{REQ64}}$ to $\overline{\text{HRESET}}$[9] setup time	t_{PCRVRH}	$10 \times t_{SYS}$	—	clocks	6, 7
$\overline{\text{HRESET}}$ to $\overline{\text{REQ64}}$ hold time	t_{PCRHRX}	0	50	ns	7
$\overline{\text{HRESET}}$ high to first $\overline{\text{FRAME}}$ assertion	t_{PCRHFV}	10	—	clocks	8
Rise time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—
Fall time (20%–80%)	t_{PCICLK}	0.6	2.1	ns	—

Notes:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the SYSCLK clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.2 Local Bus Specifications*.
3. All PCI signals are measured from $OV_{DD}/2$ of the rising edge of PCI_SYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3-V PCI signaling levels.
4. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The timing parameter t_{SYS} indicates the minimum and maximum CLK cycle times for the various specified frequencies. The system clock period must be kept within the minimum and maximum defined ranges. For values see Section 19, "Clocking."
7. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$.
8. The timing parameter t_{PCRHFV} is a minimum of 10 clocks rather than the minimum of 5 clocks in the *PCI 2.2 Local Bus Specifications*.
9. The reset assertion timing requirement for $\overline{\text{HRESET}}$ is 100 μs.

Figure 41 provides the AC test load for PCI.

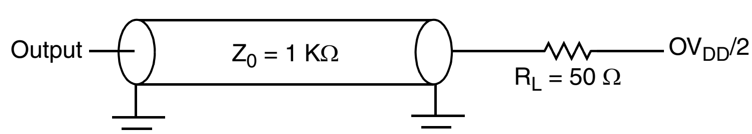


Figure 41. PCI AC Test Load

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 57). Note that the series capacitors, CTX, are optional for the return loss measurement.

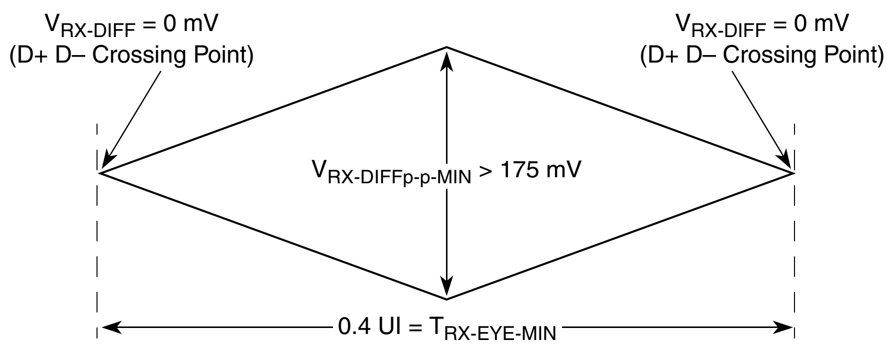


Figure 57. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 58.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

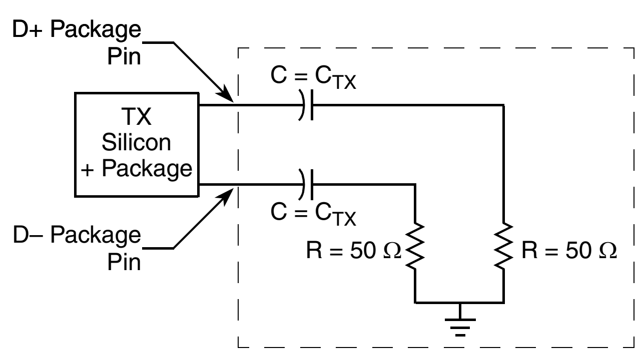


Figure 58. Compliance Test/Measurement Load

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8544E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in Table 61.

Table 61. Package Parameters

Parameter	PBGA[1]
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Note:
1. (FC-PBGA) without a lid.

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV_{DD}	4, 8, 14
EC_MDIO	Y9	I/O	OV_{DD}	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV_{DD}	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV_{DD}	4, 8, 14
TSEC1_COL	R5	I	LV_{DD}	—
TSEC1_CRS	T4	I/O	LV_{DD}	16
TSEC1_GTX_CLK	T1	O	LV_{DD}	—
TSEC1_RX_CLK	V7	I	LV_{DD}	—
TSEC1_RX_DV	U7	I	LV_{DD}	—
TSEC1_RX_ER	R9	I	LV_{DD}	4, 8
TSEC1_TX_CLK	V6	I	LV_{DD}	—
TSEC1_TX_EN	U4	O	LV_{DD}	22
TSEC1_TX_ER	T3	O	LV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV_{DD}	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV_{DD}	4, 8, 14
TSEC3_COL	M9	I	LV_{DD}	—
TSEC3_CRS	L9	I/O	LV_{DD}	16
TSEC3_GTX_CLK	R7	O	LV_{DD}	—
TSEC3_RX_CLK	P9	I	LV_{DD}	—
TSEC3_RX_DV	P8	I	LV_{DD}	—
TSEC3_RX_ER	R11	I	LV_{DD}	—
TSEC3_TX_CLK	L10	I	LV_{DD}	—
TSEC3_TX_EN	N6	O	LV_{DD}	22
TSEC3_TX_ER	L8	O	LV_{DD}	4, 8
DUART				
$\overline{\text{UART\_CTS}}$[0:1]	AH8, AF6	I	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[0:1]	AG8, AG9	O	OV_{DD}	—

Table 62. MPC8544E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
DFT				
L1_TSTCLK	AC20	I	OV_{DD}	18
L2_TSTCLK	AE17	I	OV_{DD}	18
$\overline{\text{LSSD\_MODE}}$	AH19	I	OV_{DD}	18
$\overline{\text{TEST\_SEL}}$	AH13	I	OV_{DD}	3
Thermal Management				
TEMP_ANODE	Y3	—	—	13
TEMP_CATHODE	AA3	—	—	13
Power Management				
ASLEEP	AH17	O	OV_{DD}	8, 15, 21
Power and Ground Signals				
GND	D5, M10, F4, D26, D23, C12, C15, E20, D8, B10, E3, J14, K21, F8, A3, F16, E12, E15, D17, L1, F21, H1, G13, G15, G18, C6, A14, A7, G25, H4, C20, J12, J15, J17, F27, M5, J27, K11, L26, K7, K8, L12, L15, M14, M16, M18, N13, N15, N17, N2, P5, P14, P16, P18, R13, R15, R17, T14, T16, T18, U13, U15, U17, AA8, U6, Y10, AC21, AA17, AC16, V4, AD7, AD18, AE23, AF11, AF14, AG23, AH9, A27, B28, C27	—	—	—
OV_{DD}[1:17]	Y16, AB7, AB10, AB13, AC6, AC18, AD9, AD11, AE13, AD15, AD20, AE5, AE22, AF10, AF20, AF24, AF27	Power for PCI and other standards (3.3 V)	OV_{DD}	—
LV_{DD}[1:2]	R4, U3	Power for TSEC1 interfaces (2.5 V, 3.3 V)	LV_{DD}	—
TV_{DD}[1:2]	N8, R10	Power for TSEC3 interfaces (2.5 V, 3.3 V)	TV_{DD}	—
GV_{DD}	B1, B11, C7, C9, C14, C17, D4, D6, R3, D15, E2, E8,C24, E18, F5, E14, C21, G3, G7, G9, G11, H5, H12, E22, F15, J10, K3, K12, K14, H14, D20, E11, M1, N5	Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V)	GV_{DD}	—
BV_{DD}	L23, J18, J19, F20, F23, H26, J21, J23	Power for local bus (1.8 V, 2.5 V, 3.3 V)	BV_{DD}	—

19 Clocking

This section describes the PLL configuration of the MPC8544E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 63 provides the clocking specifications for the processor cores and Table 64 provides the clocking specifications for the memory bus.

Table 63. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	667 MHz		800 MHz		1000 MHz		1067 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	667	667	667	800	667	1000	667	1067	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 64. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	667, 800, 1000, 1067 MHz			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals (see Table 65):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

19.5 Security Controller PLL Ratio

Table 67 shows the SEC frequency ratio.

Table 67. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1[1]
	1	3:1[2]

Notes:
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

19.6.1 SYSCLK to Platform Frequency Options

Table 68 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

Table 68. Frequency Options of SYSCLK with Respect to Memory Bus Speeds

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
	Platform /CCB Frequency (MHz)						
2							—
3					—	333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500			
8		333	533				
9		375					
10	333	417					
12	400	500					
16	533						

Table 71 provides the thermal resistance with heat sink in open flow.

Table 71. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 25 mm pin fin	Natural convection	6.1
Wakefield 53 × 53 × 25 mm pin fin	1 m/s	3.0
Aavid 35 × 31 × 23 mm pin fin	Natural convection	8.1
Aavid 35 × 31 × 23 mm pin fin	1 m/s	4.3
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	11.6
Aavid 30 × 30 × 9.4 mm pin fin	1 m/s	6.7
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	8.3
Aavid 43 × 41 × 16.5 mm pin fin	1 m/s	4.3

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8544E thermal model without a lid is shown in Figure 60. The substrate is modeled as a block 29 × 29 × 1.18 mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block 29 × 29 × 0.58 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6 × 8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 59 for actual dimensions.

20.2 Recommended Thermal Model

Table 72 shows the MPC8544E thermal model.

Table 72. MPC8544EThermal Model

Conductivity	Value	Units
Die (7.6 × 8.4 × 0.75mm)		
Silicon	Temperature dependent	—
Bump/Underfill (7.6 × 8.4 × 0.070 mm) Collapsed Thermal Resistance		
Kz	6.5	W/m•K
Substrate (29 × 29 × 1.18 mm)		
Kx	18	W/m•K
Ky	18	
Kz	1.0	

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 61). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

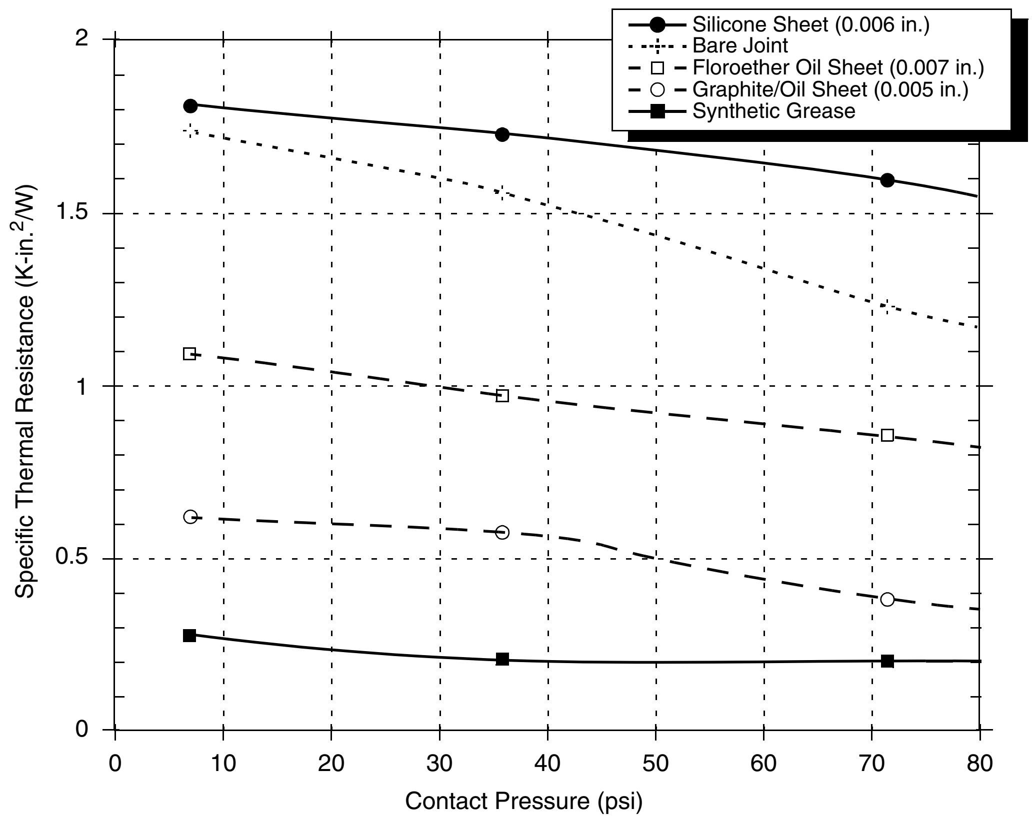


Figure 63. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

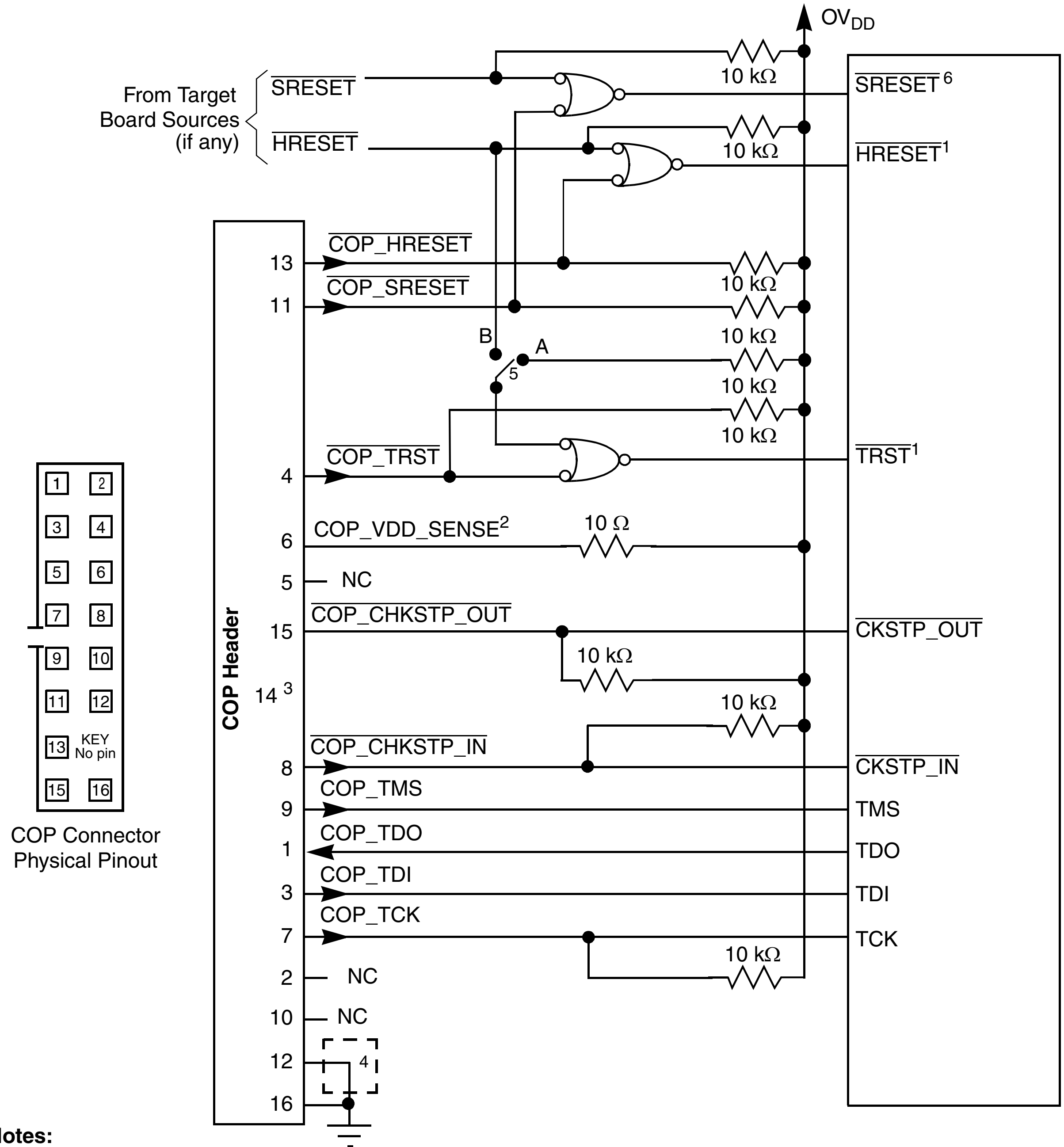
Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

Figure 69 shows the JTAG interface connection.



Notes:
1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 69. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

22.2 Nomenclature of Parts Fully Addressed by this Document

Table 75 provides the Freescale part numbering nomenclature for the MPC8544E.

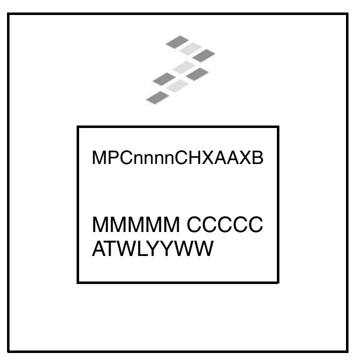
Table 75. Device Nomenclature

MPC	nnnn	E	C	HX	AA	X	B
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range**	**Package[1]**	**Processor Frequency[2]**	**Platform Frequency**	**Revision Level**
MPC	8544	Blank = not included E = included	B or Blank = Industrial Tier standard temp range(0° to 105°C) C = Industrial Tier Extended temp range(–40° to 105°C)	VT = FC-PBGA (lead-free) VJ = lead-free FC-PBGA	AL = 667 MHz AN = 800 MHz AQ = 1000 MHz AR = 1067 MHz	F = 333 MHz G = 400 MHz J = 533 MHz	Blank = Rev. 1.1 1.1.1 A = Rev. 2.1

Notes:
1. See Section 18, "Package Description," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.
3. The VT part number is ROHS-compliant, with the permitted exception of the C4 die bumps.
4. The VJ part number is entirely lead-free. This includes the C4 die bumps.

22.3 Part Marking

Parts are marked as in the example shown in Figure 70.



FC-PBGA

Notes:
MMMMM is the 5-digit mask number.
ATWLYYWW is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 70. Part Marking for FC-PBGA Device

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